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Inter-tier Dynamic Coupling and RF Crosstalk in 3D Sequential Integration

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Abstract—For the first time, an in-depth analysis of the inter-tier dynamic coupling and RF crosstalk of digital circuits in 3D sequential integration enables to conclude on the need of a Ground Plane (GP) for various applications. Experiments in conjunction with TCAD simulations reveal the parasitic capacitances responsible for the dynamic coupling effects and their impact is investigated for a 3D sequential 2-bitcell SRAM cell circuit configuration. Furthermore, we show a greater than 20dB suppression up to 100GHz of the inter-tier RF crosstalk, achieved by the addition of a strategically designed polysilicon Ground Plane between active device layers enabling the possibility of heterogeneous 3DSI integration without metallic Ground Plane. We propose a technological solution to create experimentally a 34nm-thick polysilicon GP of 1.8×10^{20} at/cm³ n-doping and 295 Ω /sq sheet resistance.

I. INTRODUCTION

In 3D sequential integration (also named 3D monolithic integration or 3D VLSI), the stacked devices are fabricated sequentially on top of each other. This process yields to outstanding high-density-contacts between the tiers (up to 10^8 3D via/mm²) owing to the high alignment precision obtained with lithography steppers [1], [2], compared to packaging integration schemes (TSV, copper to copper bonding etc.). However, the ultra-thin Inter-Layer Dielectric (ILD) separating the sequential tiers can act as a Back Gate (BG) oxide for the top transistors, becoming a pathway of electrical interference between stacked devices. Consequently, if no Ground Plane (GP) is introduced, the top device is an asymmetrical SOI MOSFET sensitive to the bottom device electrode voltage variations (Fig.1(a)) or iBEOL metal biasing (Fig.1(b)). The goal of this study is to analyze the immunity of top devices with EOT in 1nm range ($V_{DD}=1V$) for a wide range of applications (Digital, Mixed signal/ RF) when bottom layer is either digital, RF or analog circuit ($V_{DD}=2.5V$). Simulations and experimental measurements will be used to draw conclusion on the necessity to introduce an inter-tier Ground Plane, demonstrating also a novel integration solution.

II. EXPERIMENTS AND SIMULATIONS DETAILS

Experiments: Characterization has been performed on 3D sequential integration devices. Top-tier FDSOI MOSFET are processed at low temperature (LT) (details can be found in [2]) on bottom-tier FDSOI MOSFET fabricated with standard thermal budget. The process specifications are given in Fig.2(a). The dynamic device characterization was performed using the fast IV module (down to 10ns time resolution) of the Agilent B1530A device parameter analyzer.

Simulation tools: For the inter-tier RF crosstalk, we used Ansoft's High Frequency Structure Simulator (HFSS) in

conjunction with Silvaco's TCAD suite. The circuit simulations were performed using the Leti-UTSOI model [3].

III. INTER-TIER COUPLING EFFECTS

A. Electro-Static Coupling

Experiments were performed on digital top-tier transistors varying the bottom tier transistor gate bias (from 0 to $V_{DD}=1V$) to extract the threshold voltage shift (ΔV_{th}) due to electrostatic (DC) coupling as a function of gate length (Fig.3) and are in line with TCAD simulations. The static coupling decreases with the gate length due to the screening by the high source/drain electric field of the top -tier transistor and results in a reduction of the coupling-induced ΔV_{th} by 5mV for nominal device gate length in 28nm FDSOI technology. This level of ΔV_{th} is negligible compared to the mismatch related ΔV_{th} in 28nm FDSOI digital design [4] (Fig.4). However in the case of bottom devices with V_{DD} up to 2.5V, the coupling-induced ΔV_{th} becomes significant and a thicker ILD ($\geq 350nm$) or a GP layer has to be introduced.

B. Dynamic Coupling

Dynamic switching of the back-plane bias has never been involved in the normal operation of conventional planar integrated circuits. However in 3D sequential integration, the pulse-shaped switching of the bottom transistor gate bias may lead to an important dynamic coupling to the top transistor channel. In order to experimentally determine the importance of this effect, we performed high-speed drain current sampling measurements for a top-tier FDSOI MOSFET during the application of a pulse bias from 0 to V_{DD} at its bottom gate (setup shown in Fig. 5). We chose a bottom instead of a top top-tier device because it has a buried oxide (BOX) capacitance almost 5 times higher than the ILD, allowing us to capture more accurately the capacitance-related effects. As shown in Fig. 6(a), it is evident that a parasitic spike occurs in the drain current at the beginning of the back-gate voltage pulse. This spike corresponds to the charging current of the drain-substrate capacitance ($C_{d,bg}$) and the peak amplitude, i_{ac} , is given by Ohm's law for capacitors. Therefore, as the rise time of the switching event at the back gate gets shorter (Fig. 6(b)), i_{ac} is increased, making the dynamic more critical than the DC coupling. TCAD simulations were also performed for the same bias setup and the results are presented in Fig. 8 showing good agreement with the measurements. In order to assess the expected behavior for the top devices, we ran TCAD simulations with the architecture of Fig.7(a). The effect appears to be the same with the bottom tier devices, however in this case the capacitance of interest can be either due to the fringing fields (Fig.7(a)) or the parallel plate capacitance (Fig.7(b)) between the top SOI drain and the bottom SOI gate. To

investigate the impact of the geometrical parameters we varied the width W_{Gtop} and the length L_{Gtop} of the top top-tier devices. As shown in Fig. 8, there is an evident increase of i_{ac} with W_{Gtop} , while there is no dependence on L_{Gtop} . The maximum value of $C_{\text{Dtop,Gbot}}$ is reached when the gate of the bottom tier device is right underneath the top-tier device drain region (Fig.7(b)).

IV. IMPACT ON THE STABILITY OF A SRAM CELL

We examined the configuration of a 3D Sequential 2-bit cell SRAM in 28FD, *i.e.* two stacked (no inter-tier GP) 6T-SRAM cells that are identical in layout design, so that the inter-tier coupling effects are maximized. Mixed-mode TCAD simulations were performed on a circuit containing the stacked SRAM cells. A schematic of the top-tier circuit is presented in Fig. 9: each transistor is composed by a TCAD structure including the stacked transistors of Fig.2 (a) and all the necessary physical models. Moreover, the impact of the relative positioning was studied, by placing each top-tier transistor drain in different distances with respect to the bottom-tier transistor gate. We considered two cases: a gate overlap=1 when all bottom- and top-tier transistor gates are perfectly aligned (Fig. 7(a)) and a gate overlap=0 when the bottom-tier gates are aligned with the respective top-tier transistor drains (Fig. 7(b)).

First, we obtained the DC characteristics of the top-tier SRAM circuit for each case of bottom-tier operation (no power supply, stored'0', stored'1') and for the two positioning scenarios (gate overlap=0/1), revealing a coupling induced SNM reduction of only 10 mV for the top tier SRAM (see Fig. 10). Afterwards, we emulated a Read operation on the top tier SRAM cell with '1' stored at the Channel High (CH) node (Fig. 11(a)), and a write operation was emulated for the bottom SRAM showing that the dynamic coupling is not strong enough to result in a Read destructive operation (Fig. 11(b)). The demonstrated immunity of a sensitive digital circuit like SRAM to both static and dynamic coupling shows that digital on digital circuits with 130nm ILD thickness do not need an inter-tier GP.

V. IMPACT ON RF APPLICATIONS

C. Ring Oscillator (RO)

In order to assess the sensitivity of top-tier RF circuits on electrostatic coupling due to bottom-tier analog circuits without GP in between, we selected the circuit example of a 3-stage RO (Fig.12). Fig. 13(a) shows a frequency shift of 510MHz for a 30.5 GHz oscillating signal due to the 2.5V shift of the bottom-tier electrode bias. This 1.67% shift is far from negligible for RF applications, therefore a GP layer is needed for inter-tier isolation. However, regarding the phase noise of the top RO, there is no observable impact of DC coupling from the bottom Analog tier (Fig. 13(b)).

D. Intertier RF Crosstalk

Due to the proximity of the two tiers, electromagnetically induced crosstalk can take place between them. Prior work [5] - [10] was carried out for the isolation of active devices targeting planar and 3D technologies, however they require complex process techniques, not suitable for 3D sequential integration. Here we examine an efficient way of inter-tier crosstalk isolation with the insertion of a polysilicon GP between the sequential tiers. In order to estimate the inter-tier RF decoupling efficiency of the GP, we followed the methodology proposed in [11],[12] implementing the

simulation setup of Fig. 14 and testing various materials for the GP region (SiO₂, PolySi, Copper). The S21 parameter that indicates the forward voltage gain from the in-port (bottom SOI gate) to the out-port (top SOI drain) is used to analyze the intertier crosstalk. Figure 16 shows the TCAD simulation results for the S21 parameter in the frequency range of 0.01–100 GHz for SiO₂ (no GP) and a PolySi GP. We observe that increasing the doping concentration of the PolySi GP can help extend the decoupling frequency range: for a concentration of 10^{20} cm^{-3} , there is a 20dB reduction up to 100GHz. Figure 17 also shows the results obtained by HFSS, to test the scenario of a Copper GP. The latter shows 8 dB more crosstalk attenuation than the highly doped polysilicon GP, related to the optimum conductivity of the copper. Repeating the simulation setup of Fig. 16 and expanding the GP area with respect to the top tier device active region we extract the attenuation level as a function of the well GP coverage of the top tier active device region. As Fig. 18 shows, there is a GP sizing that can result to the maximum reduction level, whereas the difference between the two tested materials varies from 3dB to 8dB. However, the increase of the area yields a decrease of the decoupling frequency range, related to the bias attenuation across the GP level. To address this issue, we increased the number of ground (gnd) taps for the GP layer (Fig. 19) up to a total number of 6, indeed observing from figure 20 that both the decoupling frequency range and the suppression level are increased.

E. Inter-tier GP processing challenges and solutions

A polysilicon GP offers several advantages compared to a metallic GP. Firstly, it is compatible in terms of Front End Of Line (FEOL) contamination environment for top MOSFET processing. Secondly, it offers the possibility of dual doping type to propose several V_{TH} flavors without requiring gate stack engineering or channel doping. However, for RF applications where high GP doping level are required, traditional GP doping through the top channel cannot be applied (Fig.21). To increase the GP doping concentration above this limit, the polysilicon needs to be doped directly after its deposition or deposited using in-situ doped epitaxy. With GP direct doping, a doping concentration of $1.8 \times 10^{20} \text{ at/cm}^3$ has been reached (Fig.22), enabling one to reach a sheet resistance of 295 Ω/sq for a 34nm-thick polysilicon layer. Therefore, this type of GP answers to all the specifications in terms of doping level and sheet resistance (-20 dB up to 100 Ghz for 1 GP tap), as well as thickness (to preserve the 3D contact aspect ratio (AR)) and FEOL contamination category.

VI. CONCLUSION

Through experiments and simulations we have shown that, for purely digital 3D sequential circuits there is no major coupling between top and bottom tiers, therefore inter-tier GP integration is not needed. However, when it comes to mixed signal and RF applications, a polysilicon GP layer provides the necessary immunity to inter-tier coupling effects like crosstalk. We have also demonstrated a novel integration scheme of inter-tier isolation with a polysilicon GP, highlighting its SOI compatibility and the advantages over metallic solutions.

ACKNOWLEDGMENT

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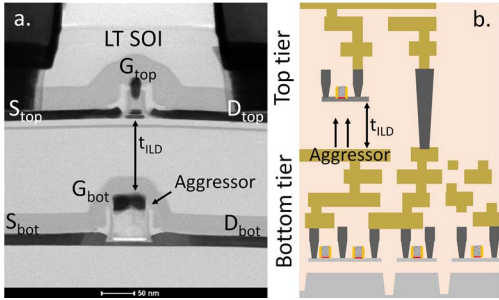


Fig. 1: (a) TEM cross-section of two stacked transistors fabricated in 3D sequential (b) Schematic of structure in a 3D sequential integration scheme with iBEOL.

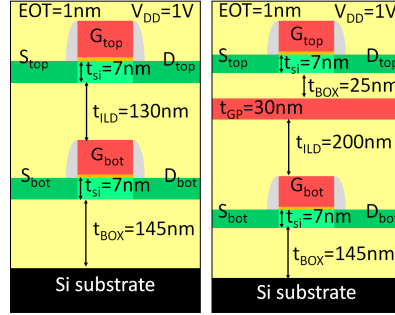


Fig. 2: Schematic of the devices under study with (a) and without (b) GP. The scope of the study is to conclude on the GP insertion need.

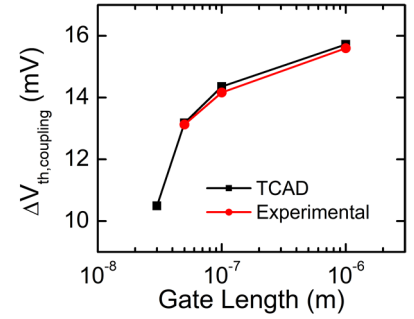


Fig. 3: Threshold voltage shift vs. gate length for top tier SOI. 28FD nominal length devices show better immunity to inter-tier DC coupling.

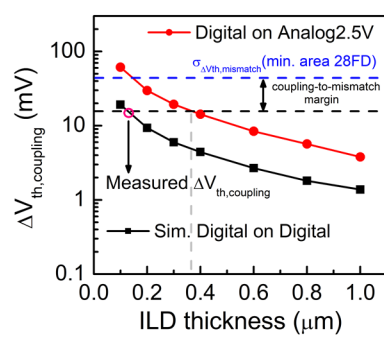


Fig. 4: Threshold voltage shift due to DC coupling for 2 different stacks of devices. To preserve the same coupling-to-noise margin for Analog bottom-tier devices a thicker ILD ($\geq 350\text{nm}$) or a GP layer has to be introduced.

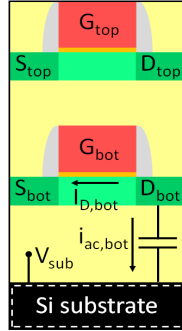


Fig. 5: Setup for bottom-tier SOI dynamic coupling characterization.

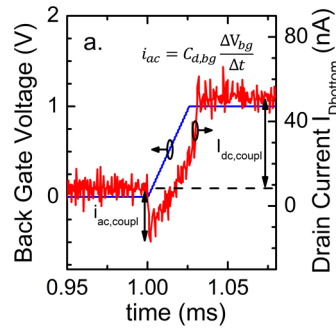


Fig. 6: Dynamic coupling transient results for a bottom tier SOI ($W=30\mu\text{m}$, $L=0.5\mu\text{m}$) at $V_G=0.1\text{V}$. (a) Experimental transient for $\tau_r=30\mu\text{s}$ with the applied pulse at the back gate of the device (blue) and the measured drain current (red) revealing the parasitic spike i_{ac} . (b) TCAD simulation for a shorter rise time ($\tau_r=3\mu\text{s}$) shows that the i_{ac} becomes greater than the coupling-induced DC shift ($I_{dc,coupl}$).

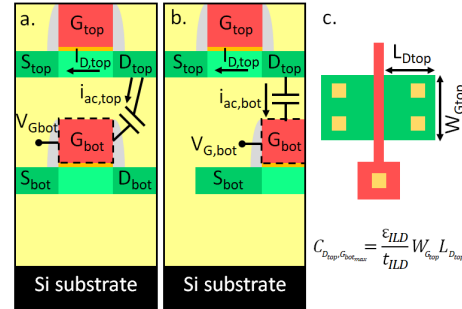


Fig. 7: (a) Setup for top-tier SOI dynamic coupling characterization, (b) worst case scenario (max. $C_{Dtop,Gbot}$), (c) top-tier SOI layout view.

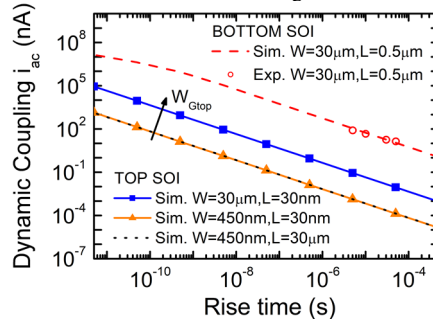


Fig. 8: Peak amplitude of i_{ac} vs rise time of the applied pulse at the back gate of the Bottom/Top SOI for Fig.5/7(a) case. The i_{ac} increases with W_{Gtop} whereas it does not change with L_{Gtop} .

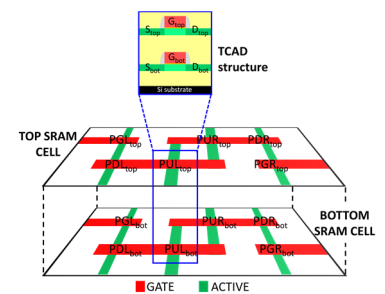


Fig. 9: Simplified layout representation of the superimposed SRAM. Each top-tier SOI is comprised by the TCAD structure shown here.

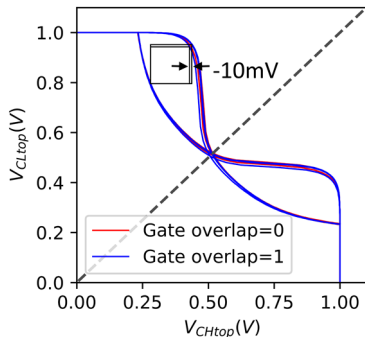


Fig. 10: SNM reduction due to bottom-tier SRAM cell static coupling. The 10mV SNM reduction observed is not critical for the stability of the SRAM cell [4].

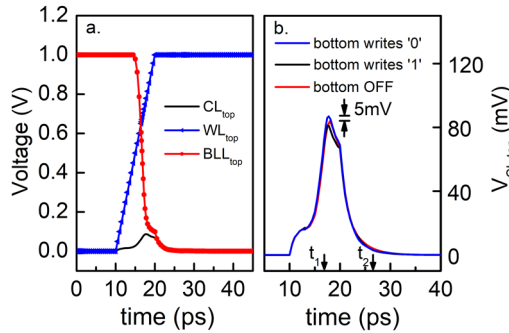


Fig. 11: (a) Read operation for top-tier SRAM cell: The WL_{top} is enabled and BLL_{top} discharges to $V_{CL,top}$. (bottom SRAM off). (b) $V_{CL,top}$ during a write operation ($0 \rightarrow 1\text{V}$ and $1 \rightarrow 0\text{V}$ from t_1 to t_2) with 10ps rise time (shortest in 28FD [13]) at the bottom SRAM.

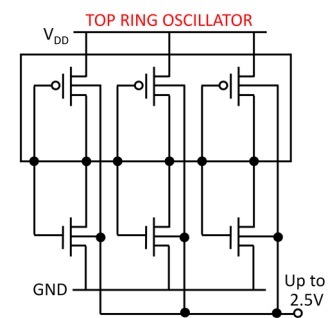


Fig. 12: Top tier Ring Oscillator composed of three NOT gates. Up to 2.5V bias is applied at the BG of each top-tier SOI (V_{DD} for bottom-tier SOI with $EOT=5\text{nm}$).

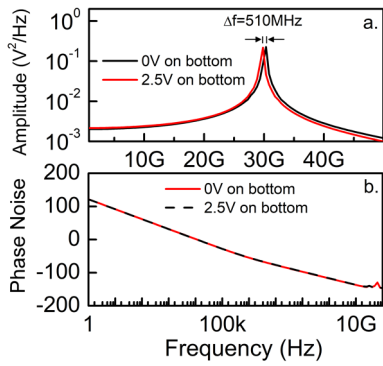


Fig. 13: FFT (a) and Phase noise shift (b) for top-tier Ring Oscillator with 2.5V bias application at each SOI back-gate.

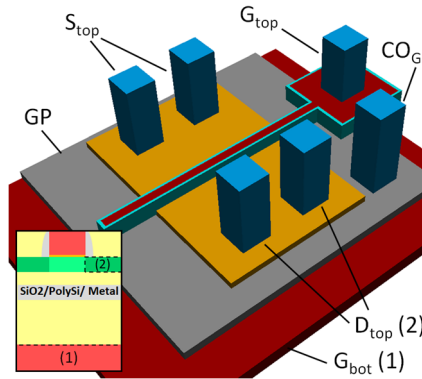


Fig. 14: Simulation setup to determine the GP decoupling efficiency. The GP area is 2x the top active with 1 gnd tap. Inset: Cross-section view.

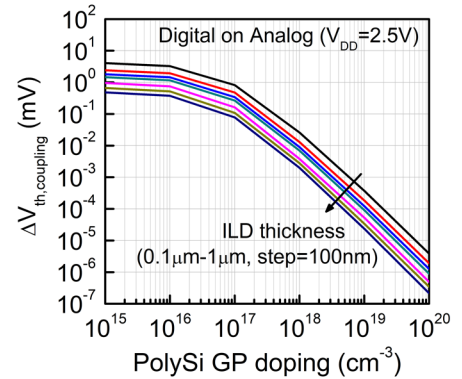


Fig. 15: Threshold voltage shift vs. GP doping concentration. The insertion of the PolySi reduces the DC coupling by 10^5 .

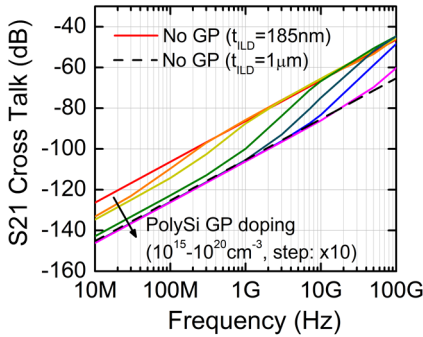


Fig. 16: Crosstalk vs. frequency. PolySi GP (10^{20} cm^{-3}) offers 20dB of suppression up to 100GHz (1 gnd tap). GP insertion preserves 3D contact AR: W/o GP, $1 \mu\text{m}$ thick ILD can reach the same suppression level.

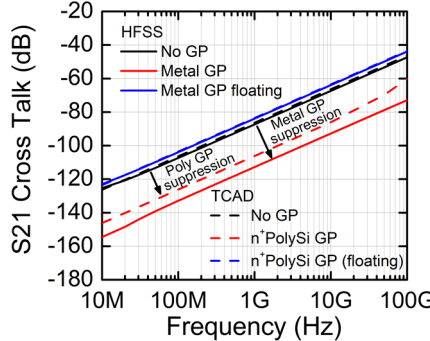


Fig. 17: Copper GP offers 8 dB more crosstalk attenuation than the highly doped PolySi GP. The already very high attenuation level and FEOL compatibility make PolySi GP the ideal choice.

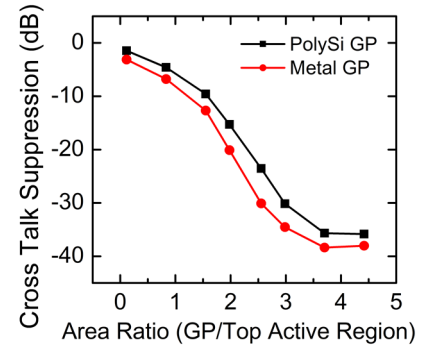


Fig. 18: Expanding the GP area, suppression level of crosstalk is increased. There is a maximum covering of the top-tier SOI for which GP reaches the suppression limit.

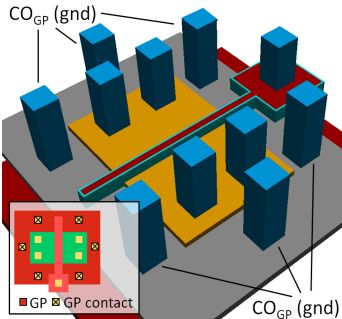


Fig. 19: The GP area now is 3x the top active and gradually up to 6 gnd taps are added. Inset: Top-tier layout view.

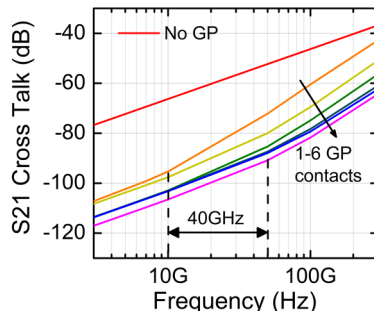


Fig. 20: Crosstalk vs. frequency. A larger PolySi GP needs greater number of gnd taps for decoupling frequency up to 100GHz. Optimum GP size: minimum number of gnd taps (denser integration) for good suppression.

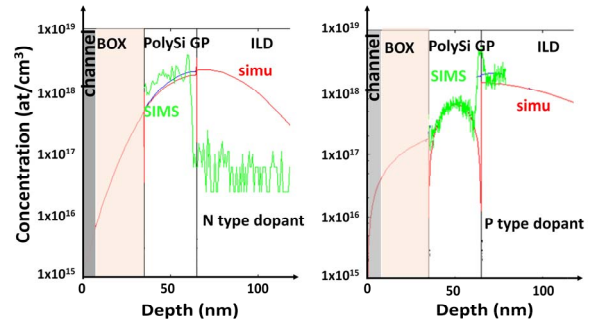


Fig. 21: Examples of GP doping conditions (N&P type) through thin channel for SOI devices. GP concentration cannot exceed the $1 \times 10^{18} \text{ at/cm}^3$ in order to avoid top channel parasitic doping.

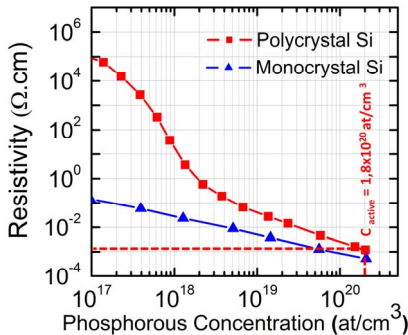


Fig. 22: Direct doping of GP enables doping concentration of $1.8 \times 10^{20} \text{ at/cm}^3$ [14].

TOP TIER	Digital ($V_{DD}=1V$)	Mixed signal/RF
BOTTOM TIER		
Digital ($V_{DD}=1V$)	No GP needed, $t_{ILD}=130\text{nm}$ (Verified with SRAM cell in [4] and this work)	GP needed depending on frequency and layout of the application
RF	For typical digital logic level noise margins, GP may not be needed	
Analog ($V_{DD}=2.5V$)	$t_{ILD}=350\text{nm}$ or GP insertion (Due to $V_{th,top}$ shift)	GP needed (Verified with RO case)

Fig. 23: Summary table on the need of inter-tier GP.

- [1] P. Batude et al., p. 3.1.1-3.1.4, IEDM'17; [2] L. Brunet et al., p. 1-2 VLSI'16; [3] T. Poiroux et al., p. 2751-68, 62, TED'15; [4] P. Sideris et al. EUROSOI'19; [5] H.-S. Kim et al., p. 160-162, LED'04; [6] T.-S. Chen, p. 255-260 TED'04; [7] S. Stefanou et al., p. 486-491, TED'04; [8] J. H. Wu et al., p. 410-412 MWCL'01; [9] W.-K. Yeh et al., pp. 817-819 TED'04; [10] A. Margomenos et al., p. 25-32 TMTT'03; [11] S. K. Kim et al., p. 1459-1467, TED'05 [12] A. Vandoren et al., p. T56-T57, VLSI'19 [13] N. Planes et al., p. 133-134, VLSI'12; [14] J. Electrochem. Soc. 1979, vol.126. N°6 p.1019.

Fig. 24: References