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# Effects of Contact Potential and Sidewall Surface Plane on the Performance of Vertical GaN Nanowire MOSFETs for Low Voltage Operation

Dong-Hyeok Son<sup>1</sup>, Terirama Thingujam<sup>1</sup>, Jeong-Gil Kim, Dae-Hyun Kim, In Man Kang, Ki-Sik Im, Christoforos Theodorou, Gerard Ghibaudo, Sorin Cristoloveanu, and Jung-Hee Lee\*

**Abstract--** GaN-based materials are expected to show excellent immunity against short-channel effects because they have relatively lower permittivity and higher electron effective mass, compared to other materials such as Si, Ge, and In(Ga)As. To further reduce the short-channel effects, it is important to enhance the gate controllability of the device by utilizing a gate-all-around structure. In this work, GaN vertical GAA nanowire MOSFETs with various diameters of 120, 75, and 45 nm have been fabricated. The device with a diameter of 120 nm shows threshold voltage of 0.7 V, drain saturation voltage of 0.5 V, and subthreshold swing of 70 mV/decade, which would be suitable for low voltage/power applications. However, the devices with smaller diameter of 75 and 45 nm show peculiar characteristics, such as a second rise of the drain current in output characteristics and a negative transconductance. Systematical analyses with dc and noise measurements as well as TCAD simulations show that the observed characteristics are due to the contact potential which strongly depends on the nanowire diameter and the trapping effect into deep traps at the sidewall surface of the nanowire channel.

**Index Terms--**GaN vertical nanowire MOSFET, low voltage application, nanowire diameter, contact potential, negative transconductance

## I. INTRODUCTION

III-V semiconductors such as GaAs and InAs offer superior material and electrical properties and are considered to replace the channel layers in the conventional Si-based devices which technologies have been quiet close to their limitations [1-6]. In contrast with other III-V

semiconductors, GaN-based materials and devices have been rarely studied for low-power purpose. Instead, they have been generally considered as promising candidates for high power and high frequency applications due to their material advantages such as wide bandgap energy, high breakdown field, and high electron saturation velocity [7-8]. Nevertheless, theoretical and simulation studies have shown that GaN nanowires could be the proper elements for extremely short channel MOSFET compared to GaAs, InAs, Ge, and Si-based nanowires [9]. Indeed, relatively small permittivity and large electron effective mass of the GaN-based materials are important parameters for alleviating the short channel effects because they reduce the source-to-drain tunneling current and the natural length which represents the penetration distance of the electric field lines from the drain [10]. Recently, GaN-based 3-dimensional FETs with gate-all-around (GAA) structures have shown improved device performances such as linearity, suppressed current collapse, high on/off-state current ratio, and high voltage characteristics, resulting from the enhanced gate control of the channel [11-15]. Especially, GaN vertical nanowire MOSFET features small threshold voltage of ~ 0.6 V and saturation drain voltage of less than 1 V which open up possibility of GaN devices as a future logic applications [15].

In this work, we present GaN GAA vertical nanowire MOSFETs (VNW-MOSFETs) with variable diameter ( $d_{NW}$ ). The device with  $d_{NW}$  of 120 nm has m-plane sidewall surface with hexagonal symmetry and features normal low-voltage operation. The devices with smaller  $d_{NW}$  of 75 and 45 nm show two additional characteristics such as second rise of drain current in output characteristic and negative transconductance (NT). Systematic experiments including low-frequency noise point on the role of the drain contact potential and the trapping effects through deep-level traps at the irregular sidewall surface of the nanowire. These results offer a sound base for further optimization of VNW-MOSFETs with narrow diameter.

## II. DEVICE FABRICATION

### A. Formation of GaN vertical nanowire.

The epitaxial layers for the nanowire consisted of an  $n^+$ -GaN layer for source, an undoped GaN channel layer, and an

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$n^+$ -GaN layer for drain with thickness of 800, 300, and 500 nm and with doping concentration ( $N_D$ ) of  $2.0 \times 10^{18}$ ,  $2.0 \times 10^{16}$ ,  $2.0 \times 10^{18} \text{ cm}^{-3}$ , respectively, which were sequentially grown by metal-organic chemical vapor deposition (MOCVD) on sapphire (0001) substrate. From the x-ray diffraction (XRD) measurement, the full widths at half maximum (FWHM)s for GaN (002) and (102) planes for this work were 314 and 310 arcsec, respectively. The screw and edge dislocation densities were  $9.5 \times 10^7 \text{ cm}^{-2}$  and  $5.0 \times 10^8 \text{ cm}^{-2}$ , respectively. Considering the GaN nanowire diameter of 120 nm for this work, the numbers of dislocations one per nanowire were  $1.07 \times 10^{-2}$  for screw and  $5.65 \times 10^{-2}$  for edge dislocations, respectively. Even with 9 parallel VNW in a device the probability of 1 dislocation per nanowire is very small, which unlikely to affect the device operation.

To form the etch mask layer, the  $\text{HfO}_2/\text{SiO}_2$  dielectric layer was first deposited with using atomic layer deposition (ALD) and plasma-enhanced chemical vapor deposition (PECVD) in sequence. The Ti/Ni/Au metal layer was evaporated on the dielectric layer after electron-beam lithography to define the initial mask pattern. The pattern was transferred to the dielectric  $\text{HfO}_2/\text{SiO}_2$  layer with using  $\text{CF}_4$ -based inductively coupled plasma reactive ion etching (ICP-RIE) to complete the double metal-dielectric mask structure.  $\text{Cl}_2$ -based ICP-RIE was then carried out to selectively etch GaN down to 1  $\mu\text{m}$  depth with using the mask, which results in flat-top cone-shape nanowires. Anisotropic lateral wet etching in TMAH solution (5 % concentration at 80 °C) was followed to form pillar-shaped nanowires with very steep sidewall. After 30 min wet etching in TMAH solution, however, different shapes of nanowires were obtained as shown in Fig. 1(c) and (d); hexagonal symmetry nanowire pillar with m-plane sidewalls and non-hexagonal irregular nanowire pillar with mixed-plane sidewalls rather than a single crystal plane, respectively. The difference in shape for the nanowires after TMAH wet etching depends on the strength of the adhesion between the etch mask layer and the top surface of the GaN nanowire. If the adhesion of the mask layer on the top surface of the GaN nanowire is sufficiently strong, the mask layer can be sustained during the anisotropic lateral TMAH wet etching, which typically leads to the hexagonal GaN nanowire pillar with m-plane sidewall surfaces as shown in Fig. 1 (c). However, if the adhesion is weak, the mask layer can be peeled off during the TMAH wet etching to expose the vulnerable edges between c-plane surface (top of nanowire) and m-plane surface (sidewall of nanowire) [19]. Then, the etching loses the anisotropic property and proceeds toward all lateral directions, which results in forming the GaN nanowires with irregular sidewall surfaces with various crystal planes, as shown in Fig. 1 (d) [20]. After formation of GaN vertical nanowires, the etch mask layer was removed in Hydrofluoric acid (HF) solution.

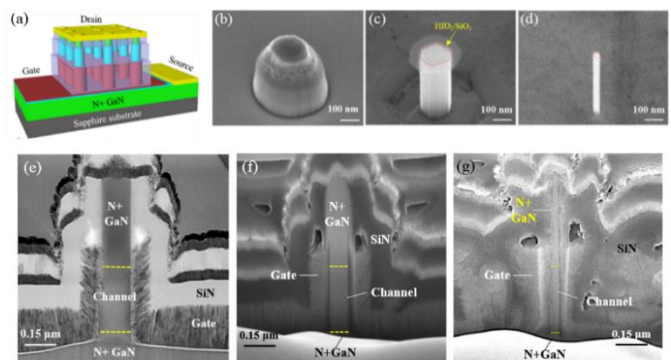
### B. GaN VNW-MOSFET fabrication.

For the formation of ohmic contact, the nanowire structure was coated with photo-resist (PR). In general, there exist a finite difference in the PR thickness between top and bottom

of nanowire due to high etching aspect ratio in GaN layer. The etch-back process utilizing dry etching was applied to selectively remove the PR only on top of the nanowire. This etch-back process enables the Si/Ti/Al/Ni/Au drain ohmic metal to be deposited only on the top of nanowires. After depositing the source ohmic metal, rapid thermal annealing was followed at 800 °C in  $\text{N}_2$  ambient to obtain the ohmic contact for the source and the drain,. The specific contact resistance was  $3 \times 10^{-5} \Omega\text{-cm}^2$ , which was evaluated from transmission line method (TLM).

For the formation of the gate, 10 nm-thick ALD  $\text{Al}_2\text{O}_3$  gate dielectric, 200 nm-thick sputtered Cr gate, and 50 nm-thick PECVD SiN protection layer were sequentially deposited. To define the gate, coating of PR and etch-back process enable revealing the top of vertical nanowire. The SiN protection layer was etched in buffered oxide etch (BOE) solution and the Cr gate was etched with  $\text{O}_2$  plasma. The  $\text{Al}_2\text{O}_3$  dielectric layer, which covers the drain, protects the ohmic metal on the drain during the  $\text{O}_2$  plasma etching. The overlap length of gate metal at drain-side access region was 100 nm.

To ensure electrical isolation between the gate and the drain, 100 nm-thick PECVD SiN spacer layer was deposited. SiN spacer layer on top of vertical nanowires was selectively removed by coating of PR and etch-back process mentioned above to reveal the drain metal on top of nanowire. Additional  $\text{O}_2$  plasma etching was performed for removal of PR. Before deposition of pad metal on top of source, drain and gate electrode, dielectric layer on those electrode was selectively removed by using UV-lithography and ICP-RIE, in sequence. The  $\text{Al}_2\text{O}_3$  layer on the drain, the source, and the gate electrode was selectively removed with using ICP-RIE and the pad metal layer was finally deposited. The cross-sectional image in Fig. 1 (e) is for the hexagonal m-plane sidewall GaN VNW-MOSFET with  $d_{\text{NW}}$  of 120, and the images in Fig. 1 (f) and (g) are for the non-hexagonal sidewall GaN VNW-MOSFET with  $d_{\text{NW}}$  of 75 and 45 nm, respectively.



**Figure 1** (a) Schematic of GaN VNW-MOSFET. (b) SEM image after dry etching of VNW. (c) SEM image of VNW with 120 nm diameter after TMAH etching. (d) SEM image of VNW with 56 nm diameter after TMAH etching. (e) Cross-sectional image of GaN VNW-MOSFET with diameters of (e) 120 nm, (f) 75 nm, and (g) 45 nm.

### C. Device measurement and characterization.

The semiconductor parameter analyzer (Keysight HP4156) was used to apply the grounded source voltage, drain voltage and gate voltage to measure the drain current. The noise measurement system (Synergie Concept Noisys7) was used to

measure the low frequency noise characteristic. Silvaco TCAD software was used for the simulation of GaN VNW-MOSFETs.

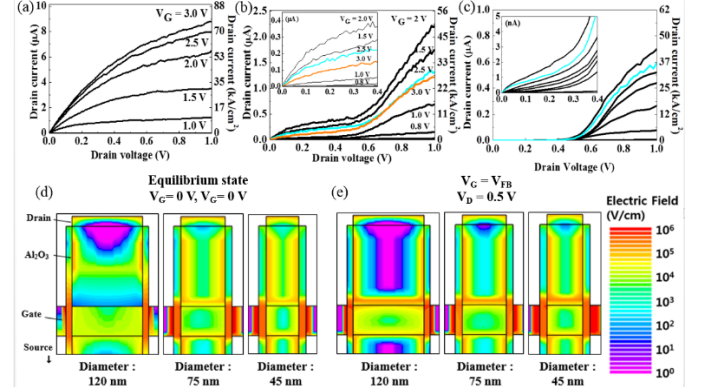
### III. RESULTS AND DISCUSSION

Fig. 2 (a), (b), and (c) show the output characteristics of the GaN VNW-MOSFETs with  $d_{NW}$  of 120, 75, and 45 nm, respectively. The device with  $d_{NW}$  of 120 nm has hexagonal nanowire pillar with m-plane sidewall surface and the devices with  $d_{NW}$  of 75 and 45 nm have non-hexagonal nanowire pillar with various crystalline planes in the sidewall. The GaN VNW-MOSFET with  $d_{NW}$  of 120 nm exhibits considerably lower saturation drain voltage ( $< 0.5$  V) compared to conventional GaN-based planar devices because the drain current in such a narrow nanowire channel can be easily pinched-off due to the electric field distribution between the gate and the drain [15].

On the other hand, the output characteristics of the device with  $d_{NW}$  of 75 nm show even lower saturation voltage at low current level, but exhibit a kink (second rise in drain current) at drain voltage ( $V_D$ ) of  $0.5 \sim 0.6$  V. Furthermore, the device with  $d_{NW}$  of 45 nm shows output characteristics with offset-like turn-on voltage at  $V_D = \sim 0.5$  V. For  $V_D < 0.5$  V, the drain current is two orders of magnitude lower than in the device with  $d_{NW}$  of 75 nm. These contrasting behaviors can be understood from the simulations of the electric field distribution. At equilibrium ( $V_G = V_D = 0$  V), the heavily  $n^+$ -doped ( $2 \times 10^{18} \text{cm}^{-3}$ ) access region between the gate and the drain contact comprises a 20 nm thick depletion region due to the surface potential formed at the  $\text{Al}_2\text{O}_3$ -deposited sidewall of the GaN nanowire channel [16]. This surface depletion induces a small but finite contact potential at the drain terminal. In the case of the device with  $d_{NW}$  of 120 nm, the contact potential is not important since a sufficiently wide access region remains neutral, as purple region shown in Fig. 2 (d). At  $V_G > V_{TH}$ , the device shows normal output characteristics with applying  $V_D$ . In the device with  $d_{NW}$  of 75 nm, the neutral access region becomes very narrow and the drain contact deviates from the original ohmic nature by building a contact barrier of 0.16 eV at the center of the drain contact. When the device is turned on, relatively low output current flows due to this contact barrier and the increased access resistance at low  $V_D$ . However, applying  $V_D$  of  $\sim 0.5$  V lowers the height of the contact barrier to a negligible value, as shown in Fig. 2 (e), and hence the output current rapidly increases, showing an apparent second rise in drain current. For the device with  $d_{NW}$  of 45 nm, the resistance of the  $n^+$ -access region becomes very high due to very narrow neutral region and the contact potential increases to 0.3 V at equilibrium. With  $V_G > V_{TH}$ , extremely small drain current flows at low  $V_D$ . A  $V_D$  of  $\sim 0.5$  V lowers the contact potential close to the thermal potential, and unblocks the device. This results in output current increase with offset-like turn-on voltage as in Fig. 2 (c).

The effect of higher  $V_D$  is two-fold; it lowers the contact barrier and supplies energy to electrons. We conclude that this abnormal behavior originates from the nano-channel

squeezing caused by the surface depletion regions. The solution to reduce the surface depletion and series resistance is to increase the  $n^+$ -type doping in the ungated access region [17].



**Figure 2** Output characteristics of GaN VNW-MOSFETs with diameter of (a) 120 nm, (b) 75 nm, and (c) 45 nm. (d) and (e) are simulated electric field profiles in the corresponding devices.

The transfer characteristics of the device with  $d_{NW}$  of 120, 75, and 45 nm at  $V_D = 1$  V are shown in Fig. 3. The corresponding threshold voltages ( $V_{TH}$ ), extracted at fixed drain current of  $(0.1) \times (\text{channel width/channel length}) \mu\text{A}$  [18], are 0.7, 0.9, and 1.2 V, respectively. In equilibrium, the surface potential of the nanowire channel with doping density of  $2 \times 10^{16} \text{cm}^{-3}$  results in depletion thickness of  $\sim 210$  nm [18], which forces the entire nanowire channel of the device with  $d_{NW}$  of 120 nm to be depleted and ensures normally-off operation. The flat-band voltages ( $V_{FB}$ ), estimated from the  $V_G$  at maximum transconductance, were 1.19, 1.40, and 1.75 V for the devices with  $d_{NW}$  of 120, 75, and 45 nm, respectively. The  $V_{FB}$  value calculated from the work-function of Cr gate and electron affinity of non-polar GaN sidewall surface with doping concentration of  $2 \times 10^{16} \text{cm}^{-3}$  is 1.1  $\sim$  1.2 V [19], similar to that of our wider device.  $V_{FB}$  increases in narrower  $d_{NW}$  where the surface potential makes the nanowire channel more deeply depleted and further raises the conduction band ( $E_C$ ) above the Fermi level ( $E_F$ ) in inside of the nanowire channel. As a result, a higher positive gate voltage is needed to recover flat energy bands.

Another interesting aspect is that devices with  $d_{NW}$  of 75 and 45 nm exhibit negative transconductance (NT) characteristics. This is mainly due to the significant trapping effect related to the deep traps at sidewall surface of the GaN nanowire channel, rather than trapping/detrapping through shallow surface traps. Narrow devices have higher deep trap density as well as shallow trap density, because their surface features various crystal planes and relatively rough surface as discussed above. The device with  $d_{NW}$  of 120 nm has hexagonal symmetry with smooth m-plane surface which results in the lower interface trap density [20-21].

The trapping effect through deep traps is responsible for the NT characteristics observed from the output and transfer curves for the narrow devices in Fig. 2 and 3. They can be explained as follows: when  $V_G$  is lower than  $V_{TH}$ , the entire

nanowire channel is completely depleted due to the gate electric field from the GAA structure and hence no current flows. As  $V_G$  increases above  $V_{TH}$ , the current starts to flow in the center and expands in the entire nanowire channel; the current continually increases until  $V_G$  reaches the  $V_{FB}$ , and the transconductance attains a maximum as shown in Fig. 3. At  $V_{FB}$ , the depletion layer disappears and the energy bands across the channel become flat. For even higher  $V_G$ , electrons tend to accumulate at the surface of the nanowire channel due to downward band bending and hence the surface accumulation current adds to the volume current.

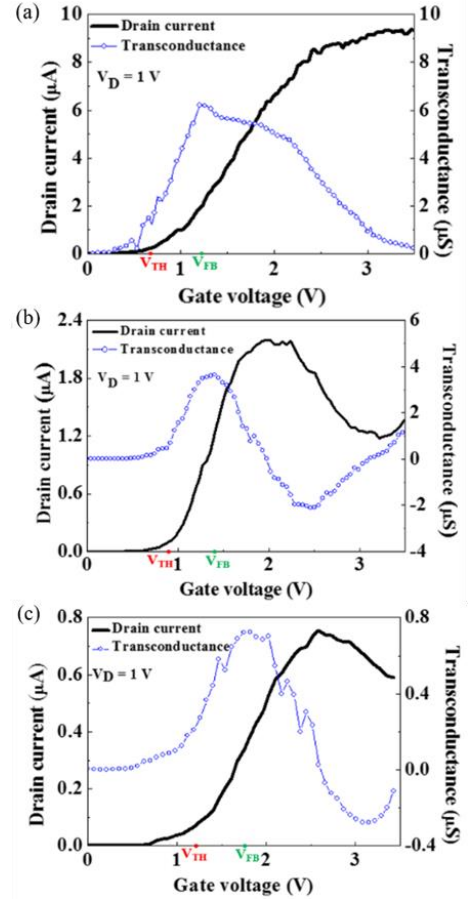
Simultaneously, some electrons tend to be captured into the deep traps as well as shallow traps at nanowire surface. Nevertheless, the device current keeps increasing until  $V_G$  reaches the peak voltage ( $V_{peak}$ ). As  $V_G$  increases beyond  $V_{peak}$ , however, the device current starts to decrease because the electron trapping into the deep traps becomes sufficiently high to give rise to dynamic shift of  $V_{TH}$  of the device due to negative charge trapping. Additionally, the higher rate of scattering between the trapped charges and the channel electrons leads to the mobility degradation of the channel electron. The trapping effect through the shallow interface traps is not significant, however, because the trapping/detrapping process is fast and hence is not supposed to cause a dynamic shift of  $V_{TH}$  for the device. The current continually decreases until  $V_G$  increases to valley voltage ( $V_{valley}$ ) where all traps are filled and trapping no longer occurs. At  $V_G$  above  $V_{valley}$ , electrons are accumulated in the surface channel and their mobility is slightly increased due to the screening effect, as shown in Fig. 5 (a). As a result, the current and transconductance increase again. On the other hand, the NT characteristics are not observed from the device with hexagonal pillar with m-plane sidewall surface and width  $d_{NW}$  of 120 nm, because the trapping occurs mostly through relatively shallower interface traps rather than deep traps.

To further analyze the NT characteristics observed in the devices with  $d_{NW}$  of 75 and 45 nm, the emission time constants were evaluated from the time response of transfer characteristics [22], as shown in Fig. 4. In this measurement,  $V_G$  is swept from 0 V to 3.0 V to fill electrons into the interface traps on the sidewall of nanowire. After a standby time (at off-state condition), the sweeping of  $V_G$  is repeated again to observe the shift of  $V_{FB}$  ( $\Delta V_{FB}$ ) due to electron capture into the interface traps. It is noticed that the  $\Delta V_{FB}$  for the device with  $d_{NW}$  of 120 nm is much smaller compared to that of the narrower devices, as shown in (a) and (b) of the figure. Fig. 4 (c) presents the  $\Delta V_{FB}$  vs. standby time for both devices, which clearly show exponential time decay. The charge variation ( $\Delta N_{dt}$ ) due to the trapping into the deep traps can be expressed as

$$\Delta N_{dt} = \frac{C_{ox}(\Delta V_{FB})}{q} \propto A \exp\left(\frac{-t}{\tau}\right) \quad (1)$$

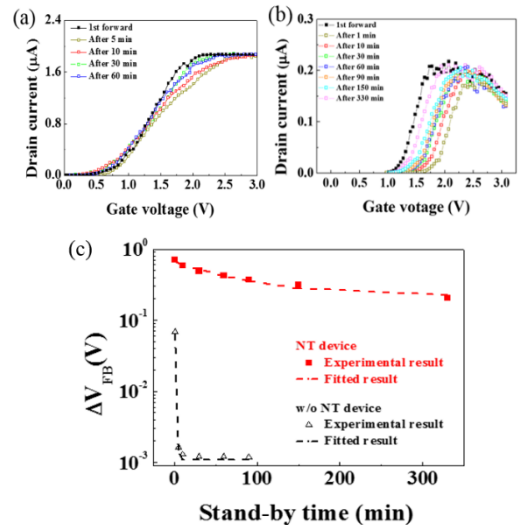
, where  $q$  is the elementary charge,  $C_{ox}$  is the unit area gate dielectric capacitance,  $A$  is a constant,  $t$  is the standby time, and  $\tau$  is the emission time constant of electron de-trapping process, respectively. The emission time constants estimated from the equation above is  $< \sim 0.6$  sec and  $> \sim 500$  sec for the devices with  $d_{NW}$  of 120 and 75 nm, respectively. This clearly

indicates that the trapping/detrapping process in the wide device is mainly due to the trapping/detrapping through shallow interface traps, whereas the trapping in the device with  $d_{NW}$  of 75 nm



**Figure 3** Transfer characteristics of GaN VNW-MOSFET with diameter of (a) 120 nm, (b) 75 nm, and (c) 45 nm.

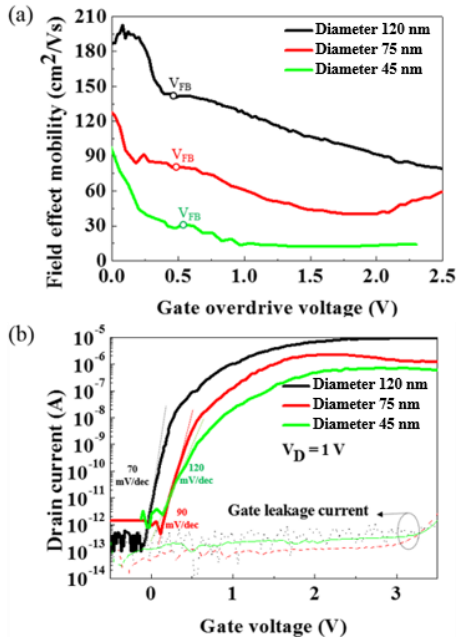
occurs mostly through deep traps. This trapping behavior through deep interface traps in the devices with  $d_{NW}$  of 75 nm is causes the dynamic shift of  $V_{TH}$  which leads to the NT characteristics discussed in Fig. 3.



**Figure 4** Transfer characteristics of GaN VNW-MOSFET with diameter of (a) 120 nm and (b) 75 nm after various standby times. (c)  $\Delta V_{FB}$  versus standby time of same VNW-MOSFETs.

Fig. 5 (a) shows the field-effect mobility versus gate overdrive voltage ( $V_G - V_{TH}$ ) for the investigated GaN VNW-MOSFETs [15], exhibiting the mobility decrease as  $d_{NW}$  narrows. When  $V_G$  is less than  $V_{FB}$ , the channel current consists of electron flow through the nanowire volume where the mobility is superior. At  $V_G$  higher than  $V_{FB}$ , the surface accumulation channel current starts to flow and increases the device current, but the mobility is degraded by additional scattering with the trapped charges at the surface. However, the mobility of the device with  $d_{NW}$  of 70 nm tends to slightly increase as the gate overdrive voltage increases above 2 V, which corresponds to ( $V_G > V_{valley}$ ), whereas the mobility of the device with  $d_{NW}$  of 45 nm becomes saturated at gate overdrive voltage higher than 1 V. The reason is that the strong electron accumulation at surface channel screens the electric field from the charges in interface traps.

On the other hand, the screening effect is hardly observed in the device with  $d_{NW}$  of 120 nm, because the trapping into the interface trap is not significant.

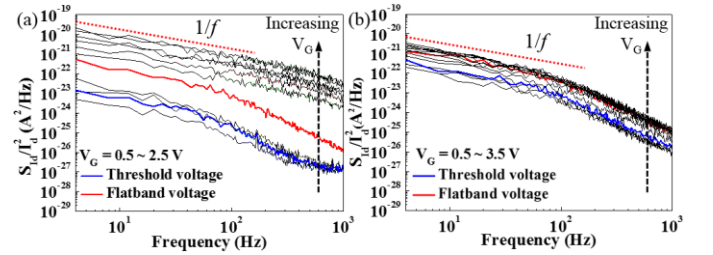


**Figure 5** (a) Field-effect mobility versus gate voltage overdrive and (b) subthreshold characteristics of investigated devices.

Fig. 5 (b) shows the semi-logarithmic transfer characteristics of all investigated devices. The device with  $d_{NW}$  of 120 nm exhibits excellent off-state performances, such as extremely small leakage current of  $\sim 10^{-13}$  A and very low subthreshold swing (SS) of  $\sim 70$  mV/dec with high on/off current ratio of  $\sim 10^8$ . This is the benefit of smooth m-plane sidewall surfaces and hence lower interface trap density. In contrast, the performances are degraded for the devices with smaller  $d_{NW}$ , which suffer from much higher interface trap density ( $D_{it}$ ) caused by the sidewall formation with different crystal planes rather than m-plane only. The  $D_{it}$  extracted from the SS values are  $8.3 \times 10^{11}$ ,  $2.5 \times 10^{12}$ , and  $5.0 \times 10^{12}/\text{cm}^2 \cdot \text{eV}$  for the devices with  $d_{NW}$  of 120, 75, and 45 nm, respectively, which clearly indicates that the m-plane surface has much

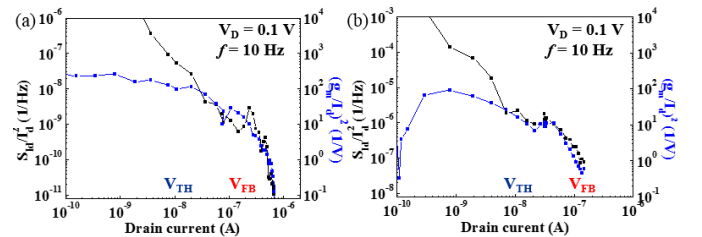
lower interface trap density. The corresponding values for the drain-induced barrier lowering (DIBL) are 120, 50, and 100 mV/V, respectively (data are not shown), which confirm that the device with smaller  $d_{NW}$  is less affected by short-channel effect due to the enhanced gate controllability. Finally, the gate leakage current remains small even at  $V_G$  of 3 V, due to the good dielectric properties of the  $\text{Al}_2\text{O}_3$  gate insulator.

Low-frequency noise measurements were performed to further analyze the characteristics of GaN VNW-MOSFETs. Fig. 6 (a) and (b) show the noise spectral density ( $S_{Id}$ ) versus frequency for the device with  $d_{NW}$  of 120 and 75 nm, respectively. The results for the device with  $d_{NW} = 45$  nm were similar to those obtained from the device with 75 nm. When  $V_G$  is higher than  $V_{FB}$ , both devices show  $1/f$  noise characteristics at low frequencies (below 100 Hz), which indicates that the noise originates from mobility fluctuations or carrier number fluctuations due to trapping/detrapping in defects located at the interface between the gate dielectric layer and the surface of the GaN nanowire channel. The deviation from  $1/f$  noise above 100 Hz in many spectra is related to the measurement bandwidth which, for  $I_d < 1$  nA, is limited at 5-100 Hz. Therefore, this behavior is not attributed to Lorentzian noise related to generation-recombination events.



**Figure 6** Noise spectral density of GaN VNW-MOSFETs with diameter of (a) 120 nm and (b) 75 nm.

Fig. 7 shows the  $(g_m/I_d)^2$  characteristics and the normalized noise spectral density ( $S_{Id}/I_d^2$ ) measured at 10 Hz. When  $V_G$  is higher than  $V_{TH}$ ,  $S_{Id}/I_d^2$  and  $(g_m/I_d)^2$  well match each other for both devices, as shown in (a) and (b) of the figure, which proves that the noise mechanism is related to carrier number fluctuations (CNF), originating caused by electron trapping/de-trapping between the channel and the traps near the gate dielectric [23-25], and not to mobility fluctuations.

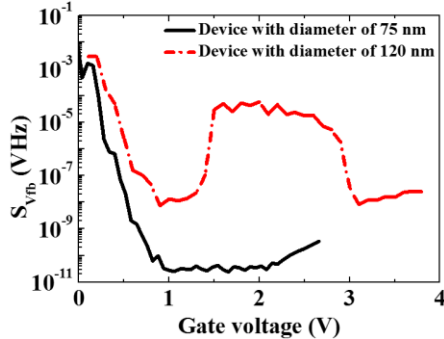


**Figure 7** Normalized noise spectral density ( $S_{Id}/I_d^2$ ) and  $(g_m/I_d)^2$  versus drain current of GaN VNW-MOSFETs with diameter of (a) 120 nm and (b) 75 nm.

Using the CNF model (2), we were able to extract the volumetric oxide trap density,  $N_t$ , for all measured devices. The results are presented in Fig. 8 .

$$\frac{S_{Id}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{Vfb} \quad (2. a), \quad S_{Vfb} = \frac{q^2 \lambda k T N_t}{W L C_{ox}^2 f} \quad (2. b)$$

As one can observe in Fig. 8, where the extraction results are presented,  $N_t$  seems to increase in devices with smaller diameter, which is in agreement with the  $D_{it}$  extraction and probably related to the presence of various crystal planes as already mentioned.



**Figure 8** The input referred gate noise spectral density versus gate bias in GaN VNW-MOSFETs with diameter of 120 and 75 nm.

#### IV. CONCLUSION

GaN VNW-MOSFETs have been fabricated and characterized. The device with m-plane sidewall ( $d_{NW} = 120$  nm) has relatively lower interface trap density and hence shows a normal low voltage operation with  $V_{TH}$  of 0.7 V, drain saturation voltage of 0.5 V, and SS of 70 mV/decade. The field-effect mobility ( $\sim 200$   $\text{cm}^2/\text{Vs}$  at very low  $V_G$ ) is rapidly degraded when  $V_G < V_{FB}$ , and then decreases slowly to  $\sim 90$   $\text{cm}^2/\text{Vs}$  for  $V_G > V_{FB}$ . However, the devices with multiple sidewall planes ( $d_{NW}$  of 75 and 45 nm) show higher  $V_{TH}$  of 0.9 and 1.2 V and  $V_{FB}$  of 1.4 and 1.7 V, and relatively large SS of 90 and 120 mV/decade, respectively. The field-effect mobility for both devices are much lower than for the device with  $d_{NW}$  of 120 nm. Furthermore, the narrow nanowires exhibit two peculiar characteristics such as second rise of drain current in output characteristics and negative transconductance, which are strongly related to the higher contact potential near the drain and higher deep trap density at sidewall surface. The high density of deep traps causes the threshold voltage shift and mobility degradation of the channel electron which leads to negative transconductance. The results obtained in this work suggest that the contact potential must be lowered at drain access region of the nanowire, via heavy  $n^+$ -type doping, while maintaining m-plane sidewalls of the nanowire channel for low interface trap density.

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