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Effect of Gate Structure on the Performance of GaN Junctionless FinFETs

Ki-Sik Im, Sung Jin An, Christoforos G. Theodorou, Gérard Ghibaudo, *Fellow, IEEE*, Sorin Cristoloveanu, *Fellow, IEEE*, and Jung-Hee Lee, *Senior Member, IEEE*

Abstract—We investigated the performances of GaN junctionless nanochannel fin-shaped field-effect transistors (FinFETs) with two different types of gate structures; overlapped- and partially covered-gate. DC, low-frequency noise (LFN), and pulsed I-V characterization measurements were performed and analyzed together in order to identify the conduction mechanism and examine both the interface and buffer traps in the devices. The fabricated GaN junctionless device with overlapped gate structure exhibits improved DC and noise performance compared to the device with partially covered-gate, even though its gate length is much larger. The LFN behavior was found to be dominated by carrier number fluctuations (CNF). At off-state, the device with partially covered-gate exhibits generation-recombination (g-r) noise on top of $1/f$ noise. This superposition is correlated with the severe current collapse revealed by pulsed I-V measurements. In contrast, the device with overlapped gate shows clear $1/f$ behavior without g-r noise.

Index Terms— GaN, Junctionless, Nanochannel, FinFET, Low-frequency noise, generation-recombination noise, Current collapse.

I. Introduction

Highly-doped Gallium nitride (GaN) nanochannel fin-shaped field-effect transistor (FinFET) without AlGaIn/GaN heterojunction was initially proposed and demonstrated by our groups [1]-[2]. The conduction mechanism of this transistor is governed by the bulk current flowing through the inside of the heavily-doped GaN nanochannel arrays, which is totally different from the two-dimensional electron gas (2-DEG) channel in AlGaIn/GaN

heterojunction FinFETs. The GaN junctionless device exhibited outstanding device performances (high I_{on}/I_{off} ratio, excellent subthreshold swing, and large breakdown voltage), added to its simple epitaxial growth and fabrication process [1]-[2]. The fully gate-covered nanochannel structure has been adapted to GaN-based FinFET, omega FinFET, and gate-all-around (GAA) FET because this architecture provides superior device performances, such as improved on-current and reduced current collapse owing to decreased access resistance and less back-gating effect [2]-[6].

Generally, GaN contains a large density of defects, impurities, and dislocations due to the lack of native substrate material. These defects can behave as charge trapping centers, which gradually degrade the device performance and give rise to severe reliability concerns. Low frequency noise (LFN) measurements have great merits in analyzing the interface and/or oxide traps [7] and can also help identifying the conduction mechanism in semiconductor devices. There have been many studies dedicated to LFN for AlGaIn/GaN MISHEMTs, AlGaIn/GaN FinFETs, AlGaIn/GaN omega FETs, AlInGaIn/GaN Fin-HEMTs, and GAA FETs with/without AlGaIn/GaN heterojunction [8]-[11]. It is generally admitted that the origin of the noise mechanism in most of GaN-based 3-dimensional (3D) devices is mainly due to the carrier number fluctuations (CNF) [7]. However, no detailed noise investigation has been conducted regarding the conduction mechanism of GaN junctionless FinFET. In this work, we characterize novel GaN junctionless FinFETs with two different types of gate structures, overlapped- and partially covered-gate, by considering DC, LFN, and pulsed I-V measurements.

II. EPITAXY GROWTH AND DEVICE FABRICATION

The heavily-doped GaN layer was simply grown on a sapphire (0001) substrate by metal organic chemical vapor deposition (MOCVD). The epitaxial layers consist of 2 μm -thick highly-resistive undoped GaN buffer layer and 150 nm-thick Si-doped n-type GaN layer which were sequentially grown on sapphire substrate. Hall effect measurements at room temperature showed a carrier density of $1 \times 10^{18} \text{ cm}^{-3}$, an electron mobility of $280 \text{ cm}^2/\text{V}\cdot\text{s}$, and a sheet resistance (R_{sh}) of $1490 \Omega/\text{sq}$.

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For the device fabrication, mesa etching for device isolation was performed using inductively coupled plasma-reactive ion etching (ICP-RIE) using a Cl_2 gas. After depositing a 20 nm-thick HfO_2 and 100 nm-thick SiO_2 hard mask layer, a fin pattern with fin width (W_{fin}) of 100 nm along $\langle 11\text{-}20 \rangle$ direction was defined by electron-beam lithography (EBL) and etched by ICP-RIE. A tetramethyl ammonium hydroxide (TMAH) wet solution (5% solution at 90 °C) was applied to decrease the slope and size of the fin and to reduce the plasma damage and surface roughness [4], [12], which resulted in 36 parallel fin arrays with width (W_{fin}) of 50 nm, height (H_{fin}) of 200 nm, and length (L_{fin}) of 2 μm . Si/Ti/Al/Ni/Au stack for ohmic contacts was then deposited by electron-beam evaporator, followed by rapid thermal annealing (RTA). Finally, Ni gate metal was deposited to form the gate length (L_g) of 0.5 μm and 2 μm for the partially covered- and the overlapped-device, respectively. It is noticed that L_g of the FinFET with overlapped-gate structure is not the length of the gate metal, but rather corresponds to the L_{fin} of the device. The device structure is illustrated in Fig. 1.

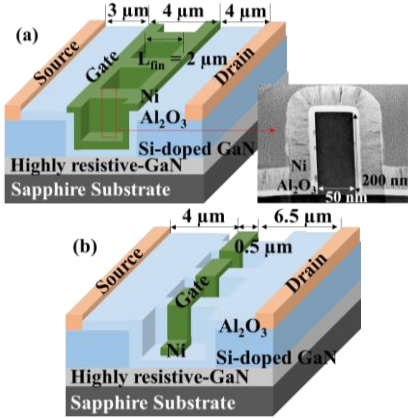


Fig. 1. Schematic illustration of the proposed GaN junctionless FinFETs (a) overlapped- and (b) partially covered-gate structure. Inset of Fig. 1(a) shows cross-sectional TEM image of the perfectly rectangular GaN nanochannel fin.

III. CHARACTERIZATION RESULTS AND DISCUSSION

Fig. 2 shows the drain current, transfer, and output curves of the fabricated GaN junctionless nanochannel FinFETs. Both devices show similar characteristics, such as a threshold voltage, V_{th} , around -0.5 V, $I_{\text{on}}/I_{\text{off}}$ ratio of 10^5 , subthreshold swing of 110 mV/dec, broadened transconductance g_m , and low saturation voltage of ~ 3 V. The reason for the negative V_{th} is the uncompleted depletion in off-state of the heavily-doped GaN fin channel with width of 50 nm. The broad g_m curves that extend to a gate voltage (V_g) of 1.5 V indicate the improvement of the device linearity due to (i) the current contribution of surface accumulation channel formed at higher V_g in addition to the channel current through the fin body and (ii) the small dynamic access resistance of the FinFETs [6], [13]. From the hysteresis under the double sweep of the V_g in Fig. 2(a), it is clearly observed that the partially covered-device suffers from the severe trapping effect with high hysteresis of 220 mV when compared to the value of 40 mV for the overlapped-device. The maximum drain current ($I_{\text{d,max}}$) and maximum transconductance ($g_{\text{m,max}}$) are however different. The device with partially

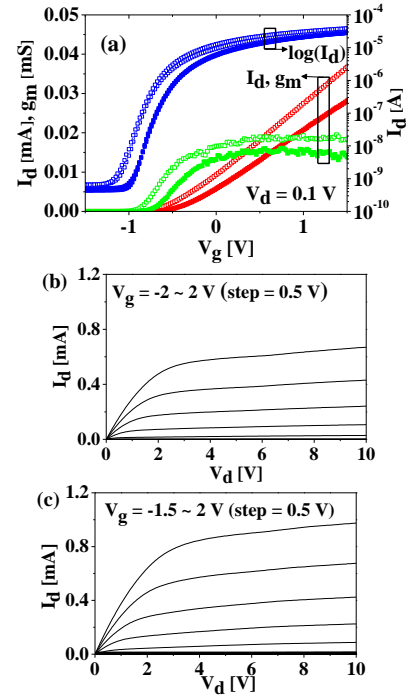


Fig. 2. (a) Transfer curves (double sweep of gate voltage) of the fabricated GaN junctionless FinFETs with overlapped- (filled rectangular) and partially covered-gate (empty rectangular) structure at $V_d = 0.1$ V. Corresponding $I_d - V_d$ curves for devices with (b) overlapped- and (c) partially covered-gate structure.

covered-gate is shorter ($L_g = 0.5$ μm) and exhibits higher $I_{\text{d,max}}$ and $g_{\text{m,max}}$ values than those of the device with the overlapped-gate and L_g of 2 μm . Even though the L_g for the device with partially covered-gate is 4-times shorter than the device with the overlapped-gate, the $I_{\text{d,max}}$ for the partially covered-device exhibits only 1.4-times higher value than that of the overlapped-device due to the larger access resistance (Fig. 2(b) and Fig. 2(c)).

LFN measurements were performed at room temperature, varying the gate bias from subthreshold to strong accumulation region in the linear region at $V_d = 0.1$ V. A fully automatic LFN measurement system from Synergie Concept is used in the frequency ranges from 4 Hz to 10^7 Hz [13]. The drain current noise spectral densities (S_{I_d}) in Fig. 3(a) show $1/f'$ shape with γ close to 1 in the entire frequency bandwidth. Regardless of the gate structure, both devices exhibit almost identical drain current noise level S_{I_d} at $I_d = 0.02$ mA.

According to the CNF model, LFN originates from trapping-related fluctuations in free carrier concentration, which is mostly ascribed to the trapping/detrapping of free carriers between the interface traps and the surface channel. The CNF equation can be expressed as follows, showing S_{I_d}/I_d^2 is proportional to $(g_m/I_d)^2$ [7], [15],

$$\frac{S_{I_d}}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \text{ with } S_{V_{fb}} = \frac{q^2 kT \lambda N_t}{W L C_{ox}^2 f} \quad (1)$$

where C_{ox} is the gate dielectric capacitance per unit area, q is the electron charge, kT is the thermal energy, λ is the oxide tunneling attenuation distance, N_t is the volumetric oxide trap density, WL is the channel area, and f is frequency. On the other hand, the Hooge mobility fluctuations (HMF) model, which is more suitable for explaining the conduction mechanism in the volume of devices [16]-[19], suggests that S_{I_d}/I_d^2 is proportional to $1/I_d$ [15]. However, S_{I_d}/I_d^2 of the devices

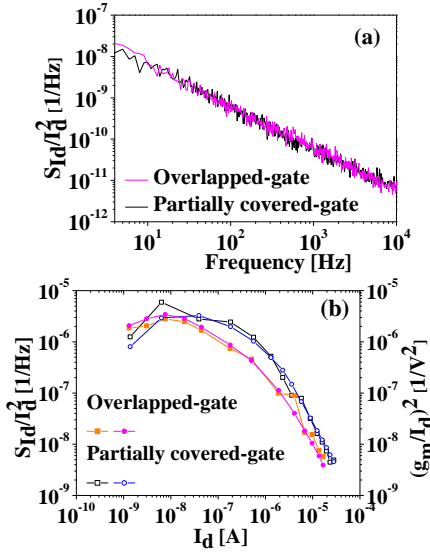


Fig. 3. (a) Normalized noise spectral density (S_{id}) as a function of frequency and (b) normalized S_{id} (left scale) matching with $(\text{constant} \times (g_m/I_d)^2)$ (right scale) versus I_d at $V_d = 0.1$ V and $f = 10$ Hz for the overlap and overlap-free GaN junctionless devices.

investigated in this work is well proportional to $(g_m/I_d)^2$, as shown in Fig. 3, which indicates that the noise of the GaN junctionless FinFETs is dominated by CNF rather than HMF, even though the channel in the fin body is separated from the $\text{Al}_2\text{O}_3/\text{GaN}$ interface by the depletion region. This noise characteristic is consistent with the observed results in Si junctionless FinFETs [17]-[19]. In these works, it was shown that the diffusion through the depletion region or direct tunneling from the bulk neutral region to the interface results in the flat-band voltage fluctuations [18]-[19].

When matching S_{id}/I_d^2 and $(g_m/I_d)^2$, the flatband voltage fluctuations ($S_{V_{fb}}$) are obtained to be $1 \times 10^{-8} \text{ V}^2 \cdot \text{Hz}^{-1}$ and $4.5 \times 10^{-9} \text{ V}^2 \cdot \text{Hz}^{-1}$ for the partially covered- and the overlapped-devices, respectively. Considering the actual gate length for the overlapped-device is $L_{\text{fin}} = 2 \mu\text{m}$, the corresponding trap density (N_t) calculated using Equation (1) with $\lambda = 0.11 \text{ nm}$ is $2.1 \times 10^{20} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ and $2.2 \times 10^{20} \text{ cm}^{-3} \cdot \text{eV}^{-1}$ [20], lower than the values reported from the GaN-based 3D devices [8]-[11]. This result suggests that the trap density of the GaN junctionless device is lower than the interface trap density in devices with surface channel.

Fig. 4 shows $S_{id} \times f$ as a function of frequency at off-state ($V_g = -1$ V) for variable V_d from 0.1 V to 5.0 V. No spectral deformation is observed for the overlapped-device, which reflects that there is no generation-recombination (g-r) noise component because the noise well follows a $1/f$ behavior, even though the active channel of the devices becomes fully depleted at off-state. However, for the partially covered-device, the product $S_{id} \times f$ clearly presents two noise components: one is $1/f$ and the other is g-r noise, described through the following equation [21].

$$S_{if} = K_f + \sum_{i=0}^N \frac{A_i f}{1 + \left(\frac{f}{f_{oi}}\right)^2} \text{ with } \tau_i = \frac{1}{2\pi f_{oi}} \quad (2)$$

where the first term explains the $1/f$ noise component with coefficient of K_f and the second term is the sum of g-r noise components including the plateau value of A_i , the cutoff frequency f_{oi} , and τ_i is the trap time constant. $S_{id} \times f$ for the

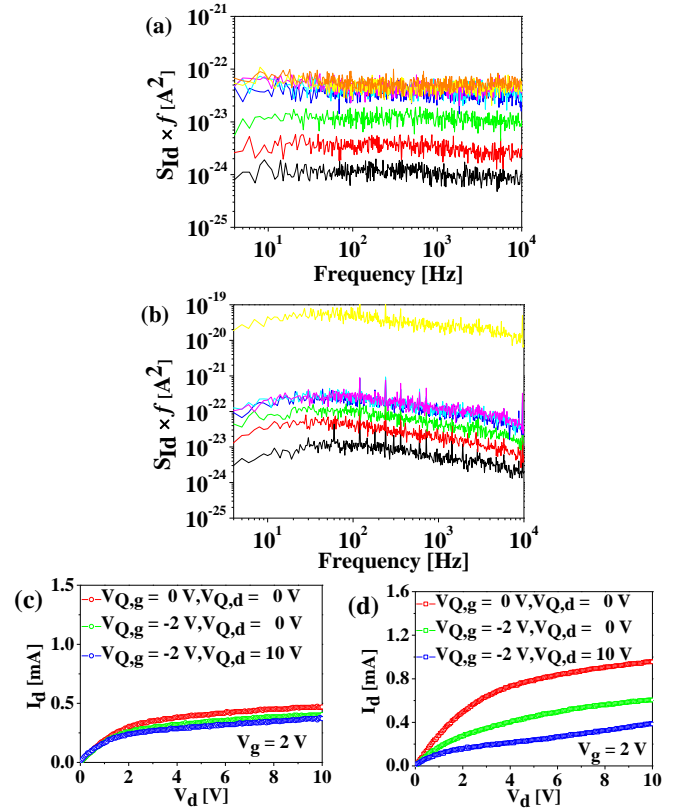


Fig. 4. Product $S_{id} \times$ frequency versus frequency in the fabricated GaN junctionless devices with (a) overlapped- and (b) partially covered-gate structure at $V_g = -1$ V with V_d varied from 0.1 V to 5 V. Pulsed $I_d - V_d$ curves for the devices with (c) overlapped- and (d) partially covered-gate structure at $V_g = 2$ V sweeping $V_d = 0 \sim 10$ V.

partially covered-device (Fig. 4(b)) dramatically decreases at approximately cutoff frequency (f_{oi}) of 30 ~ 40 Hz due to the existence of g-r noise component, which indicates that the device has larger trap time constant in GaN buffer layer than that of the overlapped-device. In the overlapped-device buffer trapping is effectively reduced.

To further examine the buffer trapping effect observed from noise experiments, pulsed I-V measurements for both devices were conducted using Keysight B1500 semiconductor device analyzer with pulse width of 1 ms, as shown in Fig. 4(c) and (d). The pulse conditions are three quasi-bias of (1) $V_{g,Q} = V_{d,Q} = 0$ V, (2) $V_{g,Q} = -2$ V, $V_{d,Q} = 0$ V, and (3) $V_{g,Q} = -2$ V, $V_{d,Q} = 10$ V. The drain voltage is swept from 0 to 10 V at $V_g = 2$ V. The partially covered-device exhibits relatively large current collapse for all pulse conditions. The reason for this large current collapse is the wider effective trapping region, the ungated region between the gate and the drain electrode as shown in Fig. 1 [3], which includes the planar region between the gate and the drain, as well as the uncovered neutral fin array region which is not fully depleted. On the other hand, the overlapped-device shows much smaller current collapse, probably due to the reduced electric field at the gate edge caused by the overlapped gate structure along with smaller trapping region. The results obtained from the pulsed I-V characteristics of the GaN junctionless devices well match with the g-r noise performances at off-state.

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