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Comparative experimental study of junctionless and inversion-mode nanowire transistors for analog applications

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Abstract— We fabricated JunctionLess (JL) and Inversion-Mode (IM) monocrystalline nanowire NMOSFETs down to $L=18\text{nm}$ gate length and $W=20\text{nm}$ width. We demonstrate record performance of nanowire junctionless transistors for analog applications: $A_{VT}=1.4\text{mV}\cdot\mu\text{m}$ matching, $A_{V0}=62\text{dB}$ gain ($L=200\text{nm}$), $f_T=126\text{GHz}$ cut-off frequency and $f_{MAX}=182\text{GHz}$ maximum operating frequency. Junctionless transistor performances even exceed those of IM-FETs in terms of back-bias capability, low-frequency noise, hot-carrier degradation and f_{MAX} . This is explained by JL physics combining characterization and TCAD simulations: channel length modulation, bulk conduction and high channel depth sensitivity to back bias.

I. INTRODUCTION

Recent years have seen renewed interest for JL CMOS transistors because of the relative simplicity of its process integration and its potential fabrication at low temperature as a Back-End-Of-Line transistor for a 3D-sequential integration [1]. On the one hand, polycrystalline silicon or germanium channels, whose doping is activated by a laser anneal, are a promising solution for low-cost and extremely-low-temperature fabrication [2, 3]. On the other hand, monocrystalline Si junctionless channels have already been demonstrated on either planar Silicon-On-Insulator (SOI) [4], FinFET [5] or nanowire architectures [6,7]. Furthermore, JL devices are attractive for analog applications since they are less prone to Hot Carrier Injection (HCI).

II. DEVICE PROCESS FLOW

We fabricated IM and JL nanowire nMOS down to $W=20\text{nm}$ channel width and $L=18\text{nm}$ gate length. The channel thickness is 11nm . The junctionless devices are made by epitaxially growing a 7nm thick *in-situ* phosphorous (P) doped Si film on a 4nm undoped SOI layer. Excellent crystalline quality is obtained (Fig.1). After full process integration the final channel doping level is uniform and equal to $10^{19}\text{at}/\text{cm}^3$. Such channel doping and thickness are optimized for planar devices. The fabrication process is outlined in Fig.2. All the devices feature the same gate stack with HfO_2 dielectrics (equivalent oxide thickness $EOT=1\text{nm}$), TiN + poly-Si and identical 8nm thick spacer.

In order to assess the impact of the channel doping and the source/drain resistance, we added the same 17nm thick Raised Source/Drain (RSD) and HDD+LDD doping processes for so-called Junctionless Accumulation Mode (JAM) transistors as for the IM reference (final anneal at 1050°C). Purely Junctionless transistors (named JL) have also been fabricated without doping under the spacer. Instead, a 5keV P implantation in the 17nm thick RSD followed by a Solid Phase Epitaxy Regrowth (SPER) annealing at 525°C 30 min was carried out, in order to only dope the JL-RSD (see Kinetic Monte-Carlo profile on Fig.2) and avoid lateral doping diffusion. This process module is suitable for a 525°C 3D-sequential integration process [8].

III. DEVICE ELECTRICAL CHARACTERIZATION

Digital $I_{ON}-I_{OFF}$ figure of merit (Fig 3) show no significant difference between JAM and IM FET. Also, similar parasitic gate to SD capacitance C_{GDS} suggests a similar direct overlap controlled by the SD implant (Fig. 4). On the other hand, the JL FET has a $0.06\text{fF}/\mu\text{m}$ lower C_{GDS} vs JAM/IM, which cannot be explained by the fringe components but rather by a depletion region extending below the spacers in JL transistors (Fig.5). Nevertheless JL devices suffers from higher access resistance (R_0) due to non-optimized junctions (Fig 3).

Local variability: matching coefficient A_{VT} is higher for JL/JAM devices than IM ($1.7/1.4$ vs. $1.0\text{mV}\cdot\mu\text{m}$, Fig. 6). This degradation with the channel doping is attributed to Random Dopant Fluctuation [9].

Analog: we consider a nominal transistor width of $W=0.24\mu\text{m}$, (planar SOI configuration instead of a trigate nanowire structure). The JL/JAM subthreshold slope (SS) is $SS=64\text{mV}/\text{dec}$ vs. $61\text{mV}/\text{dec}$ for the IM device (Fig. 7). However, **back-bias** can be leveraged in order to adjust the threshold voltage and tune performance [10]. Indeed, back-bias is more effective for wider than for narrower devices and it is more effective on JL/JAM than on IM transistors (Fig.8). Markedly, a negative back-bias applied on JAM moves the bulk conduction channel upwards towards the gate, which results in an improvement of the electrostatic control (SS, g_d) and, therefore, improving g_m/I_d and g_m/g_d , as well as the Early voltage (V_{EA}) (Figs 9-10). As a result, JAM FETs reach analog performances that are slightly better than IM devices, up to an $A_{v0}=68\text{dB}$ gain.

Reliability: we have performed Positive Bias Temperature Instability (PBTI) and Hot Carrier Injection (HCI) (Figs. 11-12). We demonstrate similar PBTI (88 years lifetime at $V_{DD}=0.8\text{V}$) and even better HCI for JL as compared to IM. It can be explain by a lower and shifted to the drain (not underneath the gate dielectric as for IM/JAM) peak electric field.

Low-frequency drain current noise measurements (Fig.13) show a 31-die average $1/f$ signature and a slightly lower input-referred gate voltage noise level (S_{Vg}) for JAM. Using the Carrier number fluctuations with Correlated Mobility Fluctuations model [11] and taking into account the series resistance noise (S_{Rsd}), we fitted the normalized drain current noise at $f=10\text{Hz}$ (Fig.28) to extract the volumetric oxide effective trap density N_T , and the remote Coulomb scattering coefficient α_{sc} for all wafers. We extracted a value of $N_T \approx 7.5 \cdot 10^{17}\text{eV}/\text{cm}^3$ for all cases, reflecting a similar interface quality, independently of the conduction mode. This value is also very close to state-of-the-art N_T values of high-k-metal-gate CMOS technologies [12]. Concerning α_{sc} , a very similar value ($\approx 4 \times 10^3\text{Vs}/\text{C}$) is extracted for all wafers, showing that the remote Coulomb scattering is not affected by the different conduction modes. Finally, S_{Rsd} has a significant impact only for JL, which can be linked to non-optimized source/drain doping [13].

Mobility differences, due to channel doping, are also translated into a cut-off frequency shift, measured at $F_T=130\text{GHz}$ for JAM vs. 136GHz for IM. But JAM exceeds IM devices in terms of F_{MAX} because of lower gate capacitances C_{GDS} . We demonstrate a record $F_{max}=182\text{GHz}$ for JAM nMOS (Fig 15).

IV. CONCLUSION

Finally, our devices feature record performance among junctionless nMOSFETs (Fig.16). Thanks to process technology variants, electrical characterizations and TCAD simulations, we demonstrated that such a technology offers a good tradeoff for mixed analog/digital applications.

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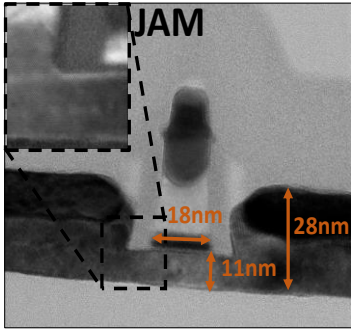


Fig.1: TEM cross section of JAM device. Excellent crystalline quality is observed.

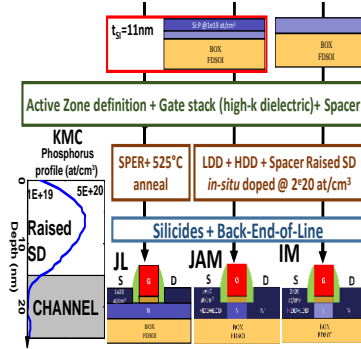


Fig.2: Detailed Process flow for IM (N+-i-N+), JAM (N+-N-N+) and JL (N) devices.

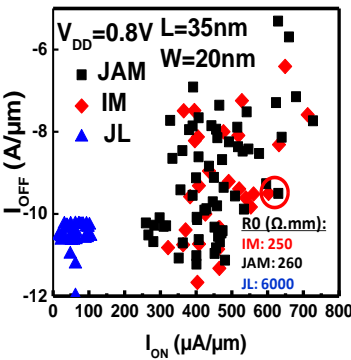


Fig.3: I_{ON} - I_{OFF} for $L=35nm$ and $W=20nm$.

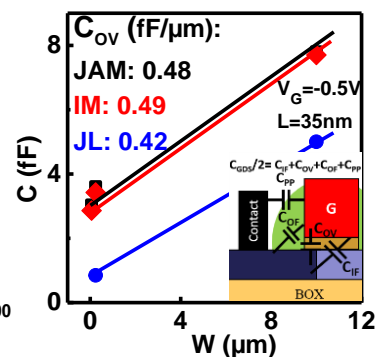


Fig.4: $C(W)$ and C_{GDS} extraction at $L=35nm$. Inset: Schematic with parasitic capacitance contributions.

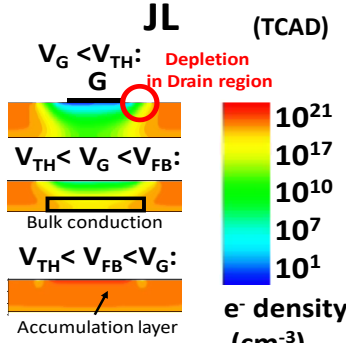


Fig. 5 : Electron density (SD cut) highlighting three operation regimes

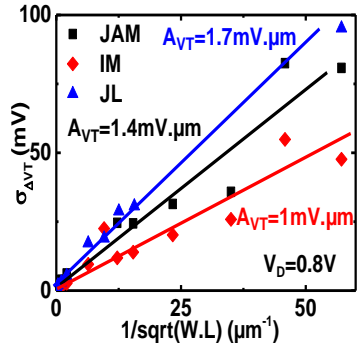


Fig.6: Pelgrom plot (local variability)

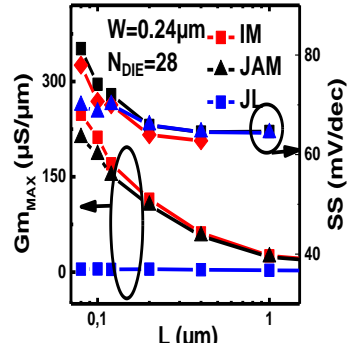


Fig.7: $g_{m,MAX}$ and SS as a function of L for $W=0.24μm$

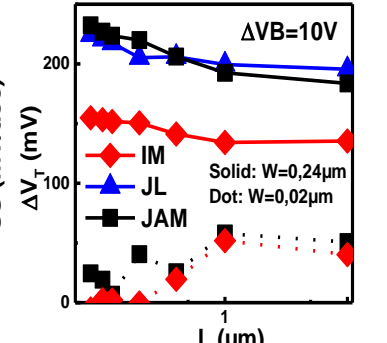


Fig.8: Back bias efficiency for $W=0.02μm$ and $W=0.24μm$.

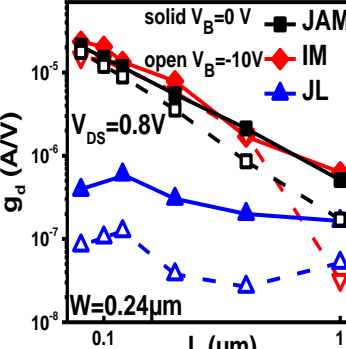


Fig.9: g_d vs. L for $V_B=0$ and $V_B=-10V$. $V_B<0$ improves electrostatics.

Gain A_{v0} (dB)	V_B (V)	$L=100$ nm	$L=200$ nm	$L=400$ nm
IM	0	1	60	50
	-10	18	65	53
JAM	0	1	12	51
	-10	64.5	68.8	55
JL	0	59	47	38
	-10	61.5	65	41

Fig.10: Gain A_{v0} for different Gate length $V_B<0$ improves A_{v0}

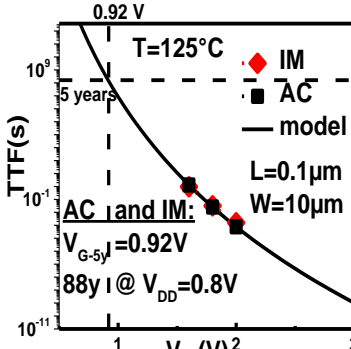


Fig.11: Time-To-Failure for PBTL. The 5-year criterion is met

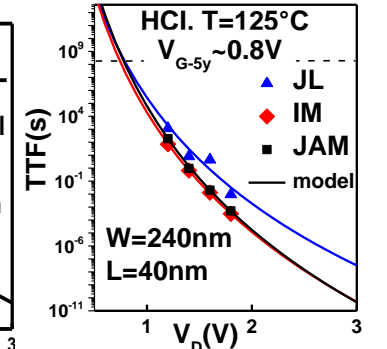


Fig.12: Time-To-Failure for HCl. The 5-year criterion is met.

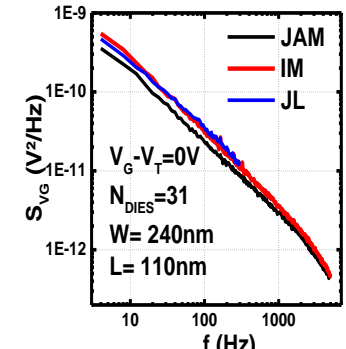


Fig.13: Input-referred gate voltage power spectral density versus frequency

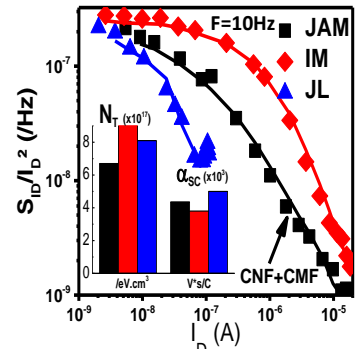


Fig.14: Normalized drain current power spectral density versus I_D . Inset: Extracted values of N_T and α_{sc}

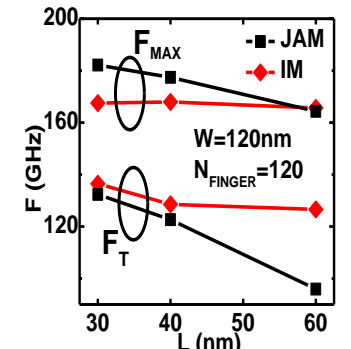


Fig.15: f_{MAX} and f_T comparison for different L .

Ref.	[14]	[6]	This Work
Techno	Low-Temp FDSOI	NW	NW/FDSOI
L_G (nm)	80	48	35
V_{DD} (V)	1.0	1.0	0.8
A_{VT} (mV.μm)	-	4.4	1.4
A_{v0} (dB)	55 for $L=40nm$	45 for $L=80nm$	68 for $L=0.2μm$
f_T (GHz)	80	>70	126
f_{max} (GHz)	117	~90	169

Fig.16: nMOS junctionless benchmark for analog FOM

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