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New Definition of Critical Energy for SiC MOSFET Robustness under Short-Circuit Operations: the Repetitive Critical Energy

C. Chen, T.A. Nguyen, D. Labrousse, S. Lefebvre, C. Buttay, H. Morel

Abstract – Previous research showed that Si devices could sustain a large number of Short Circuit (SC) events, as long as the energy dissipated during SC remains slightly below a given threshold (the so-called critical energy). In this paper, we show that this is not necessarily true for SiC MOSFETs, which can only withstand a few such SC events. This low robustness to repetitive short-circuit events is related to the gate degradation due to the cumulative carrier injection and leakage currents in the oxide. To ensure safe operation over a large number of SC events, we introduce a new parameter: the “repetitive critical energy”, which corresponds to a SC energy low enough to avoid excessive temperature increase so as to limit the transient gate leakage current during SC events. Below this repetitive SC energy value, the SiC device is able to sustain a large number (more than 1000) of SC events.

1. Introduction

As a semiconductor material, SiC has much better physical characteristics than silicon (wider bandgap, higher avalanche critical electrical field, higher thermal conductivity) [1]. Nowadays, power MOSFETs are the most common type of SiC transistors available on the market. Compared to Si devices of the same voltage ratings, SiC MOSFETs offer a lower on-state voltage drop, higher switching speeds and a lower leakage current in the off state. However, it is crucial to characterize the robustness and reliability of power SiC MOSFETs before they can be implemented on a large scale in electrical energy conversion systems. Over the last few years, various studies have investigated the robustness of SiC MOSFETs in the case of short-circuits (SC) and avalanche breakdown.

Thanks to their lower specific resistance [1], SiC dies tend to be smaller than those of comparable Si devices. This results in a higher current density which, together with the high electrical field encountered during SC events, produces a higher density of power dissipation. It should also be mentioned that the active layer of SiC MOSFETs is much thinner than that of silicon devices of the same blocking voltage. These features cause a faster temperature rise of the SiC dies, and a shorter time to failure, especially at high drain to source voltages [2-4] or when the device is turned on with a high gate to source voltage [5]. These different papers have shown that SiC MOSFETs are much weaker than Si devices with similar current and voltage ratings in SC stress.

For low gate to source voltage (10 V) and consequently low saturation current during SC events, the failure mechanisms are characterized by the trapping of positive charges into the gate oxide above the channel region or at the interface. This results in the decrease of the threshold voltage and the increase of the drain leakage current after the SiC MOSFETs have been submitted to repetitive SC events [6].

Under higher gate to source voltages, two different failure modes have been pointed out [7]. The first one is a failure during the SC (or a delayed failure mode) which is due to thermal runaway. In these conditions, experiments show a change in the current slope at the end of the SC pulse for SC durations close to the failure and a current tail after a safe opening of the SC current [8]. The second failure mode involves the degradation of the gate and can result in a SC between gate and source electrodes [9, 10]. Several studies also report the apparition of a gate leakage current during SC events for discrete components and modules [3, 9, 10, 11, 12]. The gate leakage current, which depends strongly on the gate to source and drain to source voltages [11], has been related to the Fowler-Nordheim current which is affected by the temperature [13, 14]. A recent paper points out that Schottky emission is most likely to be the mechanism explaining the large gate current observed in SiC MOSFET during SC operation [15]. It has also been shown that

the repetition of SC events can quickly lead to a gradual increase of the gate leakage current during SC and irreversible degradation [10]. The failure mechanisms have been investigated by several authors, although the results are still controversial. For both failure modes, electro-thermal simulation results show that failure appears at $650\text{ °C} \pm 100\text{ °C}$, i.e. close to the melting temperature of the topside metallization of the dies (aluminum) [16], and much lower than the thermal runaway temperature $>1200\text{ °C}$ for 1200 V 4H-SiC [17]. Another paper shows that the temperature at failure in the crystal is between 1600 and 2000 K, depending of the failure mode (fail to open or fail to short respectively) [18]. Furthermore, even if the gate oxide has been identified to be the weakest part of SiC MOSFETs, micro-structural failure analyses made on commercial devices did not show cracks in the gate oxide but mainly in the field oxide, which nevertheless results in a path between the polysilicon gate and the source terminal [19, 20].

The SC Safe Operating Area (SCSOA) of silicon IGBTs was defined many years ago [21-23], and these components are typically able to withstand the repetition of a high number of SC cycles (typically 1000s) with a duration of less than 10 μs at a voltage equal to half of V_{BR} . Previous studies have highlighted the existence of a critical energy (E_C) which separates two distinct stable failure modes for Si IGBTs. For an energy level below the critical value, devices can withstand a large number of SC cycles before failure. As soon as the SC energy exceeds even so slightly the critical energy, the devices fail at the first SC test in a “delayed failure mode” [23]. A tail current takes place after the turn-off process of the device and leads to a destructive thermal runaway phenomenon after several tens or hundreds of microseconds. This critical energy value is related to the temperature inside the device, which rises to a level where collector leakage current becomes excessive.

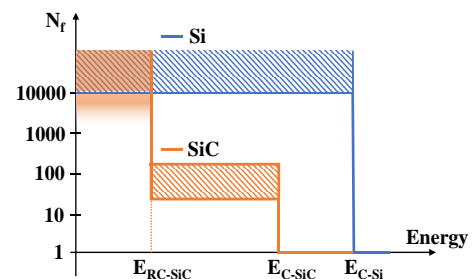


Fig. 1. Repetitive critical energy for evaluating the SC robustness of SiC MOSFETs (E_{RC} : repetitive critical energy, E_C : critical energy, N_f : number of SC events to failure).

In this paper, we investigate the critical energy (E_C) of SiC MOSFETs manufactured by Wolfspeed. The paper will show that contrarily to Si devices, which can survive many SC events providing their energy is slightly lower than the critical energy, SiC MOSFETs can only withstand a few such SC events. The reason of their fast degradation will be related to the gate oxide

degradation due to the repetition of carrier injection in the oxide or to the formation of cracks in the field oxide leading to a conductive path between gate and source terminals. In order to define a Safe Operating Area (SOA) that is valid over a large number of SC events, we introduce a new critical energy parameter: the “repetitive critical energy” (E_{RC}) for SiC MOSFET (see Fig. 1). It corresponds to a SC energy low enough to avoid excessive temperature increase so as to limit the transient gate leakage current during SC events.

2. Experimental protocol

The SC test bench is presented in Fig. 2. 4H-SiC MOSFETs rated at 1.2 kV – 80 mΩ (C2M0080120D, Wolfspeed) were selected as the Devices Under Test (DUTs). The SC test bench allows providing SC stress with a maximum DC voltage of 900 V, a maximum SC current of 400 A and a tunable SC pulse width.

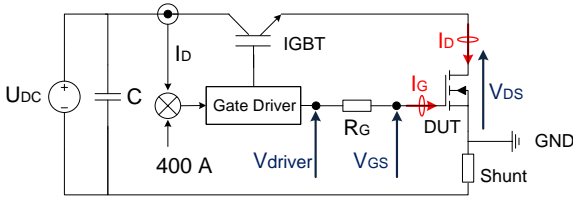


Fig. 2. Short-circuit test bench.

The SC currents are measured using a 10 mΩ coaxial shunt (T&M Research SBNC-2-01) connected in series with the source terminal of the MOSFET, while V_{DS} is measured using a Tektronix P5100A, high-voltage probe (2.5 kV) designed for high frequency (up to 500 MHz). The gate current I_G can be calculated using (1).

$$I_G = \frac{V_{driver} - V_{GS}}{R_G} \quad (1)$$

where V_{driver} is the output gate driver voltage, V_{GS} is the gate-source voltage and R_G is the gate resistance.

V_{driver} and V_{GS} are measured using Tektronix P6139B voltage probes rated at 300 V. The DUT is mounted on a temperature-regulated hot plate that sets its case temperature, to observe the influence of the initial junction temperature (from 25 °C up to 150 °C) on the robustness of the DUT.

The energy dissipated (E_{dis}) inside the DUT is calculated from the V_{DS} and I_D waveforms captured during the SC phase by integrating $V_{DS} \times I_D$ over the duration of the SC pulse t_{SC} :

$$E_{dis} = \int_0^{t_{SC}} V_{DS} \cdot I_D dt \quad (2)$$

The critical energy (E_C) [23], which is an essential metric of robustness for power devices, refers to the minimal amount of dissipated energy that leads to the failure of the tested device after one single SC. With the purpose of estimating this critical energy, the SC duration is gradually increased from a low value (where the device can safely turn-off the SC current) up to the failure point. The maximum energy the device is able to sustain during a safe SC test is recorded as the critical energy. Note that this methodology assumes that the repetition of the SC events has no effect on E_C , i.e. that there is no wear-out mechanism that would cause a progressive degradation of the DUT. As we will demonstrate, this assumption does not necessarily hold true, which is why at first SC duration is increased with coarse steps, so as to limit the number of SC events.

3. Critical energy and junction temperature estimations

A series of SC tests was carried out for the purpose of

critical energy evaluation. In a first step, as a trade-off between the accuracy of E_C estimation and preventing accelerated aging of the DUT, $\Delta t_{SC} = 0.5 \mu s$ has been chosen as a fixed time increment. The tests were performed at $U_{DC} = 600 V$, $T_{CASE} = 25 \text{ }^\circ C$ and 150 °C and $R_G = 47 \Omega$.

The results are plotted in Fig. 3.a and Fig. 4.a, where V_{DS} and V_{GS} are presented on the left scale and V_{GS} is multiplied by 20 to match the V_{DS} scale.

At $T_{CASE} = 25 \text{ }^\circ C$, for $t_{SC} = 8, 8.5$ and 9 μs , the drain current returns to zero after the DUT has turned off. However, for $t_{SC} = 9.5 \mu s$, 4 μs after the turn-off, a delayed failure appears, causing a SC between all three terminals of the device (Fig. 3.a). If we consider $t_{SC} = 9 \mu s$ (the highest value resulting in a safe turn-off), the critical energy E_C can be estimated to about 726 mJ.

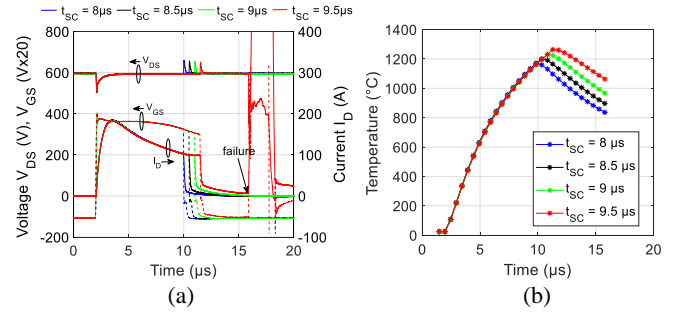


Fig. 3. (a) Estimation of critical energy for $R_G = 47 \Omega$, $U_{DC} = 600 V$ and $T_{CASE} = 25 \text{ }^\circ C$, $E_C = 0.726 J$. (b) Simulation of the corresponding junction temperature (ANSYS Multiphysics).

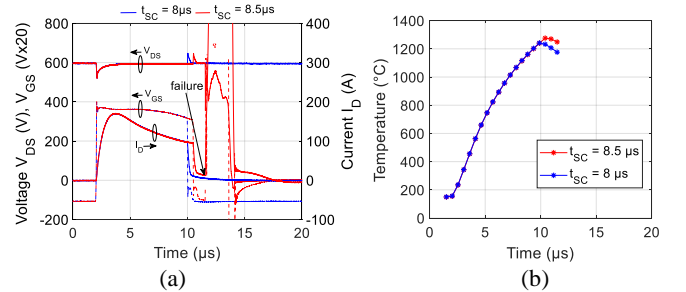


Fig. 4. (a) Estimation of critical energy for $R_G = 47 \Omega$, $U_{DC} = 600 V$ and $T_{CASE} = 150 \text{ }^\circ C$, $E_C = 0.620 J$. (b) Simulation of the corresponding junction temperature (ANSYS Multiphysics).

The same experimental protocol was also performed at $T_{CASE} = 150 \text{ }^\circ C$. As shown in Fig. 4.a, for $t_{SC} = 8 \mu s$, the DUT can safely switch off the SC current. However, a delayed failure appeared for $t_{SC} = 8.5 \mu s$ (about 1.5 μs after the turn-off). A critical energy of about 620 mJ was estimated for $t_{SC} = 8 \mu s$.

In both cases (25 and 150 °C case temperatures), the delay between the end of the SC pulse and the failure may be due to the diffusion of heat inside the DUT that delays the heating up of the most sensitive zones of the device. The lower critical energy observed for a higher T_{CASE} also points towards a thermal effect.

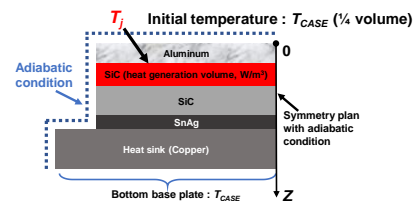


Fig. 5. Simulated power assembly structure.

In this paper, the junction temperature (T_j) during SC cycles was estimated using ANSYS Multiphysics software. As shown in Fig. 5, the simplified simulation structure consists of different layers: Aluminum (4 μm thickness), 4-H SiC (180 μm thickness), solder (50 μm thickness), and heat sink (Copper) layers, whose dimensions and physical parameters were individually adjusted according to the features of DUT. The

thermal conductivity and the specific heat of 4-H SiC have also nonlinear behaviour with the temperature [24-25]. We assumed that the dissipated power is applied over a thin (5 μm thick) SiC layer located just below the metallization layer, and T_J is estimated at the interface between the metallization and the SiC layers (Fig. 5). The experimental power waveforms are supplied to the simulation for the calculation of T_J . Before the failure event, the simulation shows that the maximum T_J can reach 1264 $^\circ\text{C}$ and 1276 $^\circ\text{C}$ in the test of $T_{\text{CASE}} = 25$ $^\circ\text{C}$ (Fig. 3.b) and of $T_{\text{CASE}} = 150$ $^\circ\text{C}$ (Fig. 4.b), respectively. The estimated temperatures should be considered indicative only: very simplified thermal models, which do not consider the non-linearity in all material properties nor the liquefaction of the metallization which should occur. [16, 18, 26].

4. Aging under successive short circuit tests

4.1. Ageing under small-time increment of SC duration

A much smaller time increment Δt_{SC} (~ 100 ns) was then used to determine precisely the critical energy. In these conditions, the device experiences a very large number of SC cycles before failure. We have observed that this repetition of SC events causes the device to wear out. The corresponding experimental results are presented in this section.

The tests were conducted on DUTs for a DC voltage $U_{\text{DC}} = 600$ V and a case temperature $T_{\text{CASE}} = 25$ $^\circ\text{C}$, with a gradual increase of the SC duration from 4.0 to 15.8 μs by steps of 100 ns. The results in Fig. 6 clearly show that the transistor can sustain SC up to 15.7 μs . However, several phenomena occur even before the final destruction of the DUT.

The evolutions of V_{GS} (Fig. 6.a), I_{G} (Fig. 6.b) and I_{D} (Fig. 6.c) can be split up into four stages represented by the four colours of the waveforms. Variations are gradual within a given stage and, by contrast, discontinuous from stage to stage. This stepwise decrease seems to be related to cumulative physical degradations.

The drain current I_{D} is controlled by V_{GS} . We notice that the repetition of SC events results in the sudden occurrence of a large transient gate leakage current $I_{\text{G,tr}}$ (> 200 mA, for a SC duration of 7.8 μs), which then gradually increases, step by step. The increase in the gate leakage current results in the decrease of V_{GS} because of the larger voltage drop across the gate resistance. This lower V_{GS} then explains the step-by-step decrease of the saturation current I_{D} .

The energy dissipated during the first cycle (4 μs of duration) is 0.57 J and increases up to only 0,64 J in the last SC (15.8 μs of duration) after 118 cycles. The increase in the dissipated energy with the SC duration is relatively moderate due to the gradual degradation of the DUT which causes the SC current to decrease as the tests are repeated (see Fig. 6.c).

For the tests where t_{SC} ranges from 4.0 μs to 7.7 μs (in blue), we can observe that the DUT does not exhibit any permanent gate leakage current $I_{\text{G,per}}$ (gate current is zero before and after the SC pulses - before $t = 0$ μs and after $t = 7.7$ μs in Fig. 6.b). But a transient gate leakage current is visible through the decrease in V_{GS} after 4 μs (Fig. 6.a). After switch-off of the SC current, no noticeable gate leakage current can be observed in the off-state despite the negative polarization of the gate (-5 V). This means that the transient gate leakage current $I_{\text{G,tr}}$ is related to a reversible phenomenon such as carrier injection, and not to the breakdown of the gate oxide.

For the stage in red ($t_{\text{SC}} = 7.8$ μs to 11.8 μs) we note a high transient gate leakage current $I_{\text{G,tr}}$ during the SC phase (about 0.4 A of maximum value), but we can also observe that a permanent gate leakage current $I_{\text{G,per}}$ exists after turn-off (about -0.1 A).

This evidence strongly supports the hypothesis of a physical degradation in the DUT, especially at the level of the gate oxide or the field oxide.

In the third and fourth stages ($t_{\text{SC}} = 11.9$ μs to 14.2 μs , green, and $t_{\text{SC}} = 14.3$ μs to 15.7 μs , yellow), the increase in gate leakage current and the decrease in V_{GS} and I_{D} implies a further degradation of the gate oxide or the field oxide. Clear jumps in the gate leakage currents are visible between stages 2, 3 and 4.

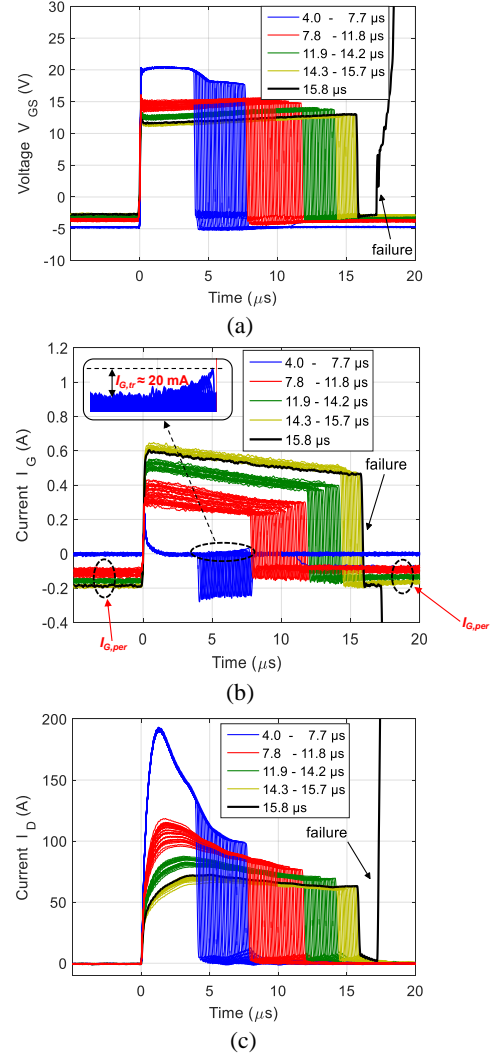


Fig. 6. Ageing under successive short circuits with 100ns increasing duration, $R_{\text{G}} = 10$ Ω , $T_{\text{CASE}} = 25$ $^\circ\text{C}$, $U_{\text{DC}} = 600$ V. (a) V_{GS} . (b) I_{G} . (c) I_{D} .

4.2. Ageing under a fixed repetitive SC duration

To determine a safe energy dissipation (or SC duration) level for repetitive SC, experimental ageing was performed under fixed SC duration. We considered SC energies significantly lower than E_{C} estimated in the section 3. Tests were undertaken with short SC durations (t_{SC}) of 7 μs , 4.4 μs , 4 μs , and 3 μs .

4.2.1. Short circuit cycle with high transient gate leakage current

Experimental ageing results under a fixed repetitive SC duration (7 μs) are presented in Fig. 7 for a dissipated energy significantly lower than the critical energy estimated in Fig. 3.a (critical energy in the same conditions is determined for a SC duration equal to 9 μs). A transient gate leakage current $I_{\text{G,tr}}$ appears at 4 μs after the beginning of SC test for the 1st cycle, and a significant $I_{\text{G,tr}}$ of about 4 mA is observed at the end of this cycle in the magnified I_{G} graph (Fig. 7.b). Permanent leakage current $I_{\text{G,per}}$ appears at the 300th cycle (i.e. negative permanent

gate current before and after the SC test) and becomes more visible for the 330th cycle. The gate leakage current causes a voltage drop in R_G and therefore a reduction in V_{GS} as depicted in Fig. 7.c. As the drain current is controlled by V_{GS} , it also gradually decreases during ageing, especially from the 300th cycle to the 330th cycle. The energy dissipated during the first cycle is 0.57 J and decreases down to 0.5 J in the last SC after 330 cycles due to the reduction in the SC current during ageing. The tests were stopped after 330 cycles due to the very high level of permanent gate leakage current.

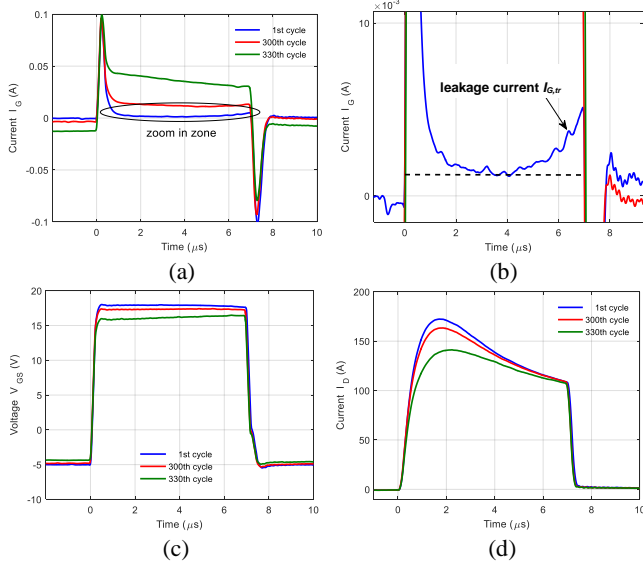


Fig. 7. (a) I_G , (b) Zoom in I_G , (c) V_{GS} and (d) I_D of DUT during repetitive short circuit, with $t_{SC} = 7 \mu s$, $R_G = 47 \Omega$, $T_{CASE} = 25 \text{ }^\circ\text{C}$, $U_{DC} = 600 \text{ V}$.

Table I - Evolution of electrical parameters of DUT under repetitive SC with $t_{SC} = 7 \mu s$, $T_{CASE} = 25 \text{ }^\circ\text{C}$.

Cycle	V_{TH} (V)	I_{GSS}	$R_{DS(on)}$ (m Ω)	I_{DSS} (nA)
0	1.84	<100 fA	86	494
300	1.08	>100 μ A	85	516
330	0.03	>100 μ A	87	777

The static characteristics were measured periodically during the test and the main parameters are presented in Table I. The experimental measurement conditions to obtain V_{TH} , I_{GSS} , $R_{DS(on)}$ and I_{DSS} are detailed in Fig. 11 of Appendix A. A substantial increase in the static gate leakage current I_{GSS} from under 100 fA in initial state to over 100 μ A after 300 cycles is observed. The large increase in the gate leakage current explains the significant decrease of the threshold voltage V_{TH} (cf. Appendix A, Fig. 11.a) from 1.84 V to 1.08 V between the first and the 300th cycle, before collapsing to 0.03 V for the 330th cycle. This confirms the physical degradation of the gate, especially on the gate or field oxides. No change is observed on the on-state resistance, and the increase in drain leakage current is associated with the gate damage.

Because of this strong degradation of the oxide (large gate leakage current and close-to-zero threshold voltage) the DUT is not considered as functional anymore. For this particular test, with a dissipated energy sensibly lower than the critical value, we observe that a very fast degradation of the oxide appears after only 300 SC cycles.

4.2.2. Short circuit cycle with moderate transient gate leakage current

To determine for what energy dissipation or SC duration we can safely consider the repetition of SC cycles, ageing tests were undertaken with a SC duration t_{SC} of 4 μ s. In these conditions,

$I_{G,ir}$ is still noticed from the first cycle in Fig. 8.b, but with a much lower amplitude than for $t_{SC} = 7 \mu s$. It seems that $I_{G,ir}$ appears after about 3.1 μ s of SC duration. The evolutions of V_{GS} , I_G and I_D are similar to what happened for $t_{SC} = 7 \mu s$. During the repetition of the SC cycles, an increase in gate leakage current and a decrease in V_{GS} are noticeable and can be attributed to the degradation of the gate or field oxide of the DUT. We also notice once again the appearance of $I_{G,per}$ under reverse biasing of the gate after once again a low number of SC events (only 300 cycles). I_D drops from 175 A at the first cycle to 150 A at the 378th cycle. The decrease of the saturation current is once again explained by the reduction of the gate to source voltage V_{GS} . The energy dissipated during the first cycle is approximately 0.34 J and decreases to 0.31 J after 330 cycles.

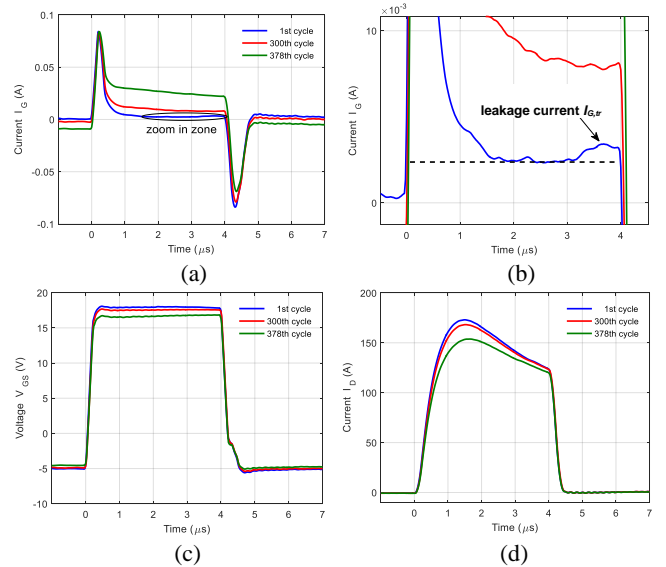


Fig. 8. (a) I_G , (b) Zoom in I_G , (c) V_{GS} and (d) I_D of DUT during repetitive short circuit, with $t_{SC} = 4 \mu s$, $R_G = 47 \Omega$, $T_{CASE} = 25 \text{ }^\circ\text{C}$, $U_{DC} = 600 \text{ V}$.

Table II - Evolution of electrical parameters of DUT under repetitive SC with $t_{SC} = 4 \mu s$, $T_{CASE} = 25 \text{ }^\circ\text{C}$.

Cycle	V_{TH} (V)	I_{GSS}	$R_{DS(on)}$ (m Ω)	I_{DSS} (nA)
0	2.02	<100 fA	68	9.06
300	1.62	>100 μ A	67	10.73
378	0.05	>100 μ A	69	15.53

In Table II, the gate degradation is once again illustrated by the increase in I_{GSS} . I_{GSS} exceeds 100 μ A after the 300th cycle, which can be related to a degradation of the gate or field oxide. A reduction in the threshold voltage happens simultaneously with the increase in the gate leakage current.

Another DUT was tested and aged. The SC duration of 4.4 μ s was adjusted to obtain a similar magnitude of $I_{G,ir}$ (about 2 mA at the end of the SC event) with that measured on the previous DUT (Fig. 8.b). The SC pulse width being different from that observed for the previous DUT shows that the features of the components are not completely identical although they have the same part reference. The static characteristics were more regularly measured on this DUT (Table III). Particularly, in the case of this DUT a great increase of 2.89 nA in I_{GSS} value has been detected after only 10 SC cycles as shown in Table III. I_{GSS} then progressively increased during the aging process from 2.89 nA to 8.01 nA after 100 SC cycles. This I_{GSS} increase seems to be responsible for triggering the failure process of the DUT. Finally, I_{GSS} abruptly increased to about 5.4 mA after 150 cycles. Furthermore, using the simulation model described in section 3, the maximum T_J was estimated to be about 840 $^\circ\text{C}$ during the 1st SC cycle of this DUT.

Table III - Evolution of electrical parameters of DUT under repetitive SC with $t_{SC} = 4.4 \mu\text{s}$, $T_{CASE} = 25^\circ\text{C}$.

Cycle	V_{TH} (V)	I_{GSS}	R_{DSON} (m Ω)	I_{DSS} (nA)
0	1.93	<100 fA	88.4	0.49
10	2.01	2.89 nA	88.2	0.48
20	2.07	4.95 nA	88.2	0.49
30	2.09	5.46 nA	88.3	0.48
50	2.11	6.73 nA	88.4	0.49
100	2.14	8.01 nA	88.8	0.50
150	1.08	5.40 mA	89.5	0.51

The evolution of V_{GS} , I_G and I_D waveforms was almost similar to the results observed for the previous DUT in Fig. 8. For this DUT, the energy dissipated during the first SC cycle is approximately 0.40 J and slightly decreases to 0.38 J after 150 SC cycles. In the case of the previous DUT, we did not observe any modification of I_{GSS} before the failure. This can be explained by the larger interval time step which does not allow to precisely detect the evolution of the leakage current I_{GSS} .

The SC duration of these two DUTs ($4 \mu\text{s}$ and $4.4 \mu\text{s}$) is still sufficient for a transient gate leakage current $I_{G,tr}$ to occur even during the first SC pulse. From these results, a hypothesis is that this transient gate leakage current may cause the physical degradation of the gate or field oxide. This leakage current is not necessarily an indicator of the gate degradation but it may be a precursor. As the SC stress is repeated, percolation of the defects may appear leading, to conductive paths and the continuous gate currents observed in the experiments. The influence of the gate leakage current on the repetitive robustness in SC stress is analysed in the next session by decreasing the SC duration further.

4.2.3. Short circuit cycle without transient gate leakage current

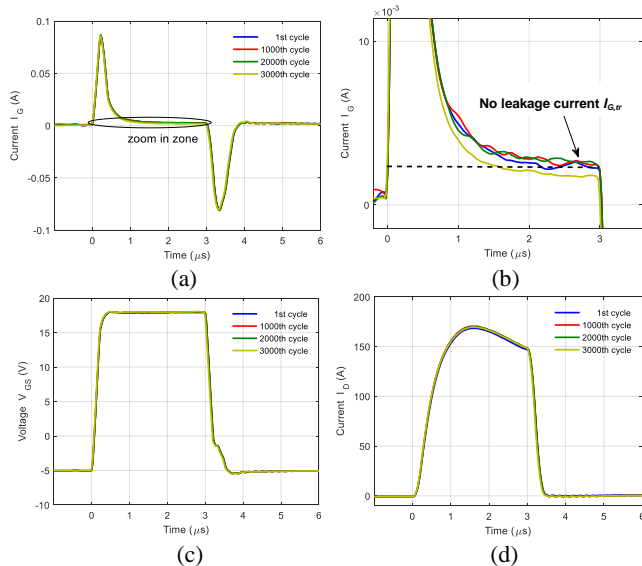


Fig. 9. (a) I_G , (b) Zoom in I_G , (c) V_{GS} and (d) I_D of DUT during repetitive short circuit, with $t_{SC} = 3 \mu\text{s}$, $R_G = 47 \Omega$, $T_{CASE} = 25^\circ\text{C}$, $U_{DC} = 600\text{V}$.

By means of estimating instant of $I_{G,tr}$ appearance in previous DUTs, the SC duration is decreased to $3 \mu\text{s}$ to avoid $I_{G,tr}$. Fig. 9 depicts the behaviour of DUT with a SC duration of $3 \mu\text{s}$ at $T_{CASE} = 25^\circ\text{C}$. During the SC phase, we do not observe any transient gate leakage current $I_{G,tr}$ (Fig. 9.a and Fig. 9.b). The evolutions of V_{GS} and I_D are not significant during the repetition of the SC cycles. So, the DUT sustained 3000 cycles without any gate degradation or other modification of its performances. Under these conditions, if the SC pulse is short enough to avoid any transient leakage current $I_{G,tr}$ in the gate, the robustness of

the DUT in repetitive SC cycles seems to be very good. As there is no evolution of the drain current during these repetitive tests, the energy dissipated remains identical at 0.26 J for each of the 3000 SCs.

Table IV - Evolution of electrical parameters of DUT under repetitive SC with $t_{SC} = 3 \mu\text{s}$, $T_{CASE} = 25^\circ\text{C}$.

Cycle	V_{TH} (V)	I_{GSS}	R_{DSON} (m Ω)	I_{DSS} (nA)
0	1.99	<100 fA	77	1.85
1000	2.02	<100 fA	78	1.81
2000	1.97	<100 fA	76	1.77
3000	2.01	<100 fA	80	1.77

The static gate leakage current remains under the level measurable with our testing setup (below 100 fA in Table IV), and the variations of V_{TH} , R_{DSON} and I_{DSS} are negligible. This reveals that there is no evolution of these electrical parameters and that the DUT operates reliably in repetitive SC cycles at this low energy level.

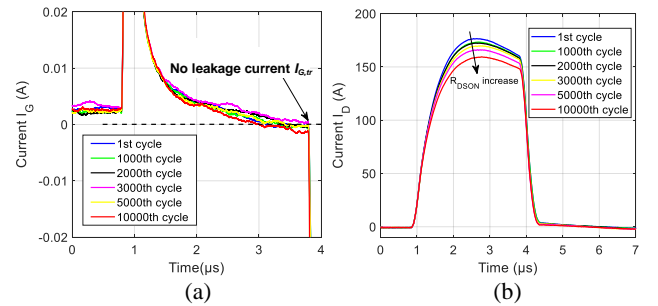


Fig. 10. (a) I_G and (b) I_D of DUT during repetitive short circuit, with $t_{SC} = 3 \mu\text{s}$, $R_G = 47 \Omega$, $T_{CASE} = 150^\circ\text{C}$, $U_{DC} = 600\text{V}$.

Table V - Evolution of electrical parameters of DUT under repetitive SC with $t_{SC} = 3 \mu\text{s}$, $T_{CASE} = 150^\circ\text{C}$.

Cycle	V_{TH} (V)	I_{GSS}	R_{DSON} (m Ω)	I_{DSS} (nA)
0	1.99	<100 fA	80.47	2.43
1000	2.09	<100 fA	80.90	2.89
2000	2.11	<100 fA	82.47	2.10
3000	2.10	<100 fA	84.36	2.20
5000	2.07	<100 fA	90.30	2.11
10000	2.01	<100 fA	94.46	1.79

Fig. 10 presents the same behaviour at higher case temperature (150°C). Here again, with a SC duration of $3 \mu\text{s}$, no significant transient gate leakage current $I_{G,tr}$ was detected during the SC phase (Fig. 10.a). Even after 10000 cycles, I_{GSS} , V_{TH} and I_{DSS} remain constant, although a significant increase of about 17% in R_{DSON} was observed (Table V). The R_{DSON} increase has been extensively studied previously on other components and can be related to the reconstruction of source metallization and/or the lifting or the degradation of bond wires. Aluminum reconstruction results in the increase of the aluminum sheet resistance and leads to depolarization of the gate to source voltage which in turns decreases the saturation drain current (Fig. 10.b) like already observed in [27]. As a consequence, the dissipated energy has clearly reduced from 0.27 J to 0.24 J between the first and the 10000th SC cycle. The simulation allows determining a maximum T_j of about 740°C for the 1st SC cycle. It is interesting to note that this is lower than the temperature estimated in section 4.2.2 ($T_{J,max} = 840^\circ\text{C}$). The transient gate leakage current $I_{G,tr}$ would therefore possibly appear, once the junction temperature reaches a critical value of approximately 840°C , difficult to estimate precisely seeing as the uncertainties linked to the thermal simulation (physical parameters and device geometry).

5. Conclusion

For silicon IGBTs or MOSFETs, it is possible to define a single critical energy. Below this threshold, the devices can sustain many SC events. On the contrary, they fail as soon as any SC event exceeds the critical energy level. In the case of SiC MOSFETs, the separation between safe operating operations in SC and failure is not so clear, and must be carefully analysed, especially if the device must support several SC events over its lifetime. For all these reasons, we introduce another parameter, the “repetitive critical energy”. This parameter corresponds to the highest SC energy that a device is able to sustain repetitively. Above the repetitive critical energy threshold, the DUT degrades rapidly during repetitive SC. Below this threshold, the DUT can sustain a large number of SC cycles.

From our observations, it appears that the repetitive critical energy value is dictated by the occurrence of a transient gate leakage current during the SC pulse, which we suppose gradually degrades the gate oxide or the field oxide. This wear-out mechanism eventually results in the large gate current observed after a few hundreds of SC pulses. This means that the apparition of a transient gate leakage current can indicate a premature ageing of the component and can be used to predict a future failure of the component.

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APPENDIX A

Measurement of electric parameters as ageing indicators using B1505 Agilent curve tracer.

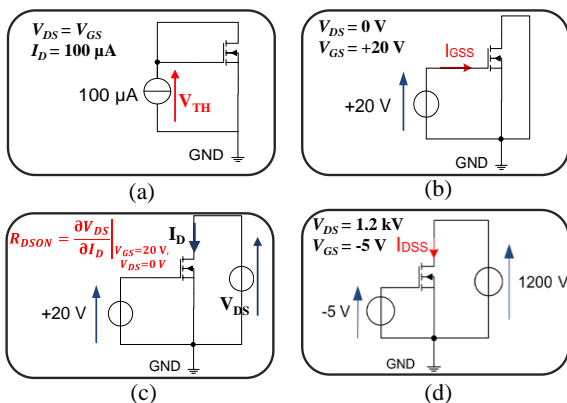


Fig. 11. Circuit diagram for measurement of (a) threshold voltage V_{TH} , (b) Gate leakage current I_{GSS} , (c) on-state resistance $R_{DS(on)}$ and (d) Drain leakage current I_{DS} .

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