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# Surge Current Capability of Ultra-Wide-Bandgap Ga<sub>2</sub>O<sub>3</sub> Schottky Diodes

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## Abstract

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is an emerging ultra-wide-bandgap semiconductor material offering superior power material limits over Si, SiC, and GaN as well as the availability of large-diameter wafers growing from its own melt. However,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices performance may be limited by the relatively poor thermal conductivity of the material.

In this paper, we investigate the behavior of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky diodes in the condition of forward current surge to explore their electro-thermal ruggedness and the related thermal management. An analytical electro-thermal device model is calibrated with experimental devices and TCAD simulations. Then this device model is incorporated into a SPICE electro-thermal network model, which is used to simulate the device temperature rise during the surge transient, considering various device and packaging configurations (i.e. various chip thicknesses and chip orientations).

It is found that provided heat is removed from the junction side, a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky diode offers a robustness to surge current exceeding that of a SiC Schottky diode. The low thermal conductivity of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is found to be overcome by the enhanced heat extraction from junction-side cooling, as well as by the intrinsically small temperature dependence of the on-resistance (and conduction loss) of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices.

## 1. Introduction

From an electrical point-of-view,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is a very promising material. Its high critical electric field ( $\approx 8 \text{ MV cm}^{-1}$ ) [1], in particular, makes it very attractive for power semiconductor devices. This can be summarized using the Baliga's Figure Of Merit (the product of a material permittivity, electron mobility, and critical field raised to the cubic power,  $\mu\epsilon E_c^3$ ). The BFOM of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is higher than that of the main wide-bandgap semiconductor materials, at 3444 (vs. 340 and 870 for SiC and GaN, respectively) [2]. This means that devices made using  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> can offer a lower on-state resistance for a given voltage rating than those made out of Si, SiC or GaN. Several high voltage, low resistance  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices have already been demonstrated, such as a  $2 \text{ m}\Omega \text{ cm}^2$ , 1100 V diode [3]. High-voltage  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diodes operational at high temperatures up to 350 °C have also been demonstrated [4].

Another advantage of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is material growth: contrarily to SiC and GaN, bulk, mono-crystalline  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates can be produced by a variety of melt-growth processes [5]. Substrates up to 100 mm in diameter are readily available, and 150 mm wafers are under development [1].

However,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> suffers from a major drawback: its thermal conductivity is very low ( $11$  to  $27 \text{ W m}^{-1} \text{ K}^{-1}$  depending on the crystal orientation [6]), approximately 10 to 20 times lower than that of GaN or SiC. This means that the semiconductor chip has a relatively high thermal resistance, making it much more difficult to remove heat from the semiconductor junction

to a heatsink. When dissipating the same power density as a SiC device, a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device will run much hotter (70 °C more in an example [7]). This may cause the device to exceed its safe operating temperature, which is limited by either the Schottky contact or the packaging materials. This also may reduce its long-term reliability due to wider thermal cycling temperature range.

A common application scenario that may cause the diode to exceed its maximum junction temperature is current surge. This may happen for example when the output of a diode rectifier is short-circuited. In this case, the diode must temporarily carry a current intensity noticeably higher than what it can sustain in steady state (nominal) conditions. This surge current value is listed in a diode's datasheet, and the corresponding tests are defined in JEDEC standards [8]. One particular test uses a half-sine current-pulse at the frequency of the ac electrical grid (here 50 Hz).

Current surges are transitory events, which result in the junction temperature of the diode rising dramatically: at one point during the current surge tests performed in [9], the junction temperature of a SiC Schottky diode was estimated to be more than 800 °C. This very high temperature transient is the result of two concomitant effects: first, the limited thermal inertia of the semiconductor chip; secondly, the positive temperature coefficient of the conduction losses, which causes the dissipated power to increase with the junction temperature, and may result in thermal runaway.

Several techniques have been developed to improve the current surge capability of semiconductor devices. Increasing the thermal inertia by clamping the semiconductor chip between

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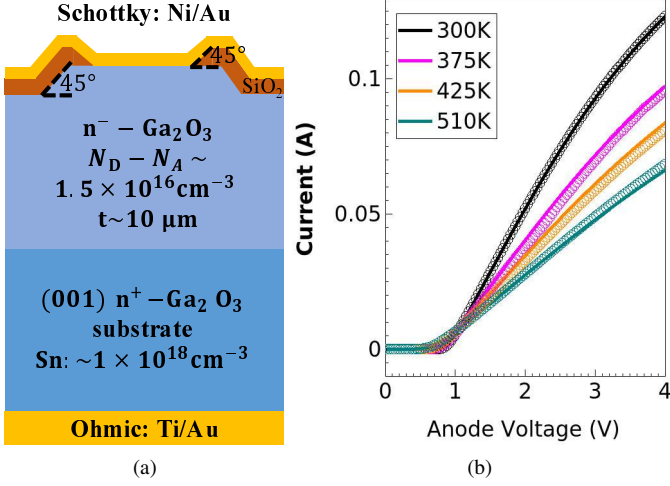


Figure 1: (a) Structure of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diodes. (b) Calibration of the TCAD simulation model: experimental (lines) and TCAD simulated (markers) IV curves at different temperatures.

two thick metal shims, for example, may result in doubling of the current surge capability of a SiC diode, as compared with a more standard single-side cooling approach [10]. Another approach is to limit the increase in conduction losses with temperature. For SiC Schottky diodes, this is achieved by introducing bipolar junctions to form JBS (Junction Barrier Schottky) or MPS (Merged Pin Schottky) structures. This was found to noticeably improve the robustness of the diodes to thermal runaway [11].

Unfortunately, JBS or MPS structures require p-type doping and hole conduction, which are not available for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices [3]. Only unipolar diodes can be made using this material. Therefore, current surge capability of these diodes is based on the intrinsic properties of the material and on the thermal performance of the associated package.

In this paper, we investigate the evolution of the conduction losses of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes, based on experimental devices fabricated on commercial 2-inch  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> wafers (section 2). Then we develop an electro-thermal model of the diodes and their packaging (section 3), and use this model to predict the surge current behavior of the diodes (section 4).

## 2. Effect of the Temperature on the Forward Characteristic of a $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky Diode

To calibrate the electro-thermal simulation models,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power Schottky Barrier Diodes (SBDs) have been fabricated on 2-inch  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates. As shown in Fig. 1a, the epitaxial structure consists of a Si-doped n-Ga<sub>2</sub>O<sub>3</sub> layer ( $N_D \approx 1.5 \times 10^{16} \text{ cm}^{-3}$ ,  $\approx 10 \mu\text{m}$  thick) grown by Hydride Vapour Phase Epitaxy (HVPE) on a commercial 2-inch n<sup>+</sup>-Ga<sub>2</sub>O<sub>3</sub> substrate. The detailed device fabrication and performance are reported in [4]. The device I-V and C-V characteristics were measured up to 510 K, and were then used to calibrate the TCAD electro-thermal simulation models (Fig. 1b). The net  $N_D$  extracted from C-V characteristics shows nearly no dependence

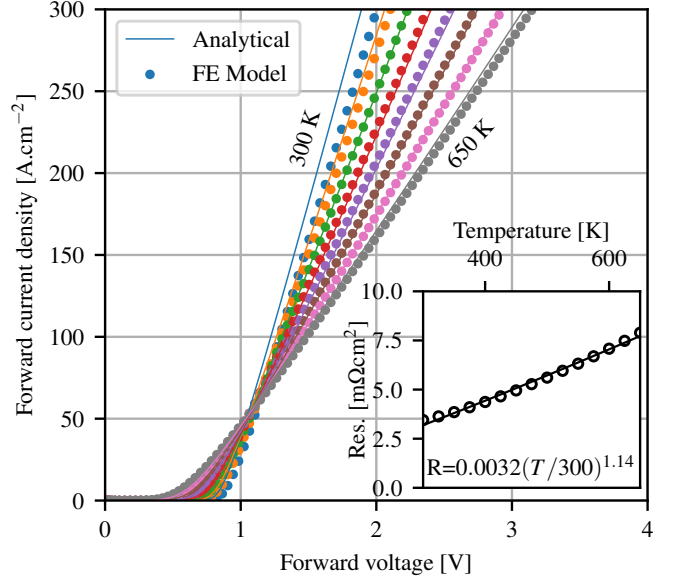


Figure 2: On-state characteristic of a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> as generated from finite element (TCAD) simulation, and corresponding analytical model, for temperatures ranging from 300 to 650 K. The inset graph presents the change in dynamic resistance as a function of temperature.

on temperature, indicating that Si is fully ionized in the drift region.

To understand the thermal limit of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power diodes, a 1.2 kV  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power SBD with an optimal drift region is designed. Here the breakdown voltage ( $BV$ ) is designed as 1440 V to provide a 20 % safety margin for voltage rating and the maximum average electric field ( $E_m$ ) at the Schottky contact is designed as  $4 \text{ MV cm}^{-1}$  based on the state-of-the-art experimental results [3, 12]. The thickness ( $t_D$ ) and donor concentration ( $N_D$ ) are designed based on the non-punch-through model, i.e.  $t_D = 2BV/E_m$  and  $N_D = qE_m^2/2qBV$ , to be  $7.2 \mu\text{m}$  and  $3.07 \times 10^{16} \text{ cm}^{-3}$ , respectively. The I-V characteristics of this optimized 1.2 kV  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power rectifier are then generated by the well-calibrated TCAD simulation up to 650 K.

With the objective of performing simple SPICE transient simulations, an analytical macro model is then fitted to this TCAD model (Fig. 2). This analytical model (forward conduction only) is comprised of two elements. The first is the Schottky junction, represented using a thermionic emission equation [24]:

$$I_F = S A^* T_j^2 e^{\frac{q\Phi_{BN}}{kT_j}} \left( e^{\frac{qV_D}{nkT_j}} - 1 \right) \quad (1)$$

where  $S$  is the junction area,  $A^*$  the effective Richardson constant,  $T_j$  the junction temperature,  $q$  the electronic charge,  $\Phi_{BN}$  the barrier height,  $n$  the ideality factor,  $V_D$  the voltage across the junction,  $k$  the Boltzmann's constant. The second element of the model corresponds to the electric resistance, mainly of the drift layer and substrate:

$$R_{on}(T_J) = R_{300} \left( \frac{T_J}{300} \right)^\alpha \quad (2)$$

with  $R_{300}$  the resistance at 300 K, and  $\alpha$  an exponent (in

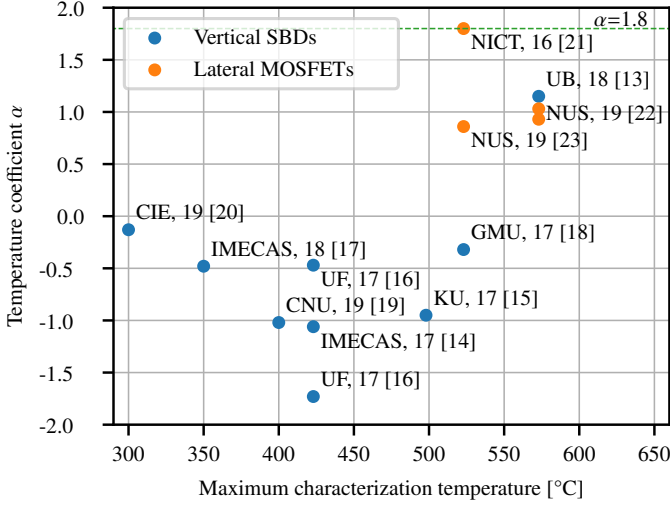


Figure 3: Value of the temperature-dependence coefficient  $\alpha$  for devices published in the literature, as a function of the maximum test temperature (with  $R_{on}(T) = R_{300} \left( \frac{T}{300} \right)^\alpha$ )

Fig. 2,  $\alpha = 1.14$ ). The value of  $\alpha$  appears to vary strongly from one device to another according to the literature. The relation between on-resistance ( $R_{on}$ ) and the temperature is vital to analyze the thermal stability of power devices [11, 25]. Following the commonly used power law in (2), we extracted the temperature coefficient  $\alpha$  in all experimental  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power devices with high-temperature performance we could find in the literature. As shown in Fig. 3, the highest  $\alpha$  is close to 1.8 in lightly doped lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> thin-film MOSFETs. This  $\alpha$  is mainly determined by the temperature dependence of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> mobility, which follows a  $T^{-1.5}$  power law as the result of phonon scattering [26, 27]. Much lower or even negative  $\alpha$  is found for many vertical  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power devices. This is attributed to the increased donor ionization in the  $n^+$ -Ga<sub>2</sub>O<sub>3</sub> substrate at high temperatures [4, 28]. These  $\alpha$  dependencies have also been validated by our TCAD simulation. To consider the worst case corresponding to the fastest  $R_{on}$  increase with temperature,  $\alpha$  is changed from 1.14, which provides the best fitting to our TCAD and experimental data (Fig. 2), to 1.8, with all other parameters in the analytical model remaining unchanged.

### 3. Electro-thermal Model of the Diode

The electro-thermal model in Fig. 4 contains two parts. First, the electric circuit, with the sine current source  $I_1$ , resistor  $R_{eq}$  (for easier convergence of simulation), diode  $D_1$  (to carry negative currents), and the model of the diode under test. This diode model contains two elements, a behavioral current source  $BI_1$  (to implement (1)) and a behavioral resistance  $BR_1$  (to implement (2)). The second part of the circuit represents the thermal model in the form of a Cauer network.

For the thermal model, two cases are considered (see Fig. 5): the chip is mounted either in the standard way (i.e with the Schottky junction on top), or it is mounted in the "flip-chip" configuration (with the Schottky junction at the bottom of the

Table 1: Parameters used for the electrothermal simulations

Parameter	Name	Value
Room temp.resistance (arbitrary)	$R_{300}$	8 m $\Omega$
Temperature coefficient of resistance	$\alpha$	1.8
Ther. cond. of $\beta$ -Ga <sub>2</sub> O <sub>3</sub> on [001] [6]	$\lambda_{Ga_2O_3}$	14 W m <sup>-1</sup> K <sup>-1</sup>
Thermal conductivity of Cu [29]	$\lambda_{Cu}$	394 W m <sup>-1</sup> K <sup>-1</sup>
Thermal cond. of Sintered Ag [30]	$\lambda_{Cu}$	238 W m <sup>-1</sup> K <sup>-1</sup>
Specific heat of $\beta$ -Ga <sub>2</sub> O <sub>3</sub> [31]	$c_{pGa_2O_3}$	560 J K <sup>-1</sup> kg <sup>-1</sup>
Specific heat of Cu [29]	$c_{pCu}$	385 J K <sup>-1</sup> kg <sup>-1</sup>
Specific heat of Sinterd Ag [30]	$c_{pCu}$	233 J K <sup>-1</sup> kg <sup>-1</sup>
Density of $\beta$ -Ga <sub>2</sub> O <sub>3</sub> [1]	$\rho_{Cu}$	5950 kg m <sup>-3</sup>
Density of Cu [29]	$\rho_{Cu}$	8960 kg m <sup>-3</sup>
Density of Sintered Ag [30]	$\rho_{Cu}$	8580 kg m <sup>-3</sup>
Chip thickness (arbitrary)	$t_{chip}$	100 or 400 $\mu$ m
Baseplate thickness (arbitrary)	$t_{base}$	1 mm
Chip area (arbitrary)	$S$	25 mm <sup>2</sup>
Ambient temperature (arbitrary)	$T_A$	300 K

chip). In the first case, power is dissipated on top of the chip and heat must diffuse through the entire chip thickness before reaching the attach and the baseplate (this is referred to as "backside cooling"). In the second case, the heat dissipated at the Schottky junction has direct access to the attach and baseplate (this is referred to as "junction cooling"). In both cases, a uniform power dissipation is considered at the corresponding surface of the chip. The side surfaces are considered adiabatic. The bottom surface of the baseplate and the top surface of the chip are considered to exchange heat with the environment through a high thermal resistance ( $R_{exch} = 100$  K W<sup>-1</sup>). Note that due to the transient nature of the surge current, this thermal resistance has little effect on the results presented below.

For the sake of simplicity, the baseplate and the chip are considered to have the same surface area, so heat spreading effects can be neglected (1-D heat propagation condition). In this case, the chip and baseplates can be subdivided in a series of thermal resistance ( $R_{Th}$ ) and capacitance ( $C_{Th}$ ) cells:

$$R_{Th_a} = \frac{t_a}{N_a \lambda_b S} \quad (3)$$

$$C_{Th_a} = \frac{t_a}{N_a} S \rho_b C_{p_b} \quad (4)$$

where subscript  $a$  stands for either the baseplate, silver die attach, or chip and subscript  $b$  for the corresponding material ( $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, Ag or Cu);  $t_a$  is the thickness of the element;  $N_a$  the number of subdivisions;  $\lambda_b$  the thermal conductivity of the corresponding material;  $\rho_b$  its density and  $C_{p_b}$  its specific heat;  $S$  is the chip surface area. The numerical values of these parameters are listed in table 1.

In combination with the two cooling configurations, two chip thicknesses are considered (100 and 400  $\mu$ m) to investigate the effect of the semiconductor thickness on the surge current behavior. The model from Fig. 4 has been simulated using LTSpice. The same model is also simulated considering SiC instead of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, using the model parameters for a SiC Schottky diode presented in [11]. For the sake of comparison, both  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and SiC diodes are supposed to have a surface area of 0.25 cm<sup>2</sup> and a nominal resistance ( $R_{300}$ ) of 8 m $\Omega$ . The main

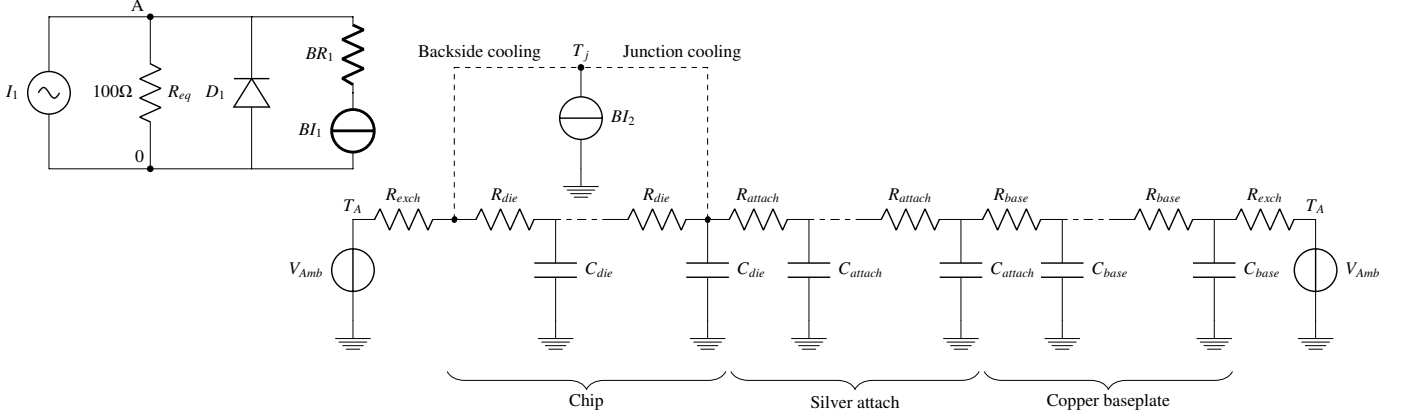


Figure 4: The electrothermal model used for SPICE simulation: the electrical circuit including the diode model comprised of behavioral elements  $BI_1$  and  $BR_1$  and the thermal network with the power source  $BI_2$  which can be connected to either the top or the bottom surface of the chip.

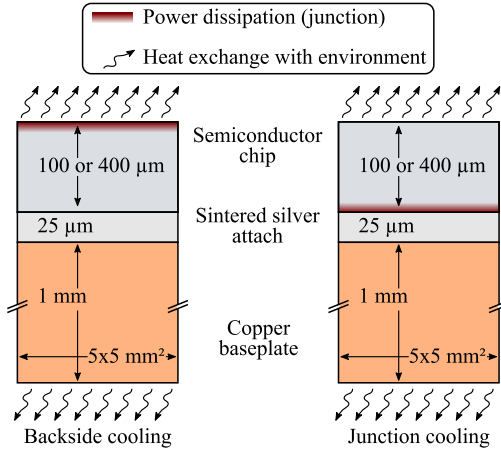


Figure 5: Packaging structures considered for the electro-thermal analysis.

difference is the temperature sensitivity of the resistance ( $\alpha$ ), which was found to be 2.95 for the SiC diode investigated in [11], while it is considered to be 1.8 for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> in the present article.

#### 4. Simulation Results

A transient simulation of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices (Fig.6) shows the calculated temperature rise for a 200 A peak, half-sine current pulse. This value was chosen as it is very close to the thermal runaway limit for the backside cooled, 400  $\mu$ m-thick chip (above this current level, the junction temperature becomes unrealistic, at several thousand degrees Celsius). It can be seen that while the temperature only rises moderately for both junction cooling cases, it increases much more for the backside cooling cases. For the junction cooling, the maximum temperature exceeds 400 °C and 1000 °C for the 100  $\mu$ m and 400  $\mu$ m-thick chip, respectively. This confirms that because of the poor thermal conductivity of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, heat conduction through the chip is limited, and even the thermal resistance of a chip as thin as 100  $\mu$ m is large enough to cause a temperature rise of more than 300 °C compared to junction-cooled devices.

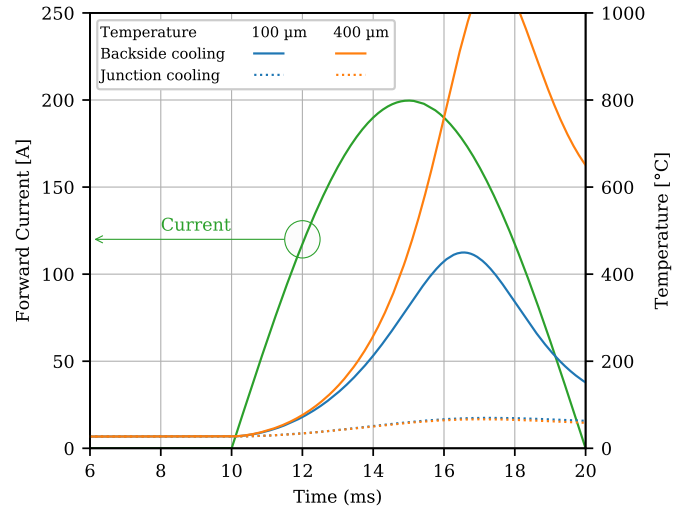


Figure 6: Simulated temperature transient during a current surge (200 A), for the 4 configuration considered (single or double-side cooling, 100 or 400  $\mu$ m-thick  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> chip).

The same data are plotted in Fig. 7, this time as a function of the forward voltage rather than time. Such representation highlights the effects of the increase in forward voltage drop (as the diode heats up) on the power dissipation. As temperature increases, so does the forward voltage drop, due to the increase in dynamic resistance, as described by (2). As a result, the power dissipation (the product of forward current and voltage) also increases, causing the temperature to rise further. The right-most graphs in Fig. 7, which correspond to the backside-cooled cases, illustrate this positive feedback: while the current pulse is identical in all cases, the resulting forward voltage is noticeably different (7 V max. for the 100  $\mu$ m-thick chip vs. >12 V max. for the 400  $\mu$ m-thick chip). This means that the elevated junction temperature reached in the backside-cooled, 400  $\mu$ m-thick chip case (>1000 °C) is the result of both the higher thermal resistance of the thicker chip and of the higher power dissipation due to the positive temperature coefficient of the forward voltage drop.



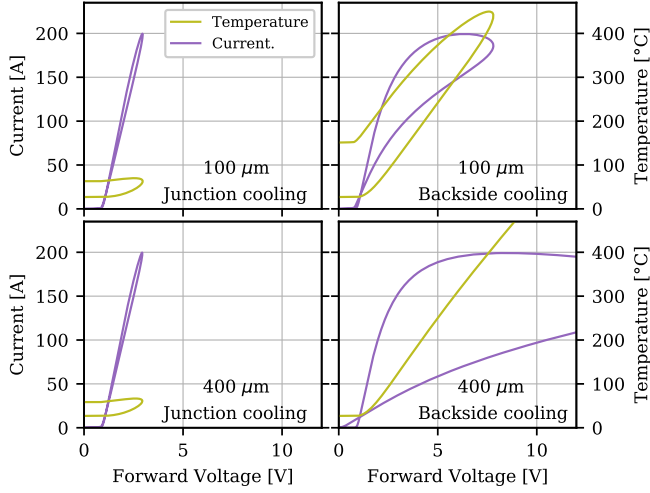


Figure 7: Simulated temperature transient during a current surge (200 A peak), as a function of the instantaneous forward voltage drop for the 4 configuration considered (single or double-side cooling, 100 or 400 μm-thick  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> chip).

Regarding the comparison between SiC and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes, the results are summarized in Fig. 8, for 400 μm-thick chips and a surge current of 200 A. Contrarily to the backside-cooled  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diode (top right graph), the SiC diode can sustain the surge event with little temperature rise, even with backside-cooling (bottom graphs). This is due to the much better thermal conductivity of SiC ( $390 \text{ W m}^{-1} \text{ K}^{-1}$ , as opposed to  $14 \text{ W m}^{-1} \text{ K}^{-1}$  for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>). When considering junction-cooling (leftmost graphs in Fig. 8), both the SiC and the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes show very similar behavior, with only small temperature rise (a few tens of degrees Celsius), as most of the dissipated heat can be absorbed by the chip attach and baseplate.

A more complete comparison between the behavior of SiC and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes is given in Fig. 9. For both materials, backside- and junction-cooled diodes are simulated, considering surge current values ranging from 1 to 500 A. In all cases, the chips are considered to be 400 μm-thick and 25 mm<sup>2</sup> in surface. As expected, backside-cooled chips have the lower surge current capability, and their junction temperature is found to exceed 600 °C above 175 A and 300 A for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and SiC, respectively. Junction-cooled diodes have a higher capability, at 400 A and 500 A for SiC and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> respectively.

Moreover, it can be seen that the temperature of the junction-cooled  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diode (orange line in Fig. 9) is lower than that of its SiC counterpart for peak currents above 300 A. This is because of the lower  $\alpha$  value of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> in (2) compared to SiC (1.8 vs. 2.95): the on-state resistance of the SiC diode increases faster with temperature, causing the SiC diode to enter thermal runaway sooner. As can be seen in Fig. 9, the slope of the blue curve (junction-cooled, SiC diode) becomes vertical at a peak current of 400 A. This means that any small increase in peak current results in a dramatic increase in junction temperature, and corresponds to thermal runaway condition. On the contrary, even though its temperature becomes very high (600 °C for a peak current of 500 A), the junction-

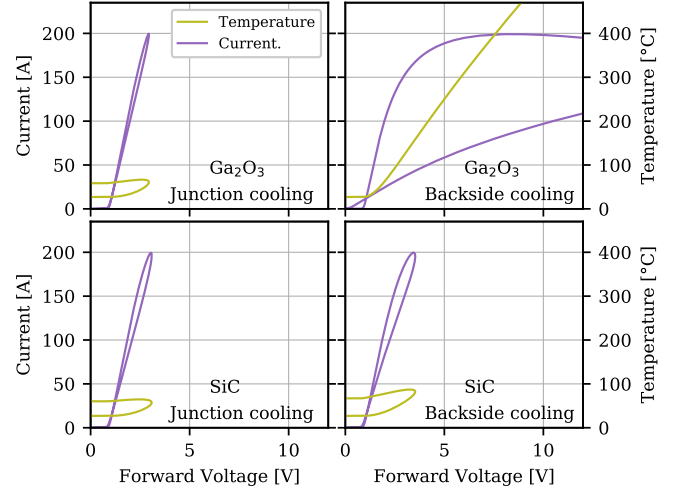


Figure 8: Simulated temperature transient during a current surge (200 A peak), as a function of the instantaneous forward voltage drop for 400 μm-thick chips with single or double-side cooling, and considering  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> or SiC semiconductor material.

cooled  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diode (orange line in Fig. 9) has not reached thermal runaway yet.

## 5. Conclusion

The poor thermal conductivity of the material has a strong effect on the current carrying capability of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes in a conventional backside-cooled package. This is especially true regarding surge current reliability, when the diodes have to sustain a transient increase in current.

Reducing the chip thickness from 400 μm to 100 μm would reduce the thermal resistance of the chip, albeit not enough to achieve a surge current capability comparable to that of a SiC diode with the same chip size.

"Flipping" the chip, so that its junction would be in direct contact with the copper baseplate is found to be a much more efficient solution, as this removes the thermal resistance of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> chip entirely. For a peak surge current of 200 A ( $800 \text{ A cm}^{-2}$ ), the behaviors of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and the SiC diodes are found to be very comparable. For higher peak surge current (above 300 A, or  $1200 \text{ A cm}^{-2}$ ), however, the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diode exhibits a lower temperature rise and a much more stable behavior: while the SiC diode enters thermal-runaway above 400 A, no such phenomenon is observed for the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diode up to 600 A. This can be explained by the lower temperature dependency of the on-state resistance ( $\alpha$ ) of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> as compared to SiC. Note that in this article we considered a high value for the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>  $\alpha$  (1.8, see Fig. 3). Lower values would result in an even greater advantage for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.

It can be concluded that the poor thermal conductivity of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is partly balanced by its low sensitivity to temperature.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> can be used to build robust devices, with performances comparable to or exceeding those of SiC. However, this requires changing the way the devices are packaged, to provide cooling closer to the junction.

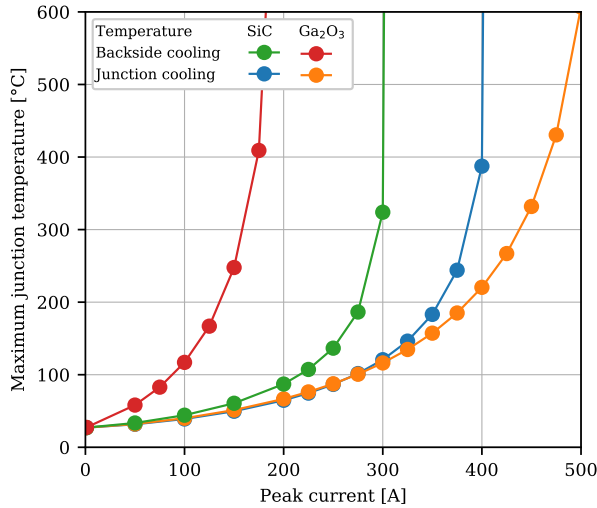


Figure 9: Simulated maximum temperature reached during a surge event as a function of the peak current, for 400  $\mu\text{m}$ -thick SiC and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes.

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