Packaging and Integration Activities at Laboratoire Ampère – CPES Seminar

Cyril Buttay

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Laboratoire Ampère, Lyon, France

09/06/2019

Who am I?

2004	PhD Electrical Engineering (Lyon, France)
2005 – 2007	Research associate (Sheffield and Nottingham, UK)
2008 – 2019	Researcher at CNRS (Lyon, France)
Since 2019	Senior Researcher (eq. Prof.) at CNRS

You can contact me at

- cyril.buttay@insa-lyon.fr
- (540) 998 6694
- Office 151, Whittemore Hall

- scholar.google.fr/citations?user=-gMeCUkAAAAJ
- I'm here until July, 2020!

Where do I come from?

- Laboratoire Ampère
  (named after André-Marie Ampère, born in Lyon)
- 180 people (Faculty, Support, PhD students)
- Academic research lab focusing on:
  - Bio-engineering, biology
  - Automation, System engineering
  - Electrical Engineering
- EE activities:
  - High voltage engineering
  - WBG devices design and test
  - Magnetics (material/design)
  - EMC, Packaging, Integration.

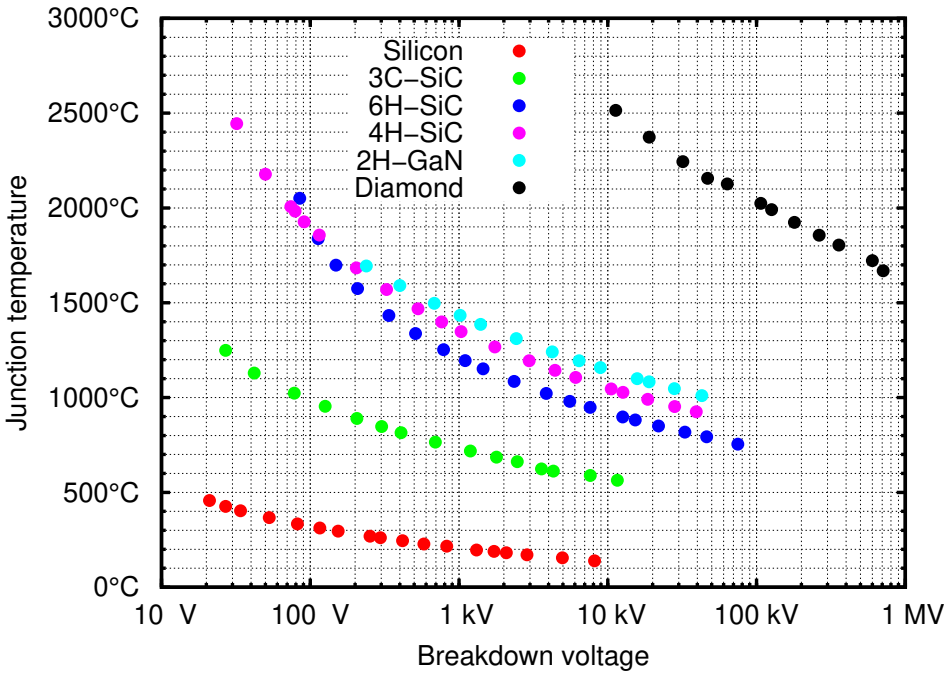
`http://www.ampere-lab.fr`

Source globe:wikipedia

Outline

Outline

Operating Temperature Limits



Source: C. Raynaud et al. "Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices" Diamond and Related Materials, 2010, 19, 1-6

Some limits:

660°C Aluminium melts

≈ 300°C Die Solder melts

200 – 250 °C Silicone gel degrades

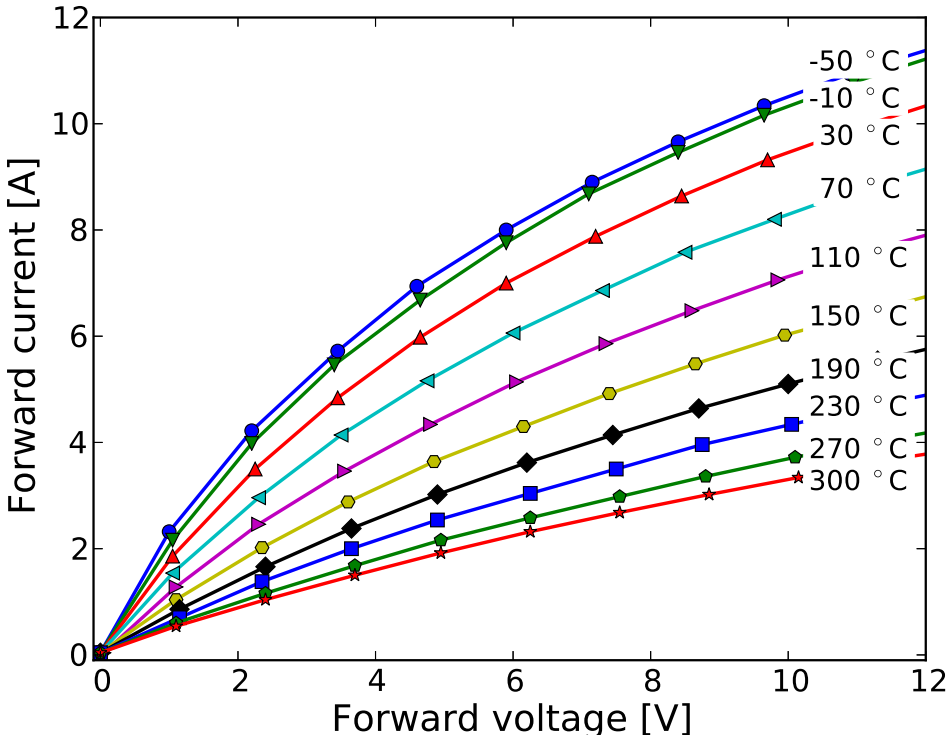
≈ 200°C Board solder melts

- **For Wide-Bandgap devices, limits set by packaging**
- Additional packaging issues with thermal cycling

Outline

High temperature behaviour of SiC devices – [1, 2]

Static Characterization of 490 mΩ JFET



$V_{GS} = 0\ V$, i.e. device fully-on

- Large increase in on-state resistance with temperature;
- Strong sensitivity of conduction losses to temperature.

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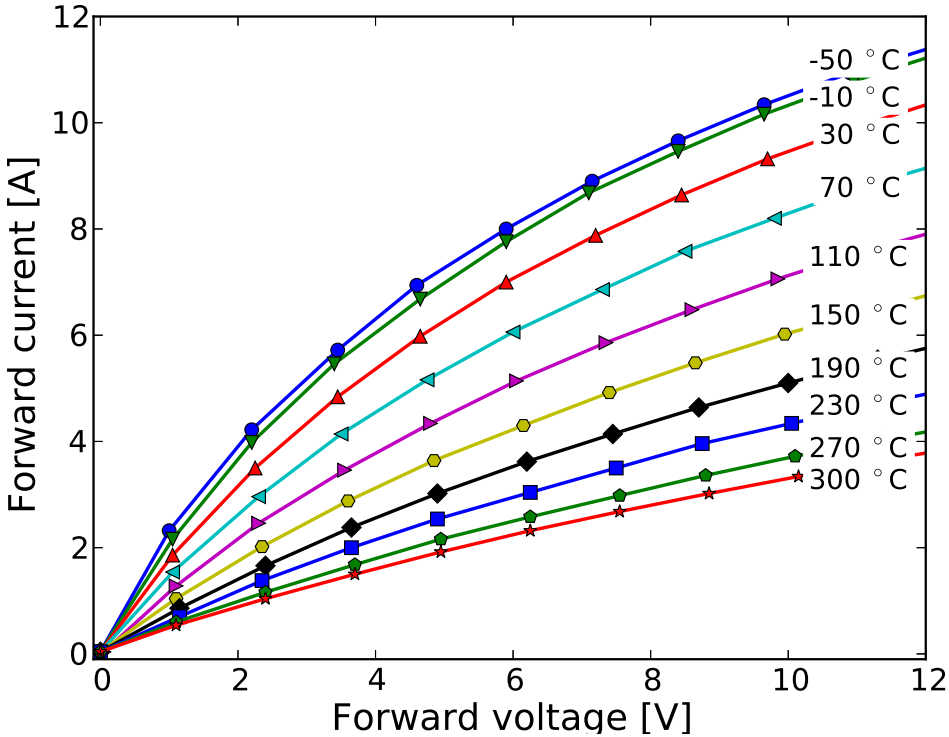

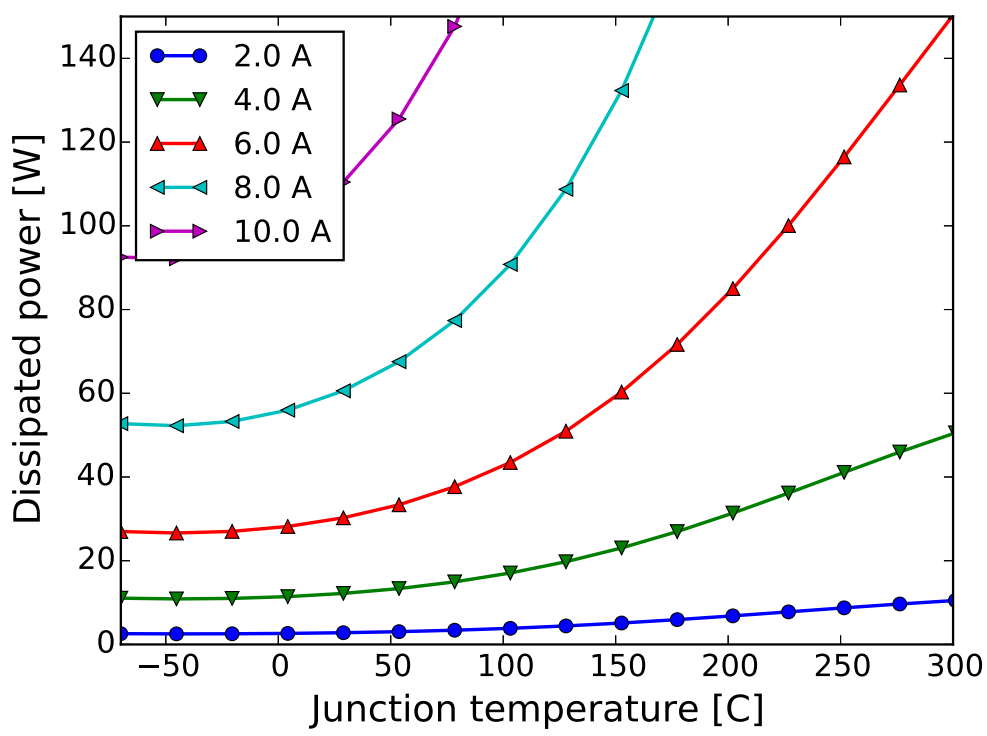

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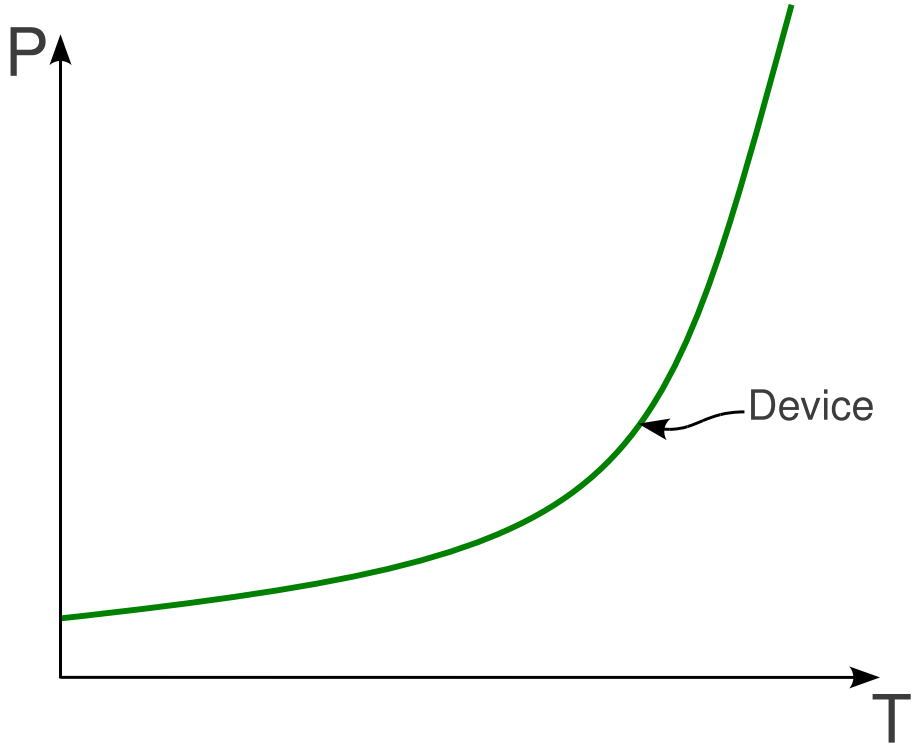

Thermal Run-away mechanism

- The device characteristic
- Its associated cooling system
- Two equilibrium points: one stable and one unstable
- Above the unstable point, run-away occurs

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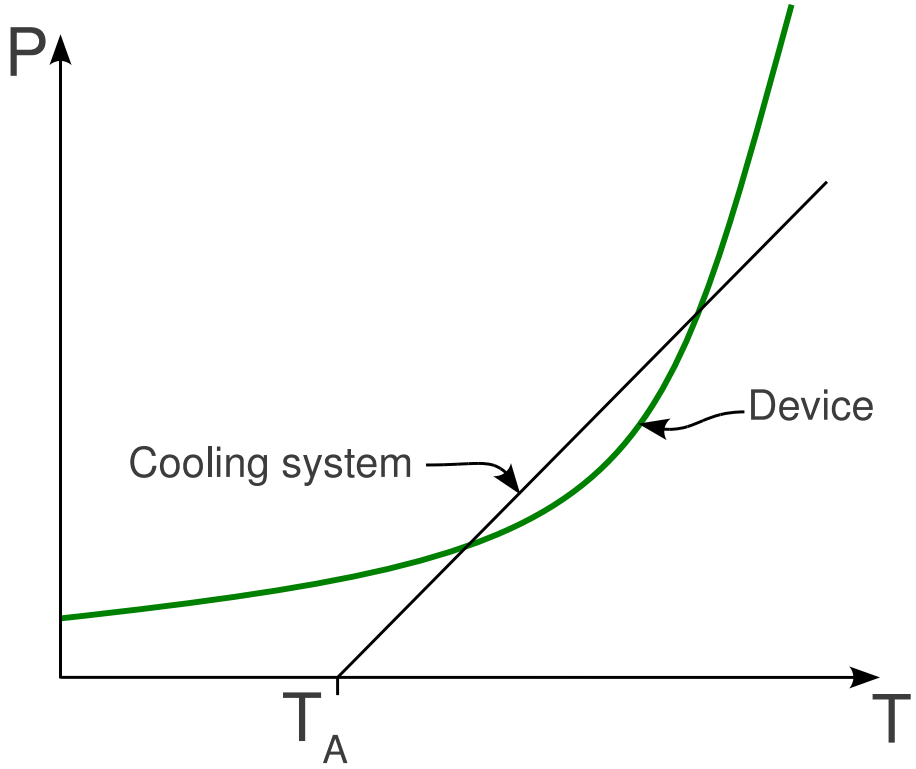

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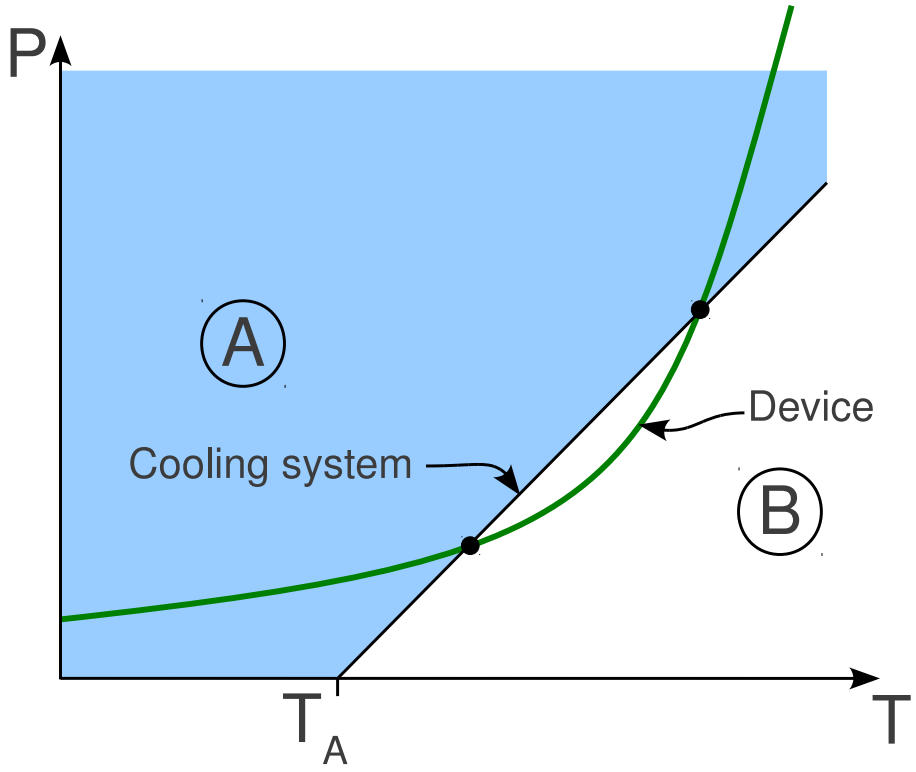

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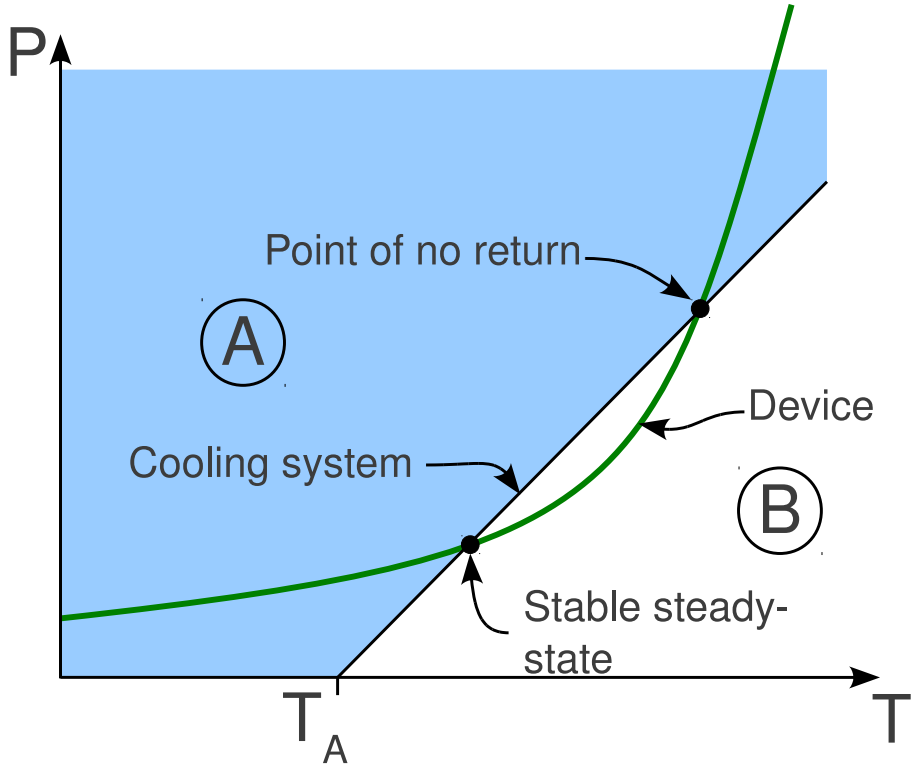

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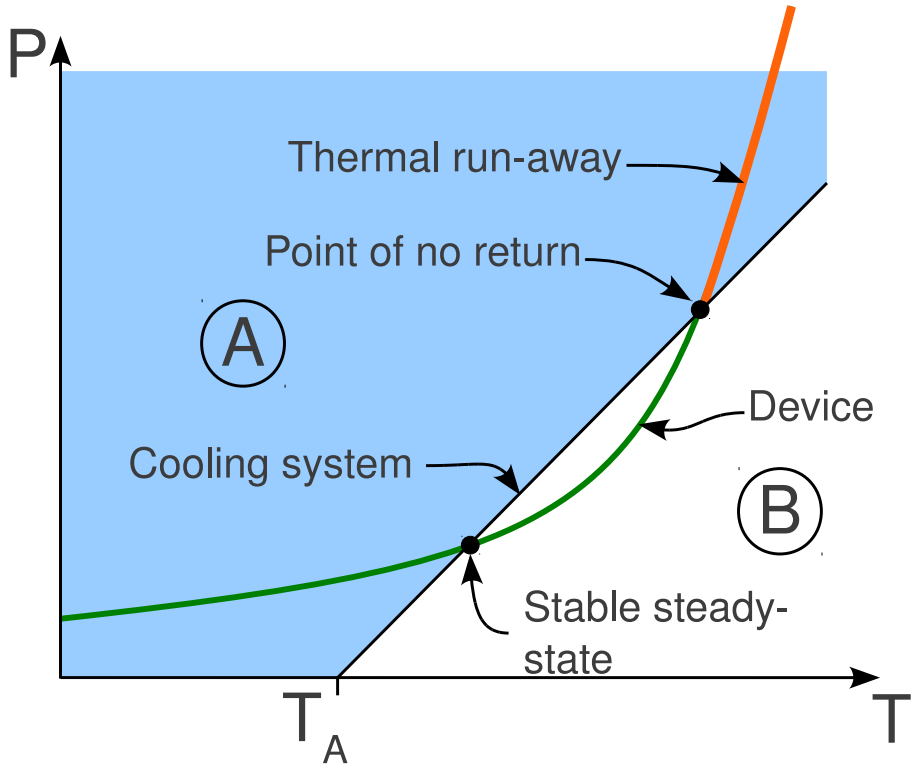

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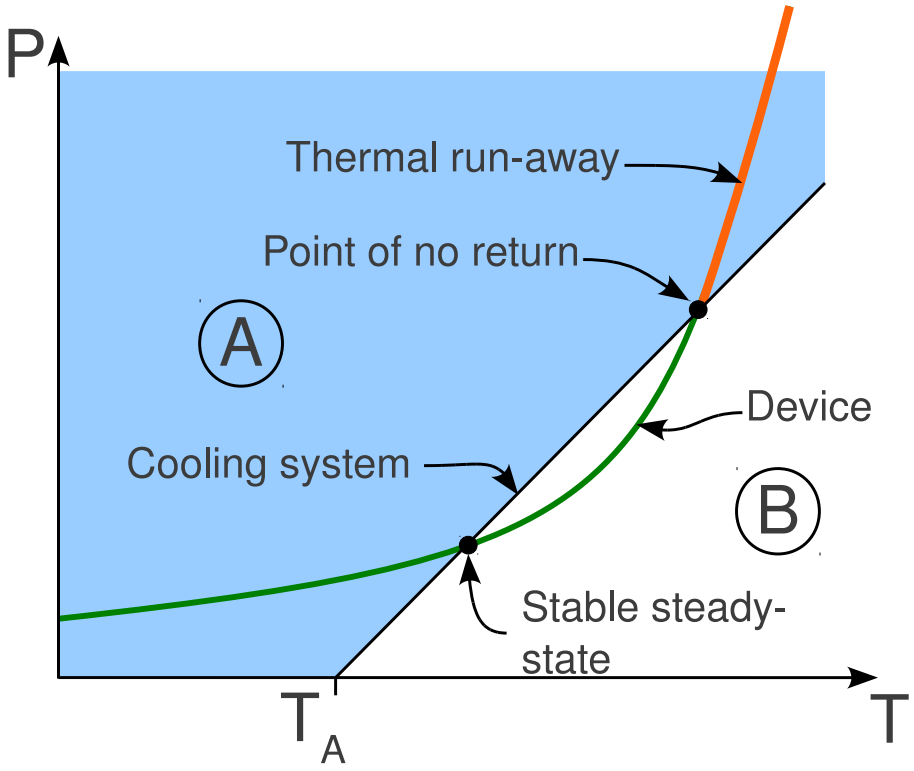

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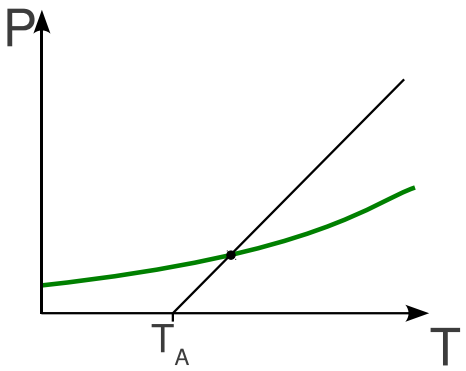
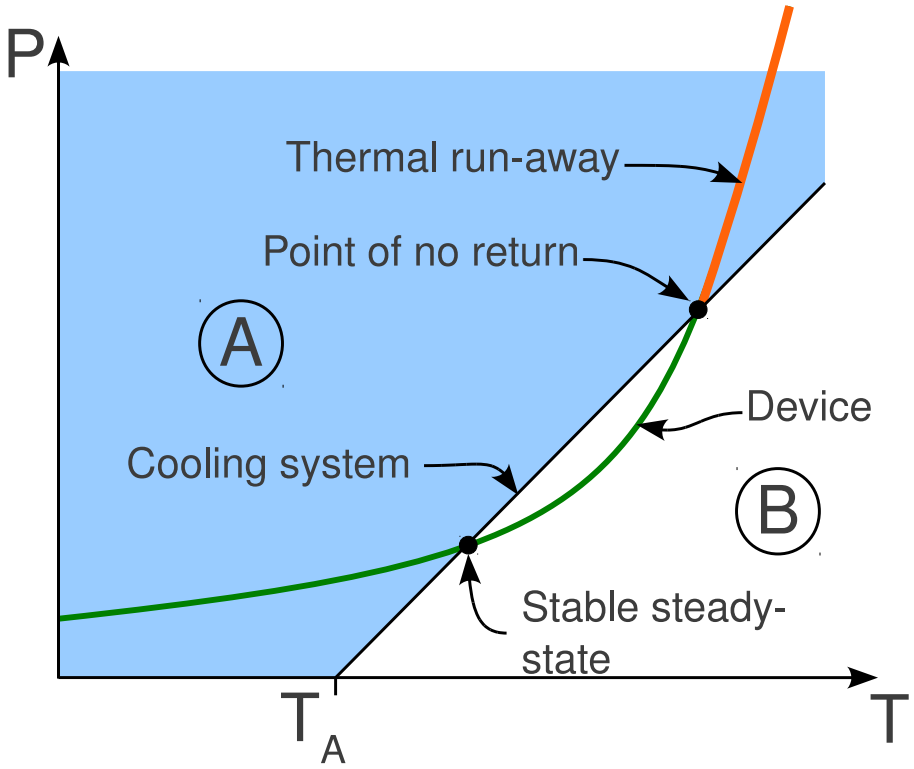


Always stable

High temperature behaviour of SiC devices – [1, 2]



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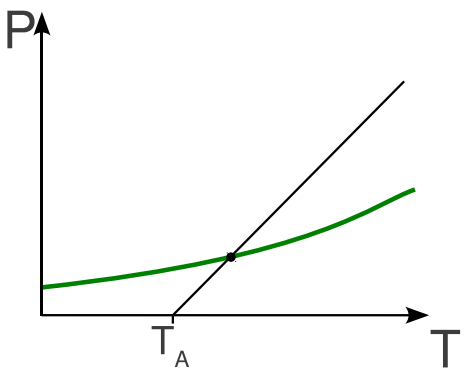

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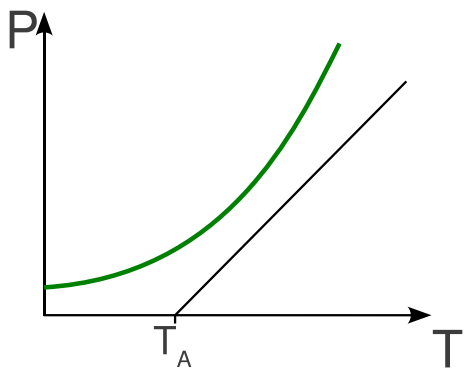

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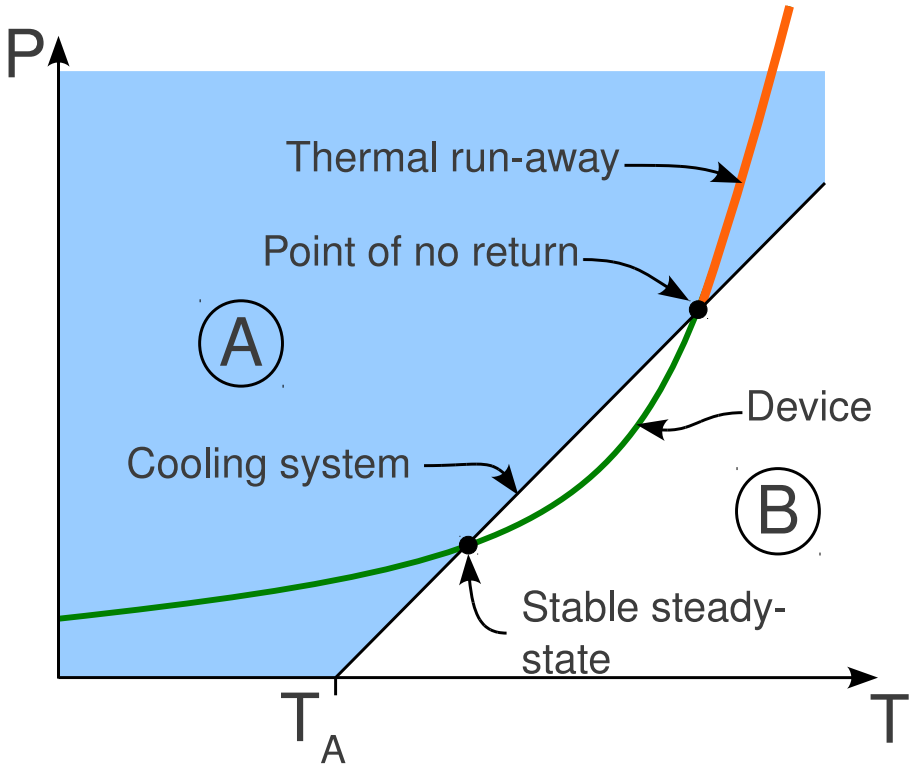

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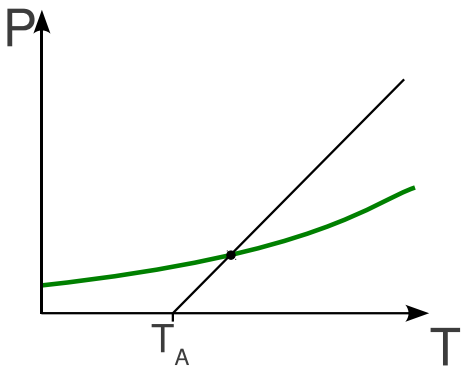

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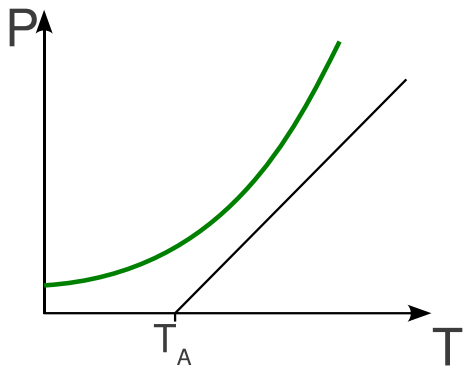

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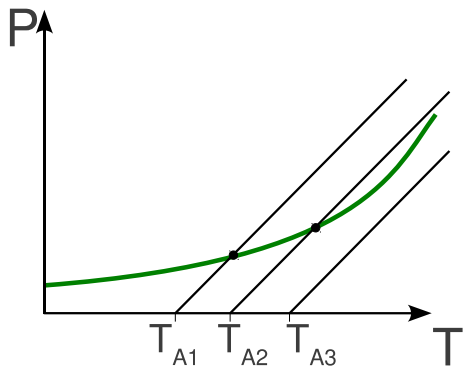
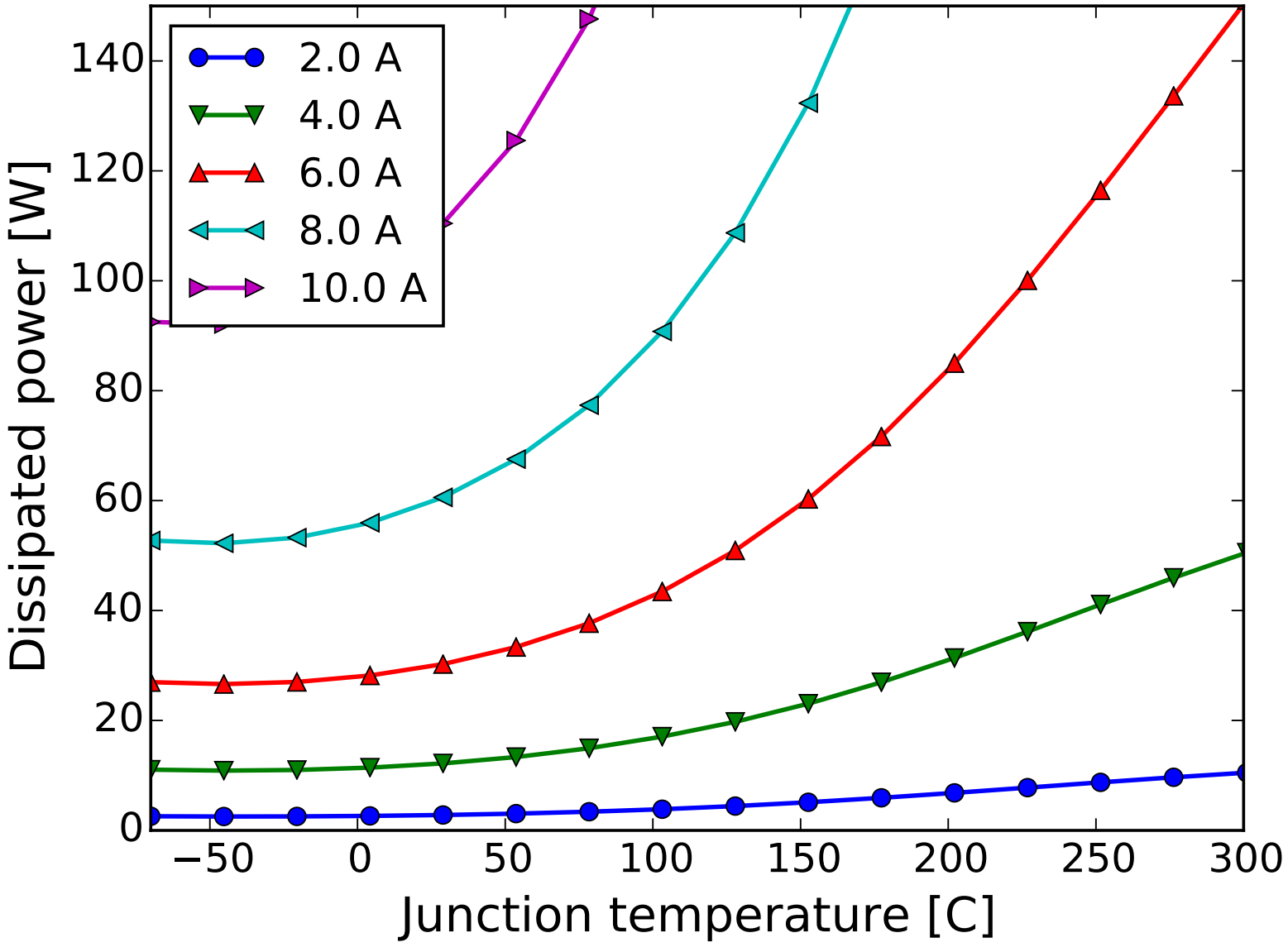


Becomming unstable with ambient temperature rise

High temperature behaviour of SiC devices – [1, 2]



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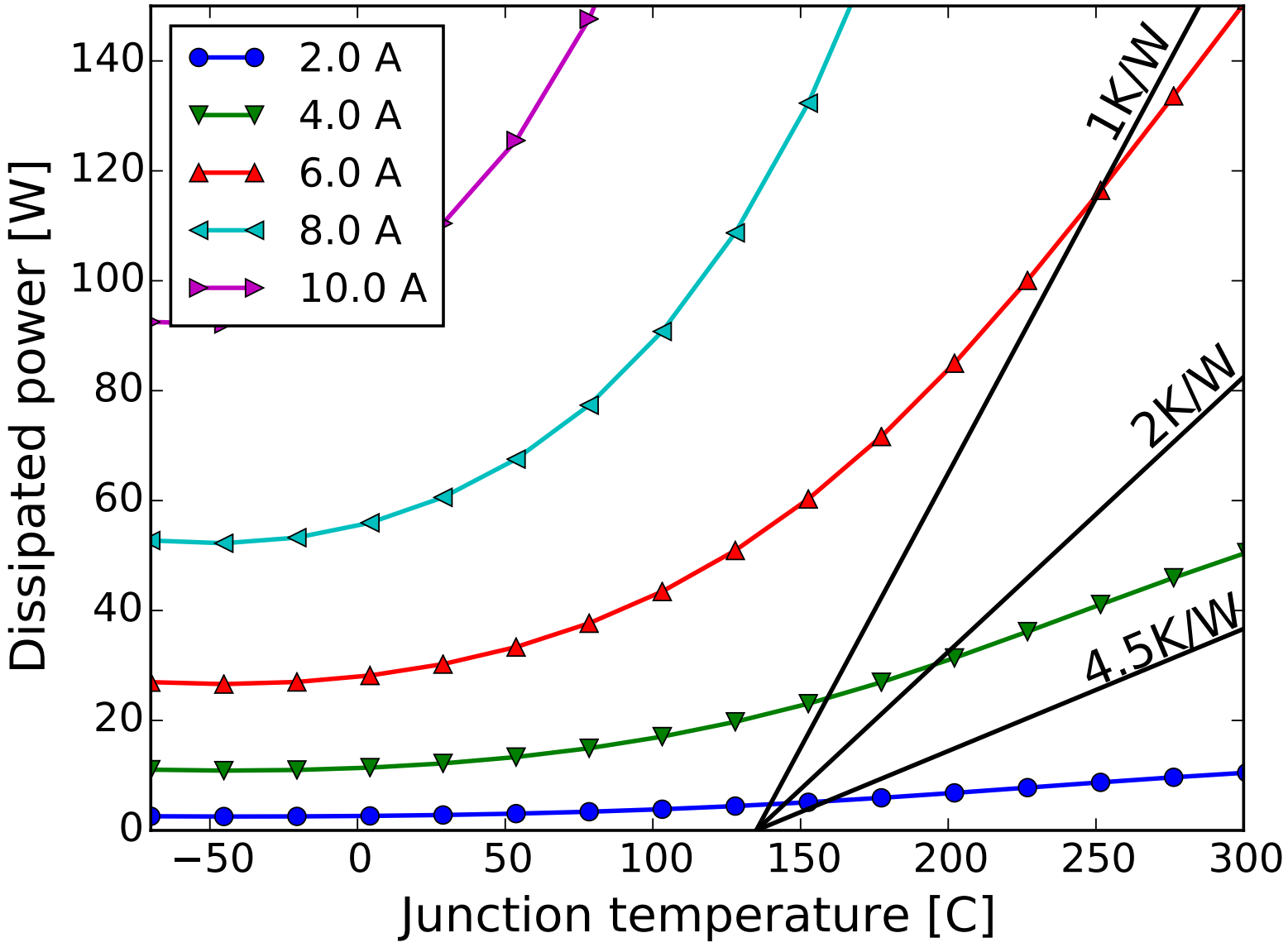
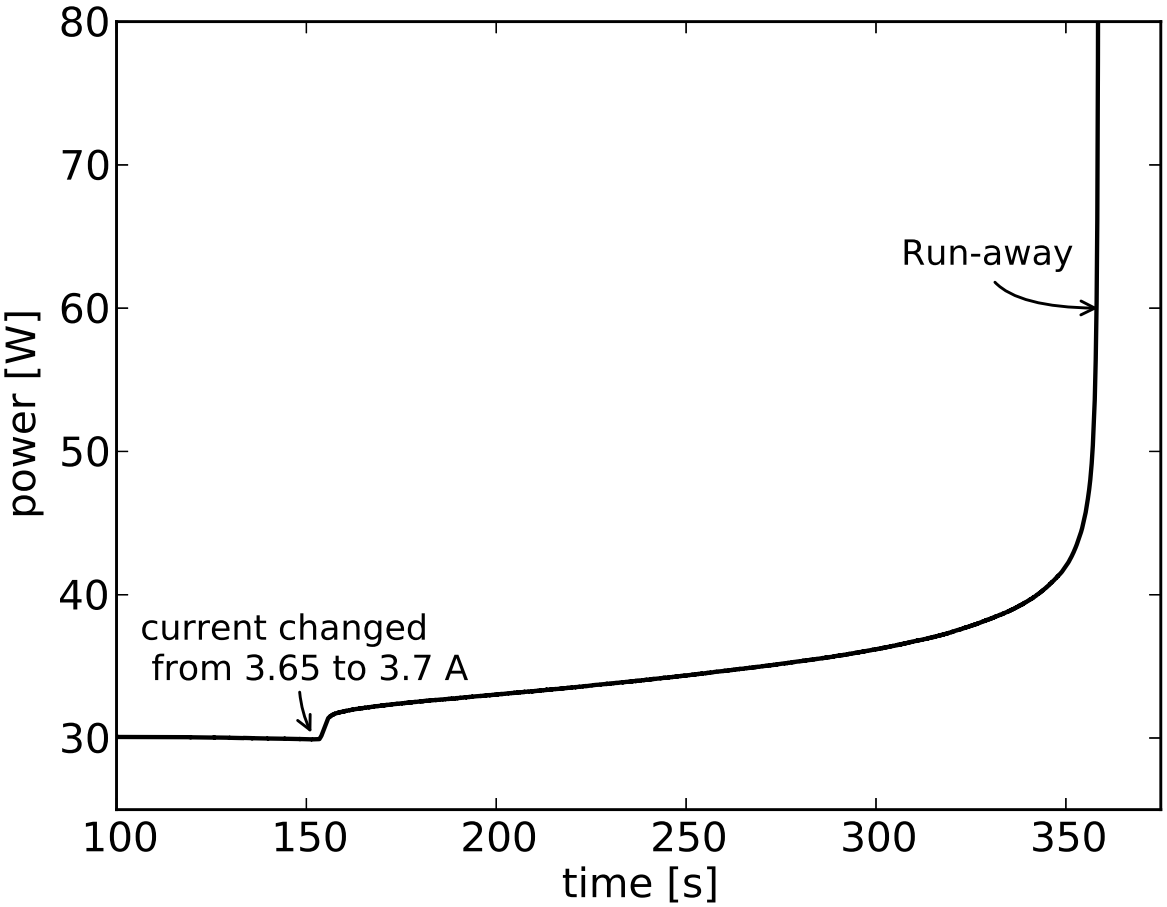


High temperature behaviour of SiC devices – [1, 2]

Buttay et al. “Thermal Stability of Silicon Carbide Power JFETs”, IEEE Trans on Electron Devices, 2014



SiC JFET:

- 490 mΩ, 1200 V
- $R_{Th_{JA}} = 4.5\ K/W$
- 135 °C ambient
- On-state losses

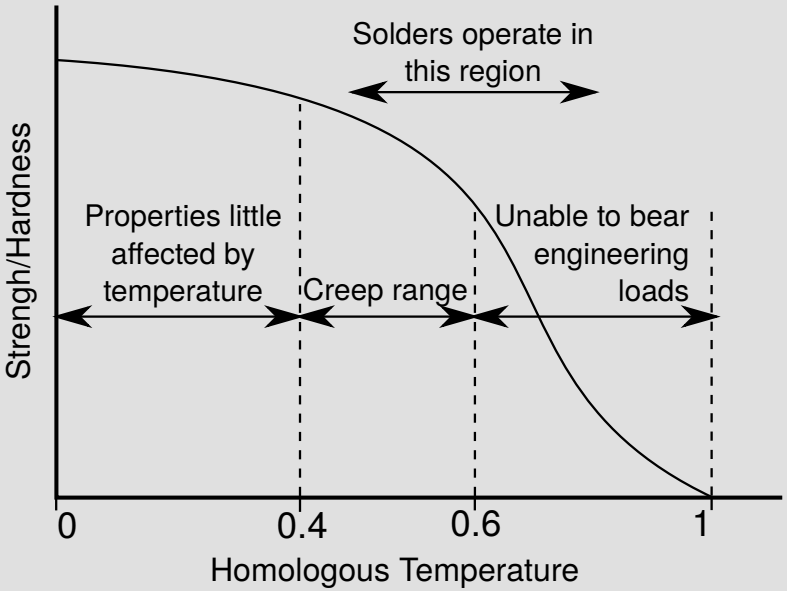
High temperature capability $\neq$ reduced cooling needs!

SiC JFETs must be attached to a low-R_{Th} cooling system.

Outline

High Temperature die attaches

The problem with solders



Source:
http://www.ami.ac.uk/courses/topics/0164_homt/

Homologous temperature:

$$T_H = \frac{T_{Oper}[K]}{T_{Melt}[K]}$$

Example:

- AuGe solder: T_{Melt} = 356°C = 629 K
- $T_H = 0.8 \rightarrow T_{Oper}$ = 503 K = 230 °C

- High temperature solder alloys not practical
- Need to decorrelate process temperature and melting point:
  - Sintering (solid state, process below melting point)
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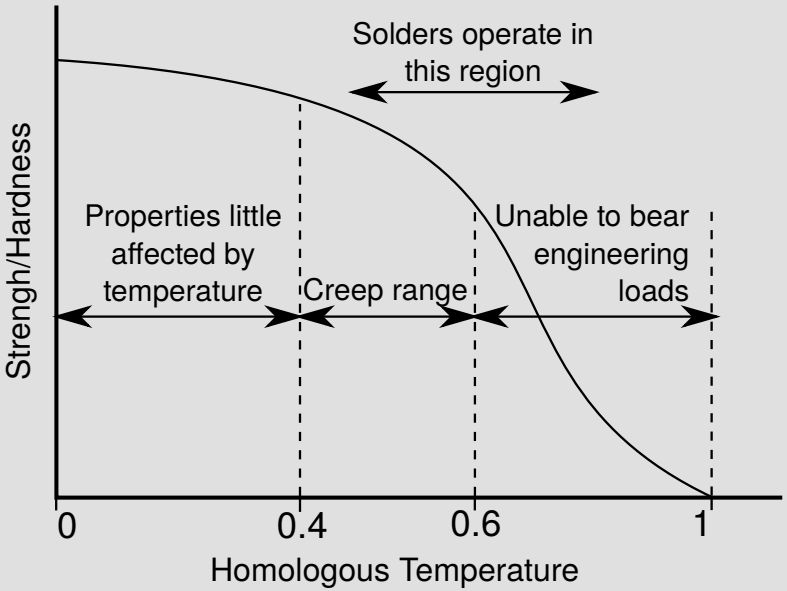

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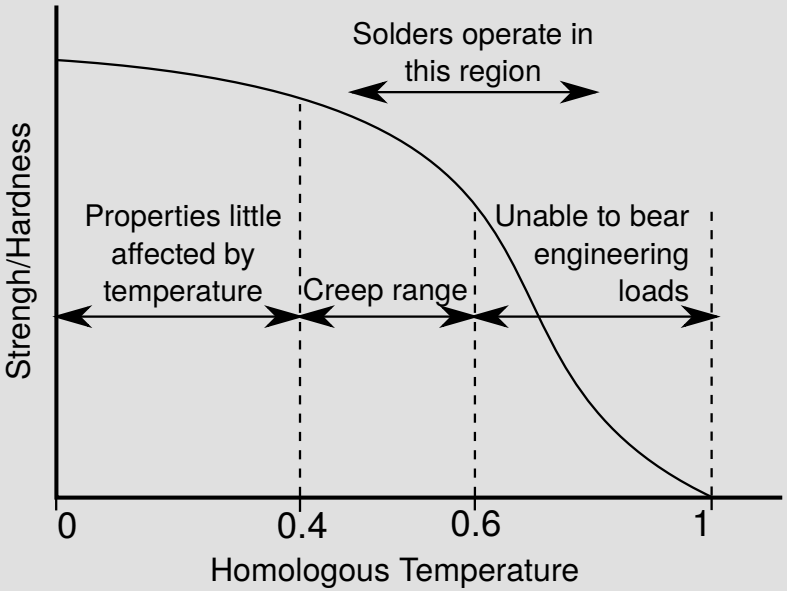

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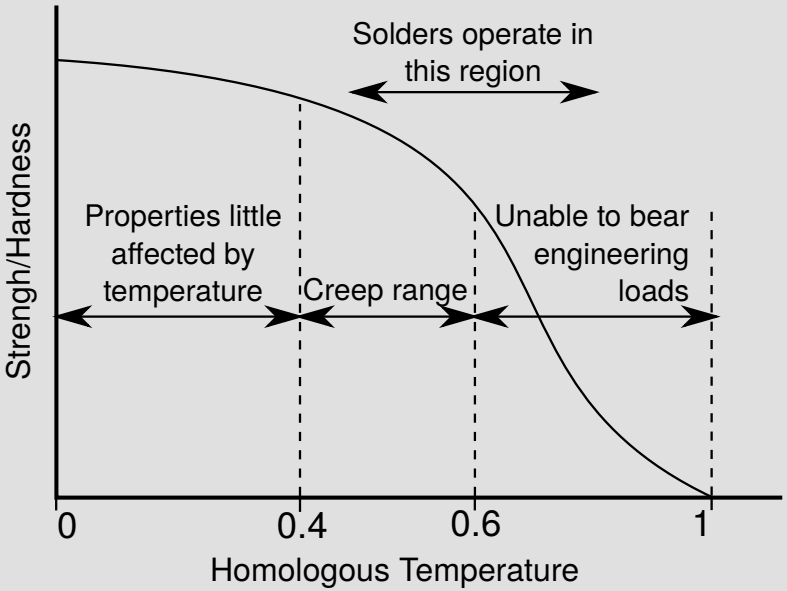

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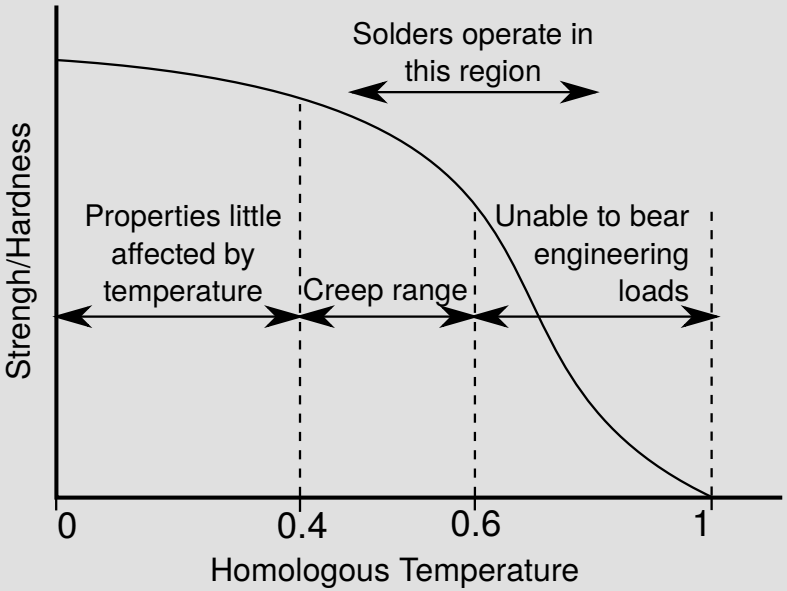

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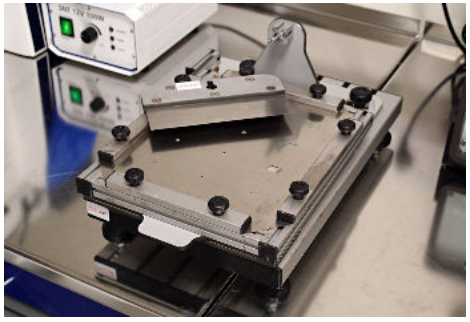
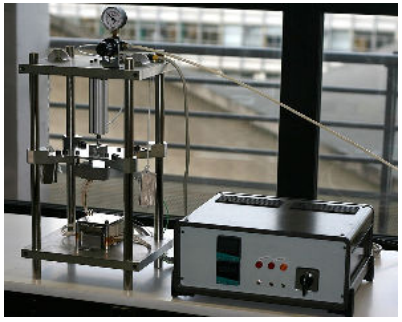
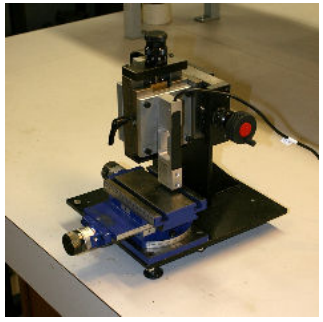
High Temperature Die Attaches – PhD A. Masson







- development of the sintering process
- Nano-particles paste from NBE Tech

- Evaluation of many parameters
  - Sintering pressure
  - Surface roughness
  - Thickness of stencil
  - Substrate finish...
- **Once set, process is robust**

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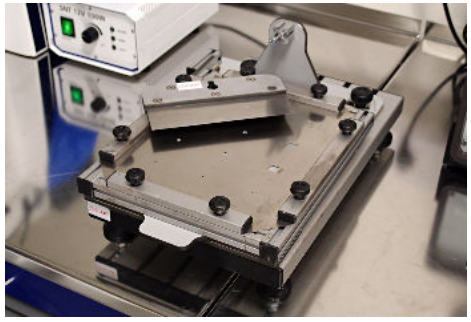

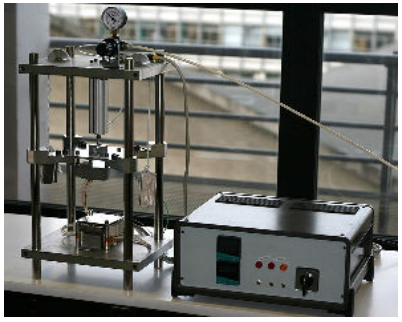

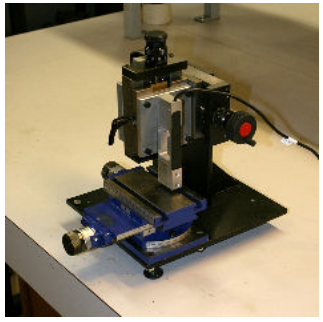

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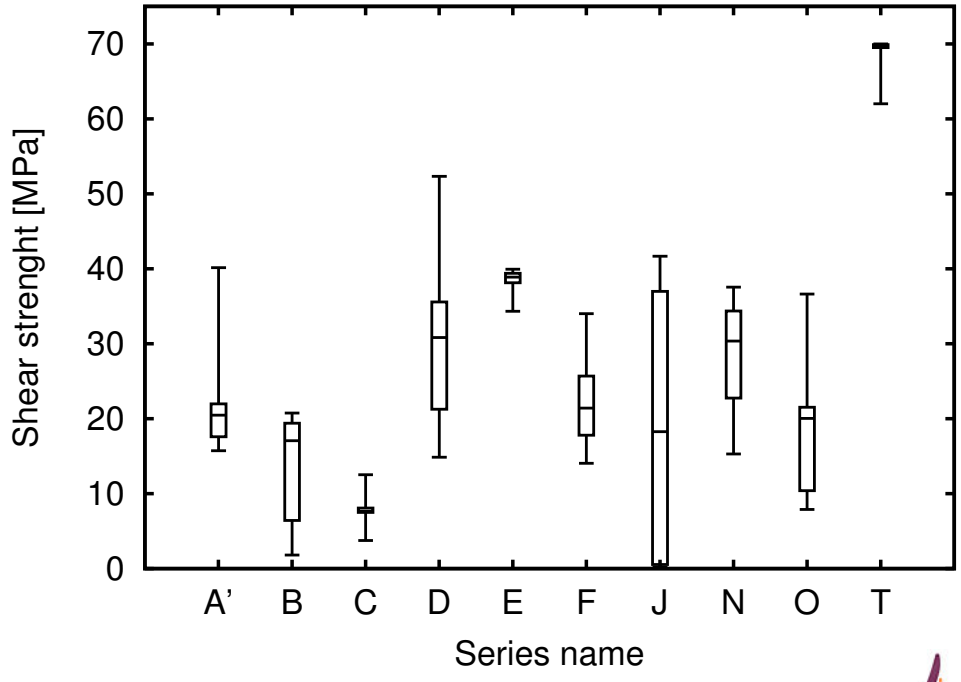

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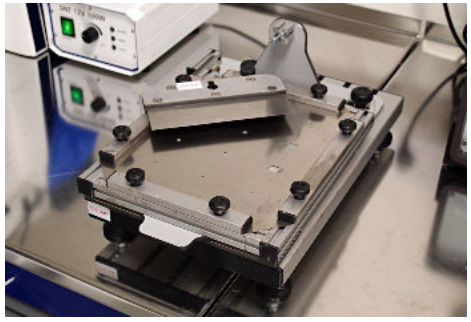

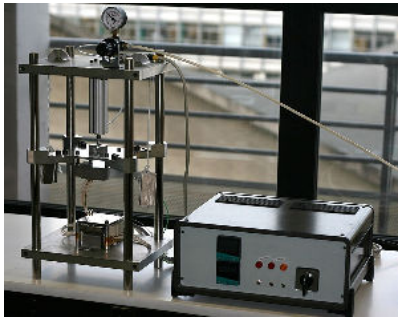

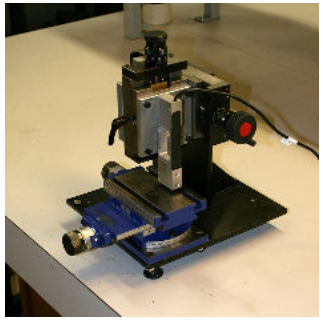

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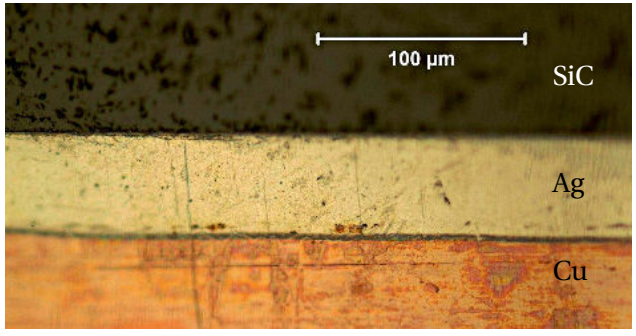
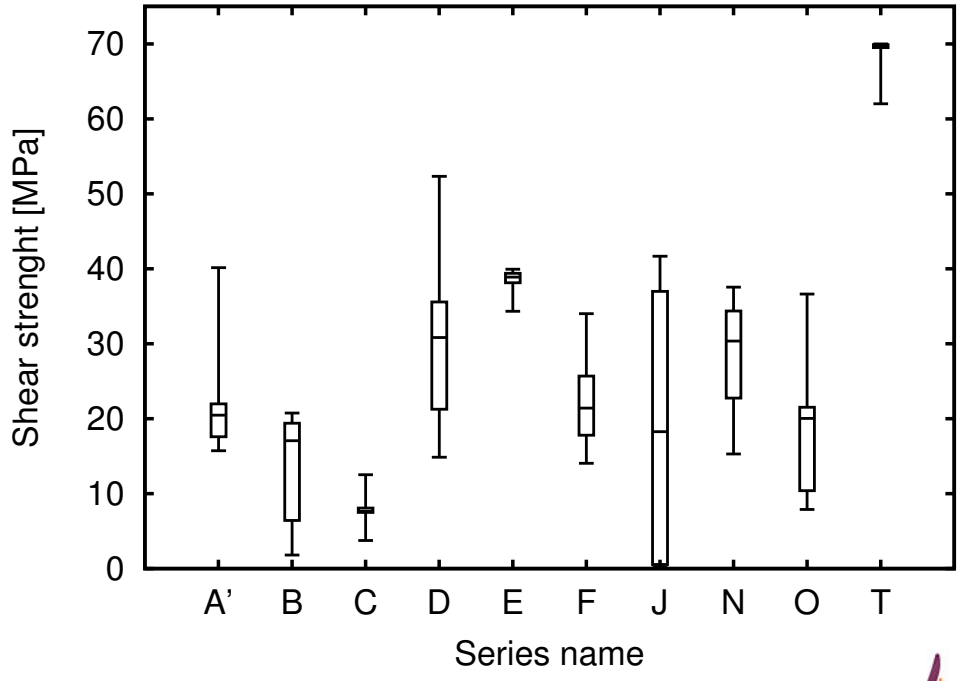
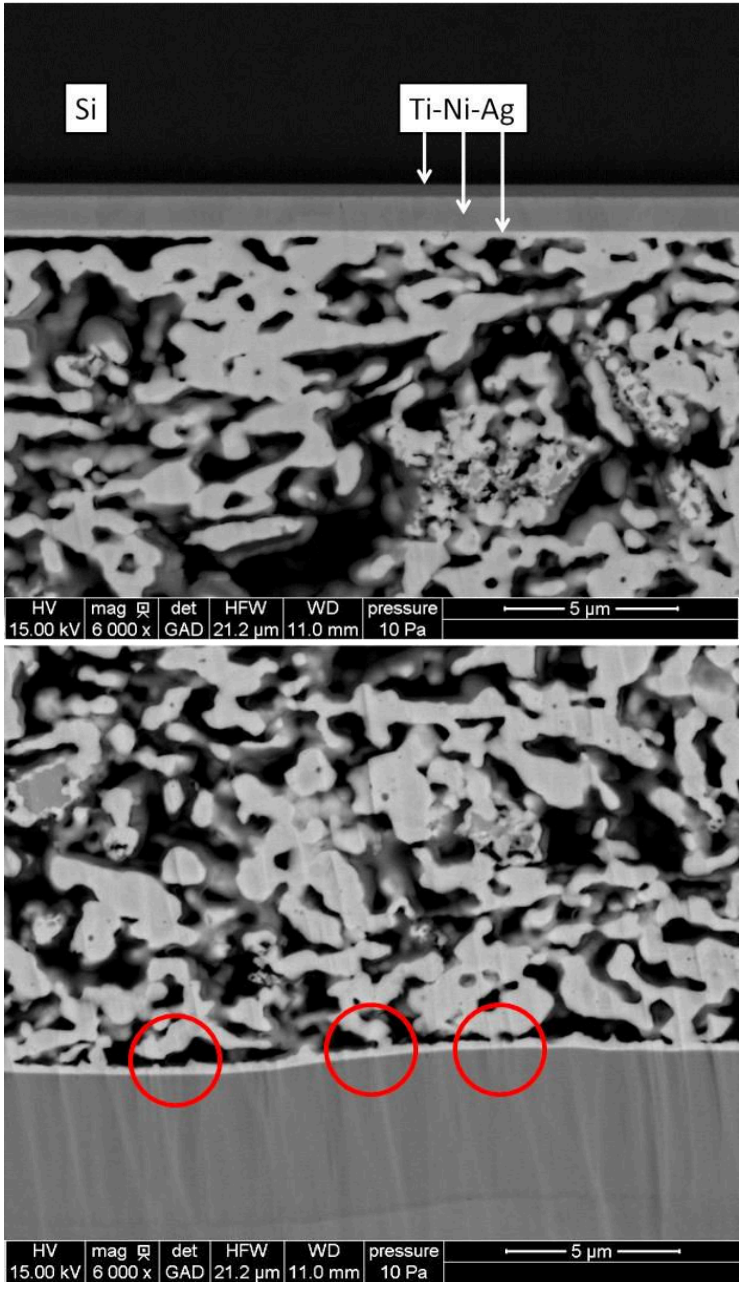


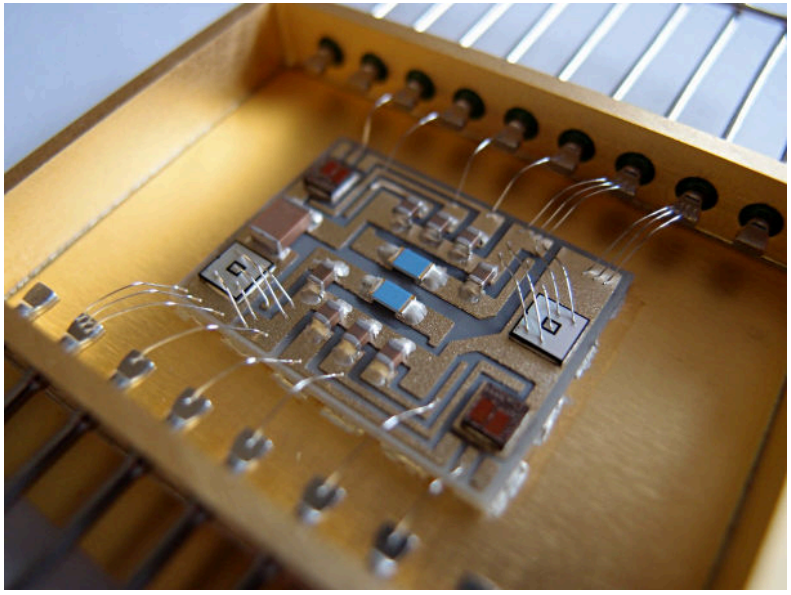


High Temperature Die Attaches – PhD S. HASCOËT

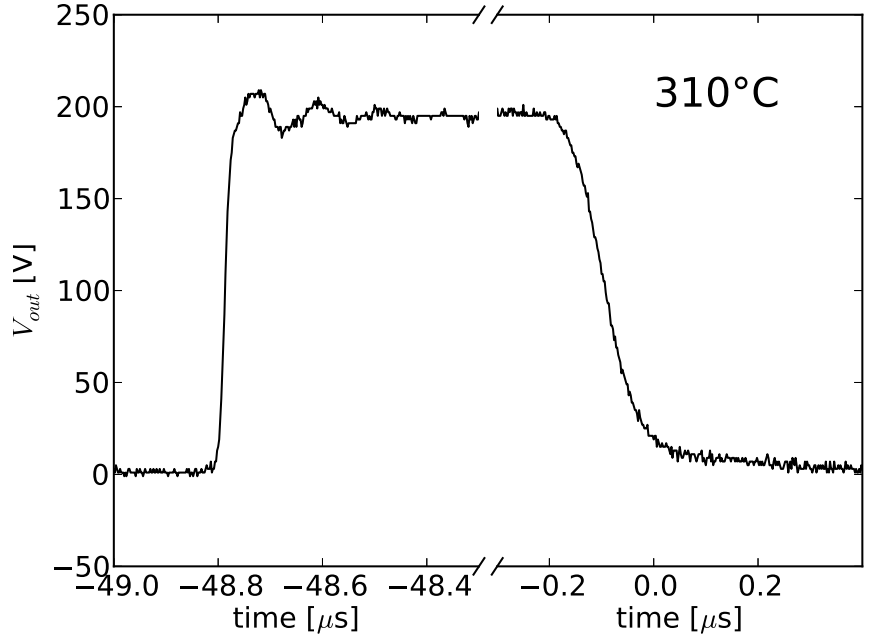


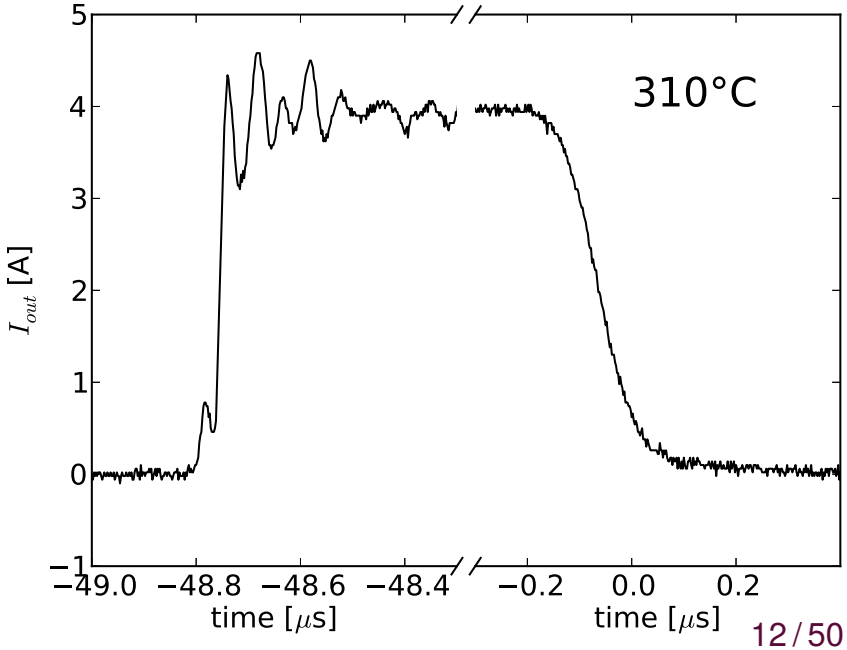
- "Pressureless" sintering process
- Based on micro-particles
- Findings:
  - Oxygen is necessary
  - Bonding on copper (oxide)
  - Standard Ni/Au finish not ideal
    - Confirmed by several teams
    - weak bonds at Ag/Au interface
  - Bond strength lower
  - Porosity higher
  - Can be used to attach fragile components

High Temperature Die Attaches – [3]

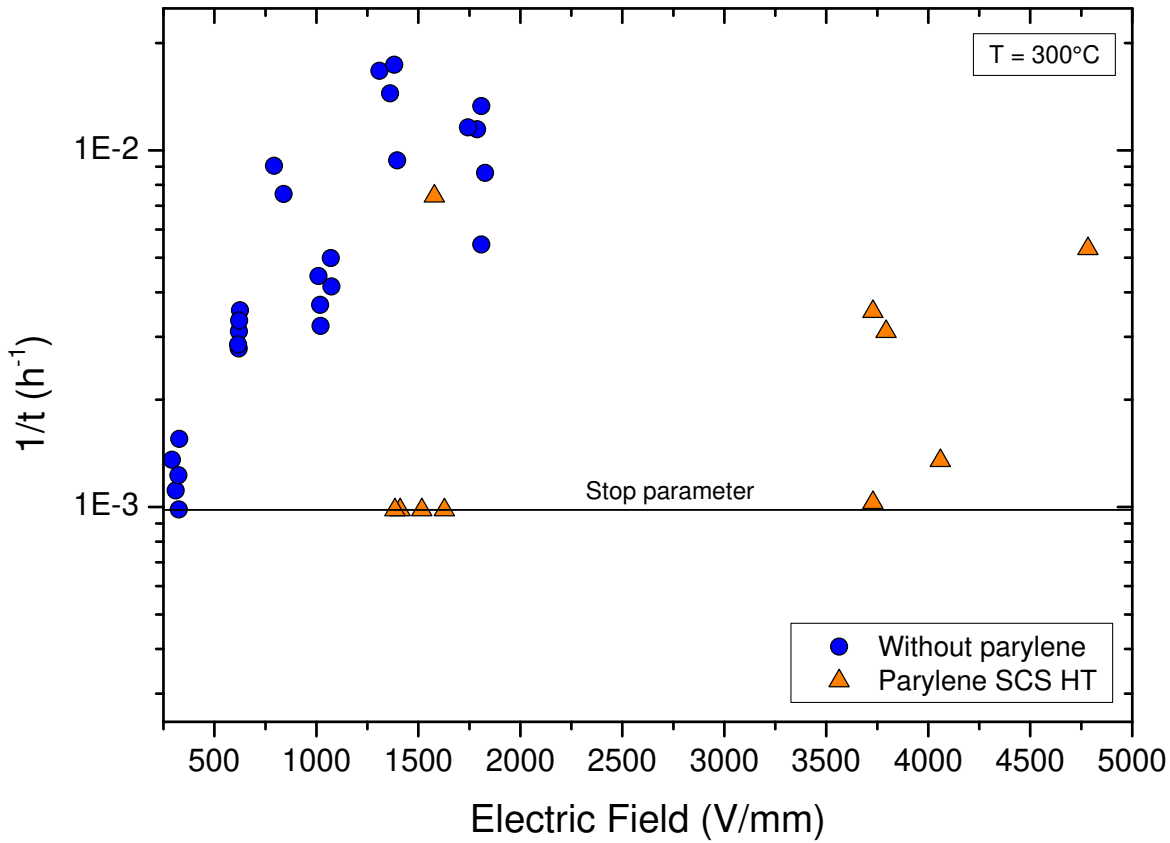


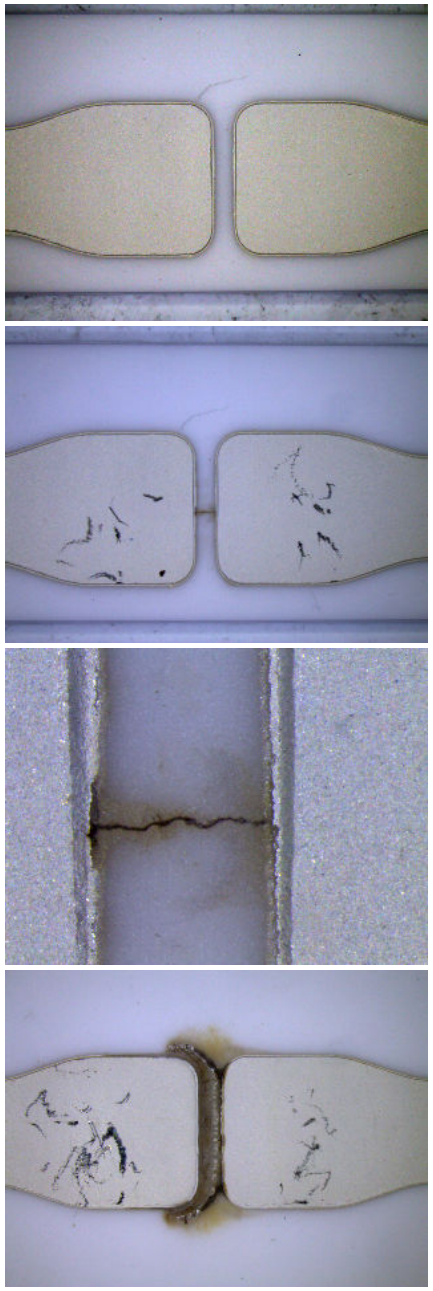
- All-sintered assembly
- Half-Bridge structure
- SiC JFETs
- Integrated gate drivers (Ampère)
- Ceramic capacitors
- Isolation function not integrated





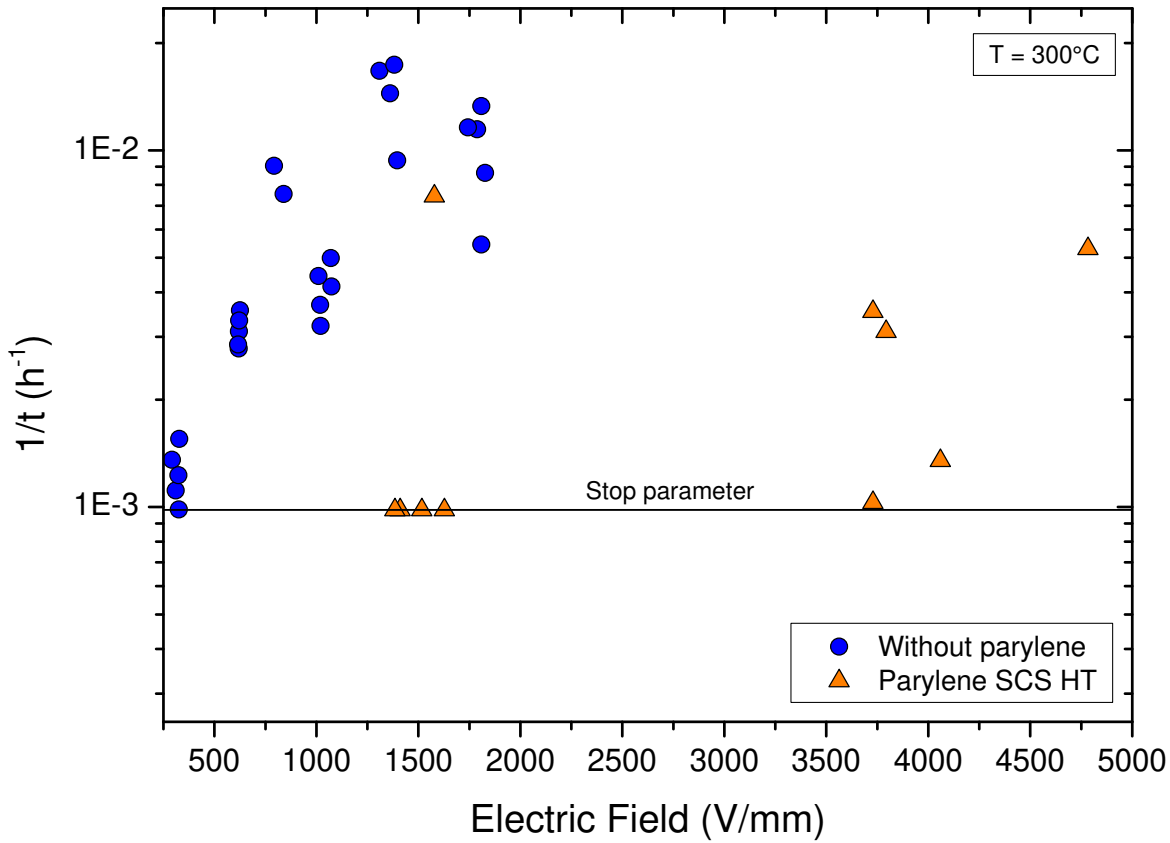
High Temperature Die Attaches – Silver migration, R. Riva [4]

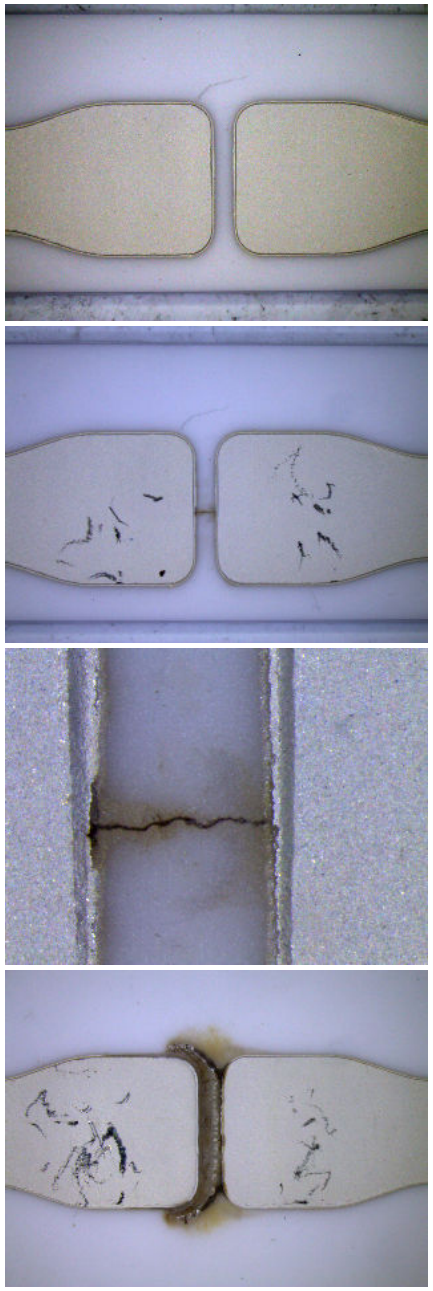




- Causes: electric field, high temperature and oxygen
- Large differences between similar test vehicles:
- **Short life without encapsulation** (100–1000 h)
- **Much longer life with parylene HT protection**

High Temperature Die Attaches – Silver migration, R. Riva [4]





- Causes: electric field, high temperature and oxygen
- Large differences between similar test vehicles:
- **Short life without encapsulation** (100–1000 h)
- **Much longer life with parylene HT protection**

Conclusion on Packaging for High Temperature

SiC devices can operate at high temperature (>300 °C)

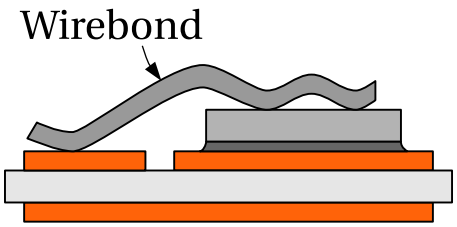
- With efficient thermal management!
- R_{Th} must remain low

Silver sintering for high temperature die attaches

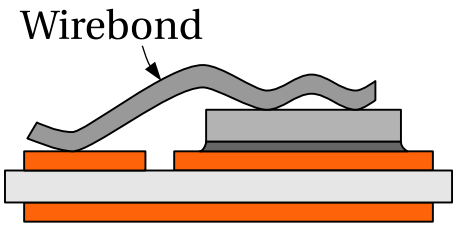
- Compatible with standard die finishes
- High thermal/electrical performance
- **Research:** long-term behaviour at elevated temperature
  - pressureless processes may be a good model
  - not presented here: cycling and storage tests [5, 6, 7]

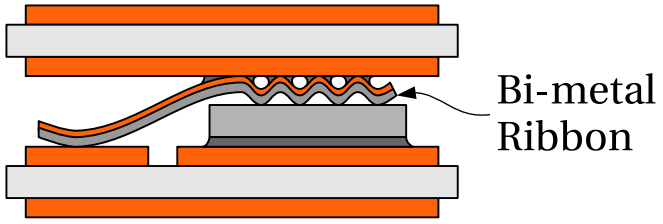
Outline

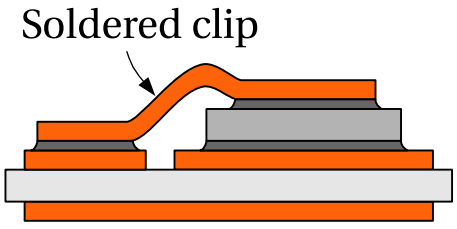
New Structures

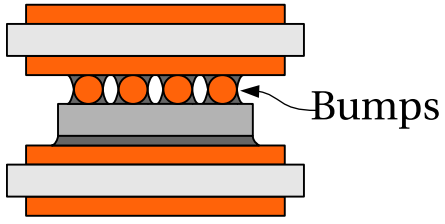


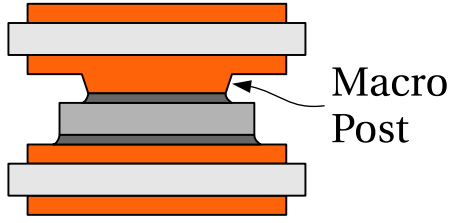
New Structures

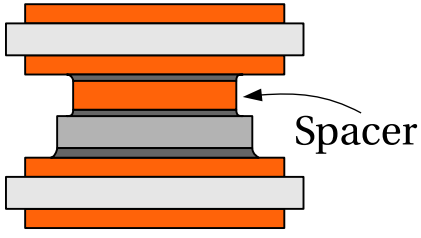


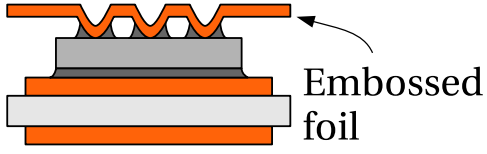


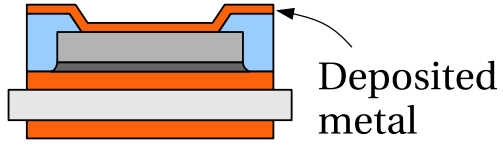


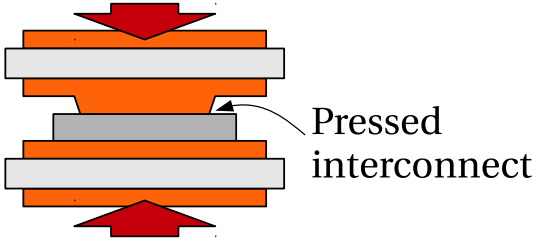


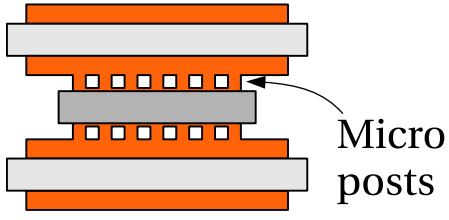


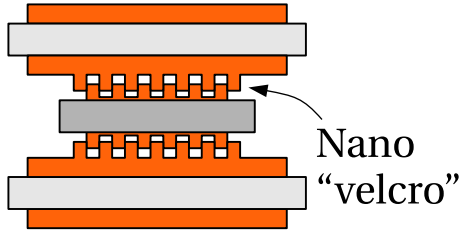




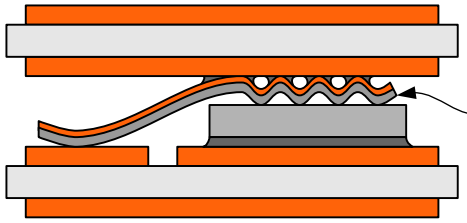


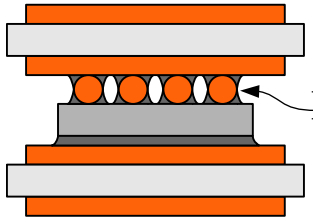


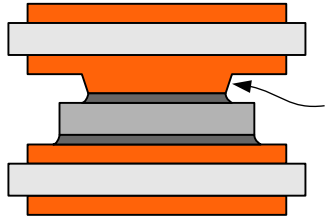


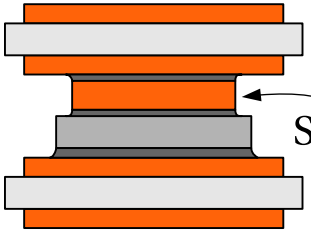


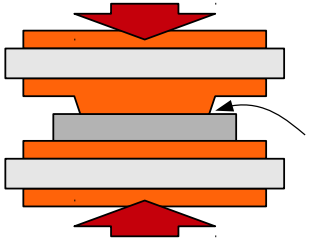
New Structures – for double-side cooling

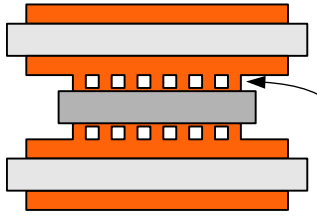


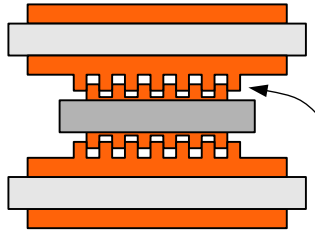




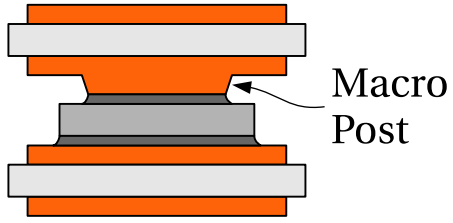


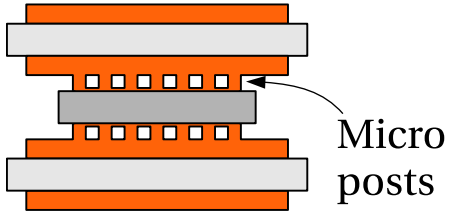






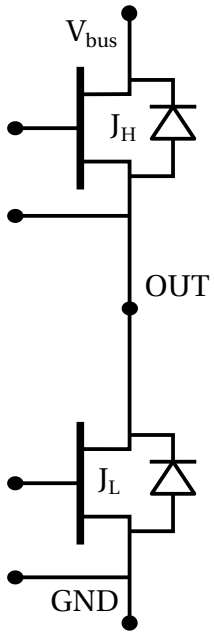
New Structures – for double-side cooling – investigated here

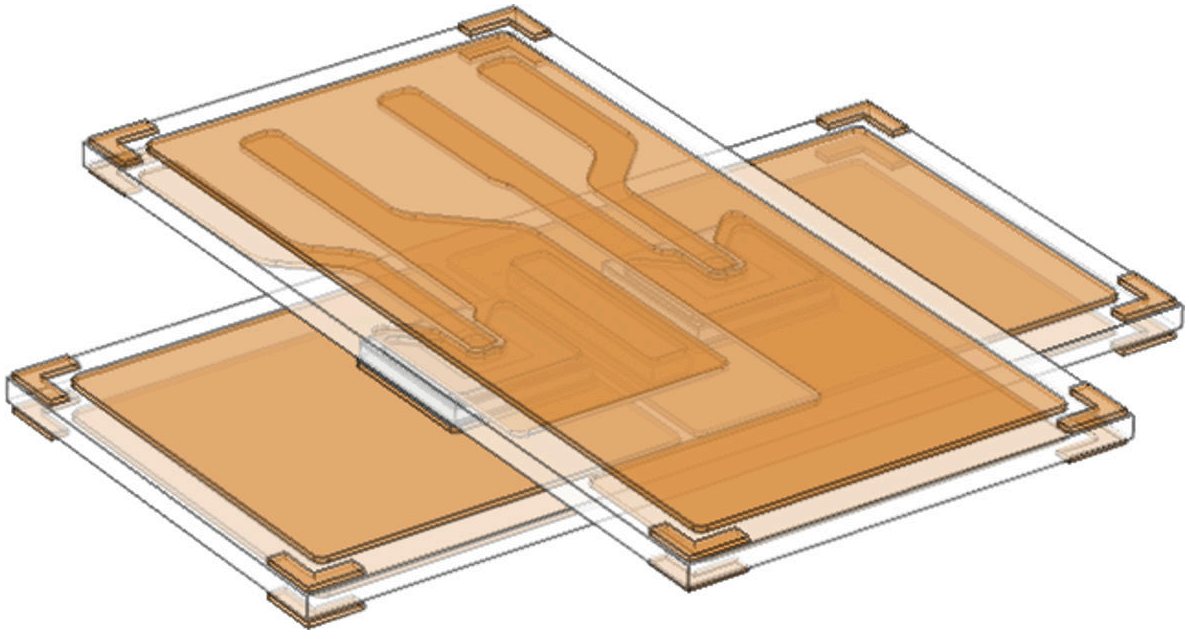




Outline

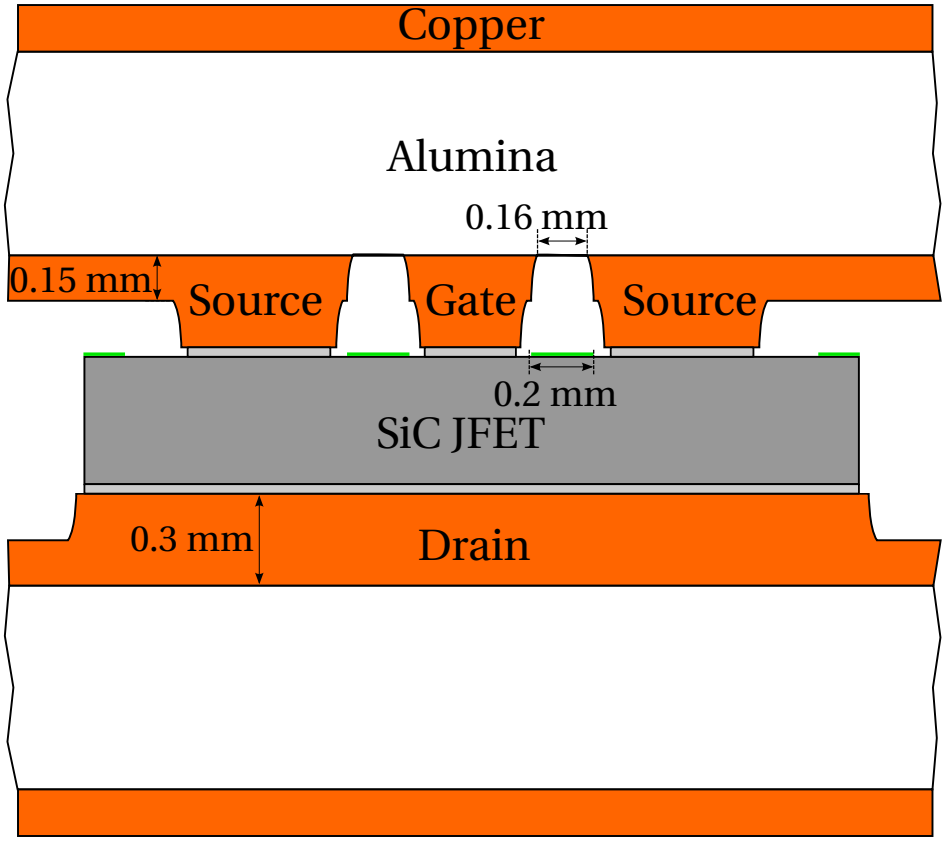
New Structures – Macro post (R Riva) [8, 9]





- Two ceramic substrates, in “sandwich” configuration
- Two SiC JFET dies (SiCED)
- assembled using silver sintering
- 25.4 mm$\times$12.7 mm (1 in$\times$0.5 in)

New Structures – Macro post (R Riva) [8, 9]

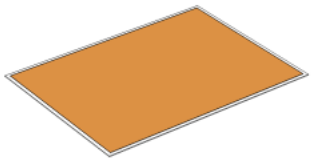


Scale drawing for 2.4×2.4 mm^2 die

- Etching accuracy exceeds standard design rules
- Double-step copper etching for die contact

➜ Custom etching technique

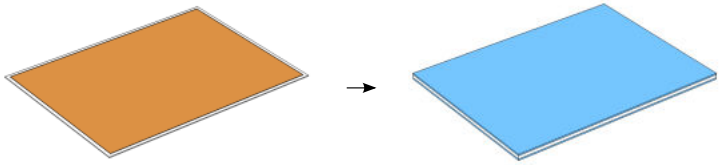
New Structures – Macro post (R Riva) [8, 9]



plain DBC board

- Final patterns within 50 μm of desired size
- Two designs, for 2.4 mm and 4 mm dies
  - Die top metallized (PVD) with Ti/Ag
- Total copper thickness 300 μm,
  $\approx$ 150 μm per step

New Structures – Macro post (R Riva) [8, 9]



plain DBC board

1a - Photosensitive resin coating

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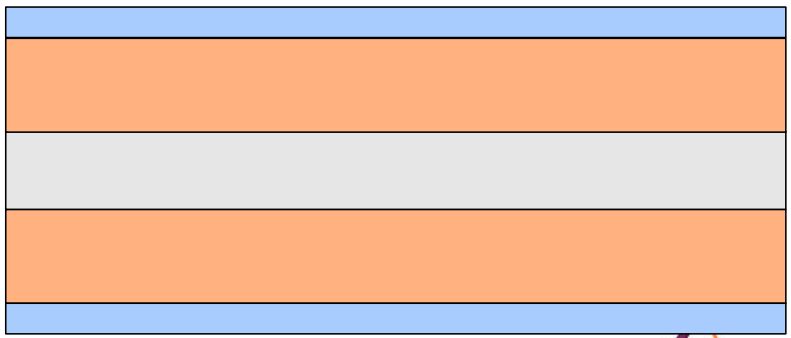

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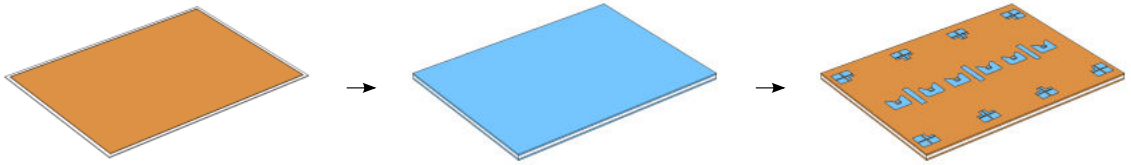

plain DBC board

1a - Photosensitive resin coating

1b - Exposure and Development

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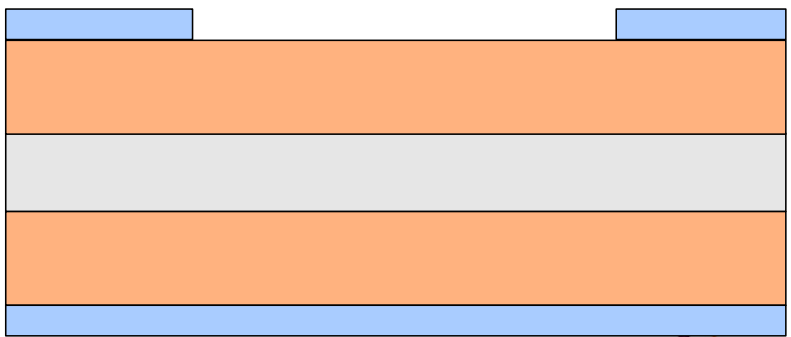

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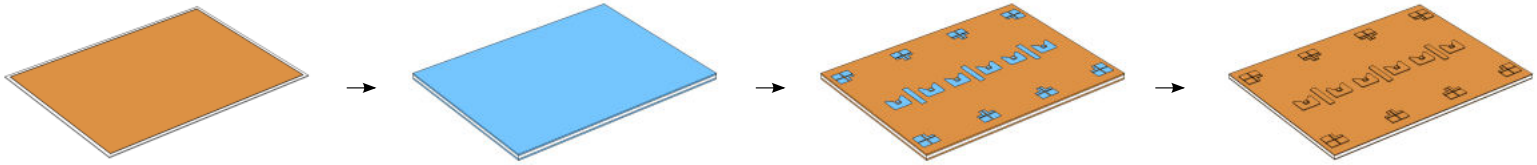

plain DBC board

1a - Photosensitive resin coating

1b - Exposure and Development

2 - Etching

- Final patterns within 50 μm of desired size
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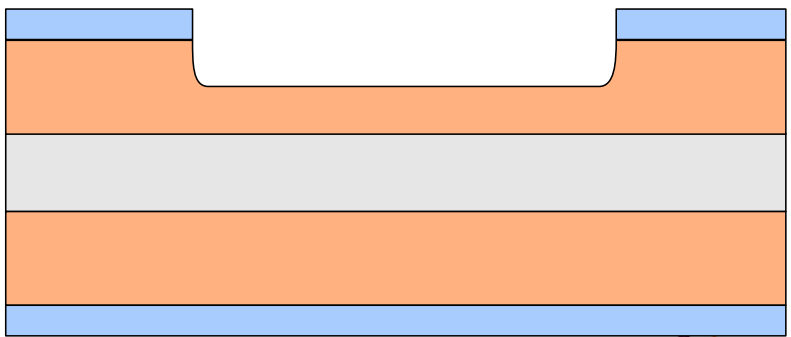

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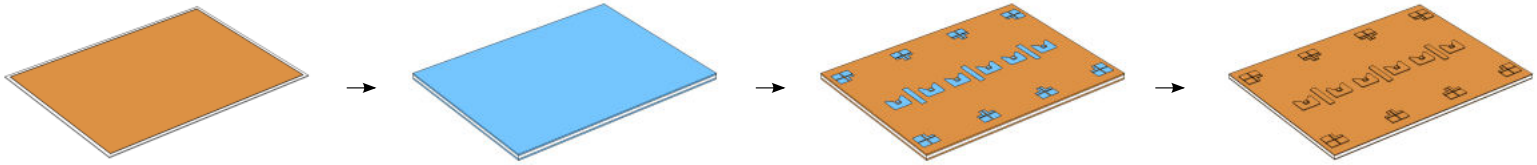

plain DBC board

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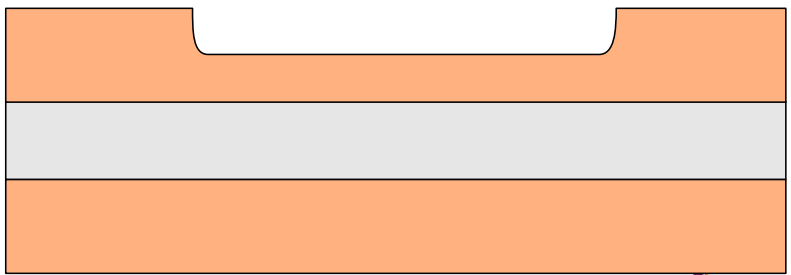
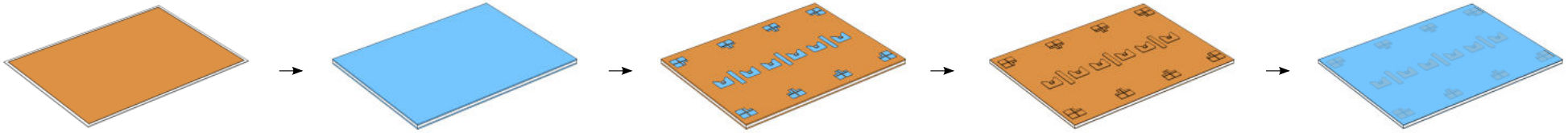


New Structures – Macro post (R Riva) [8, 9]



plain DBC board

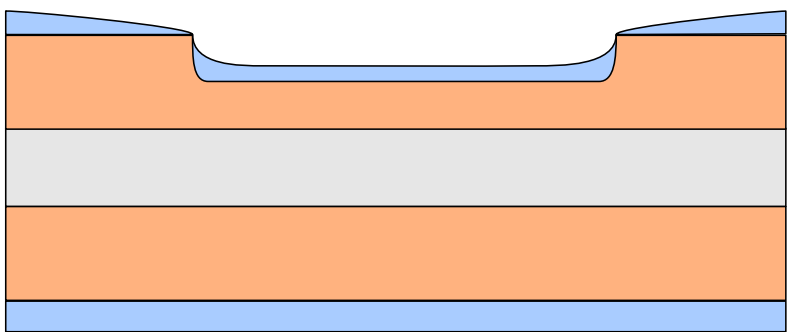
1a - Photosensitive resin coating

1b - Exposure and Development

2 - Etching

3a - resin coating

- Final patterns within 50 μm of desired size
- Two designs, for 2.4 mm and 4 mm dies
  - Die top metallized (PVD) with Ti/Ag
- Total copper thickness 300 μm, $\approx$ 150 μm per step



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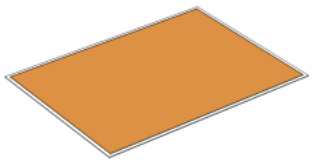
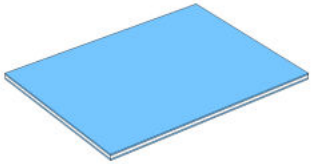
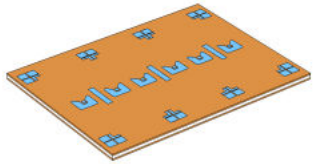


plain DBC board

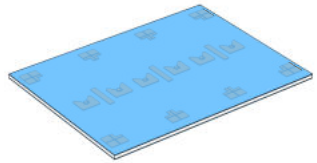


1a - Photosensitive resin coating

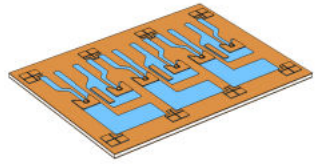


1b - Exposure and Development

2 - Etching

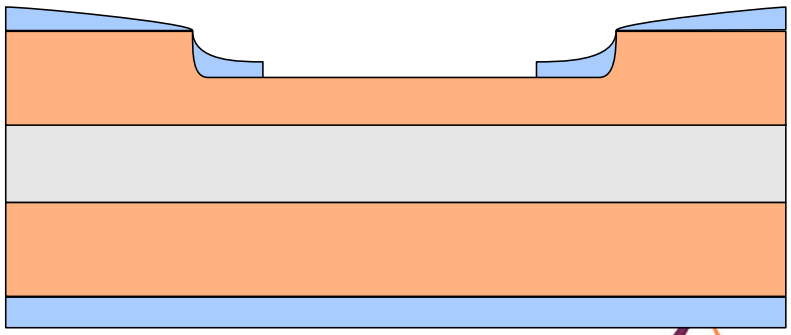


3a - resin coating

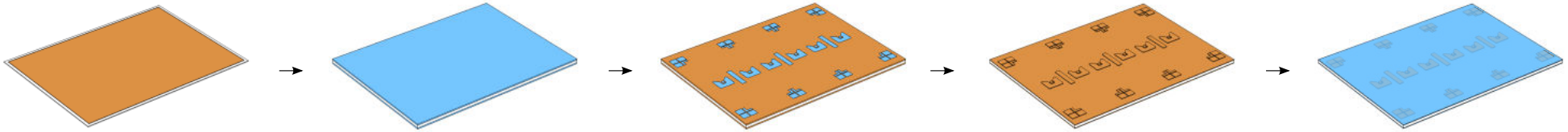


3b - Exposure and Developpment

- Final patterns within 50 μm of desired size
- Two designs, for 2.4 mm and 4 mm dies
  - Die top metallized (PVD) with Ti/Ag
- Total copper thickness 300 μm, $\approx$ 150 μm per step



New Structures – Macro post (R Riva) [8, 9]



plain DBC board

1a - Photosensitive resin coating

1b - Exposure and Development

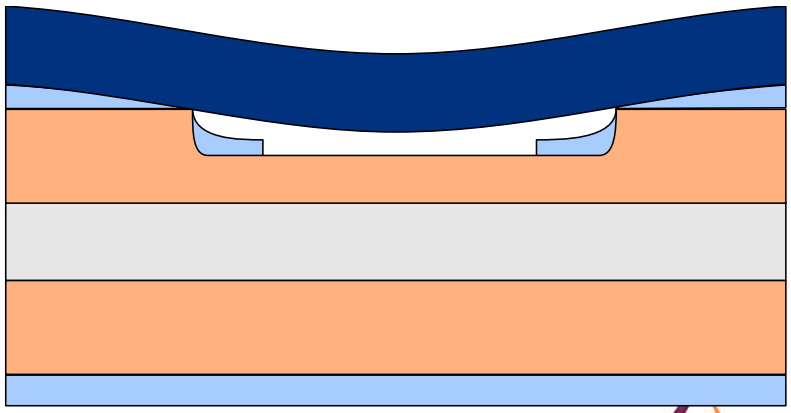
2 - Etching

3a - resin coating

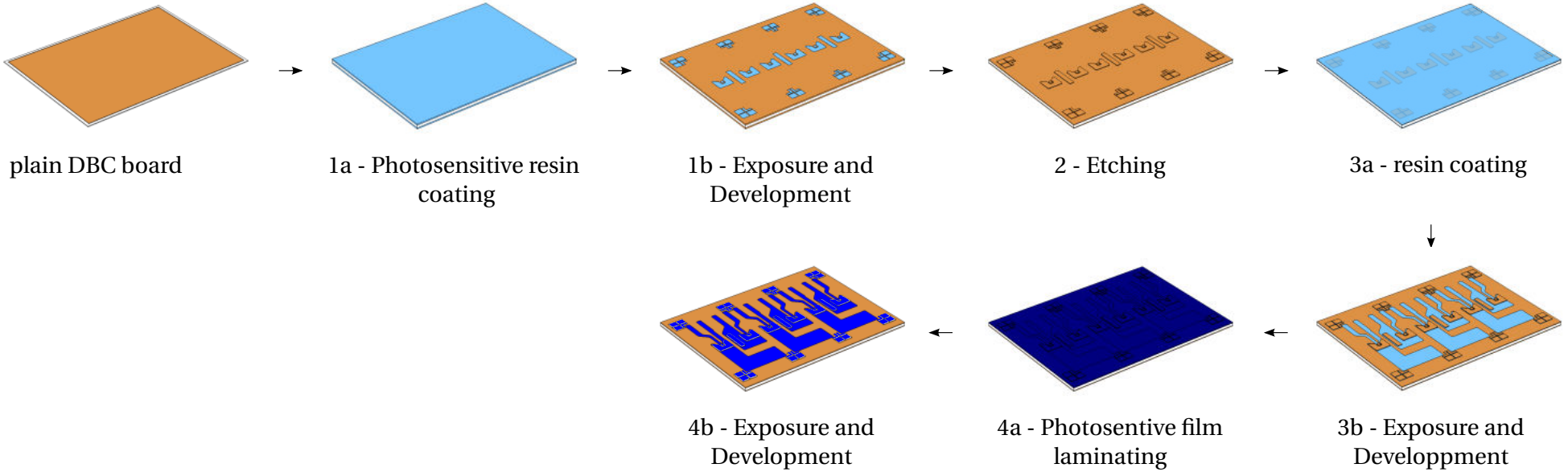
3b - Exposure and Developpment

4a - Photosentive film laminating

- Final patterns within 50 μm of desired size
- Two designs, for 2.4 mm and 4 mm dies
  - Die top metallized (PVD) with Ti/Ag
- Total copper thickness 300 μm, $\approx$ 150 μm per step



New Structures – Macro post (R Riva) [8, 9]



- Final patterns within 50 μm of desired size
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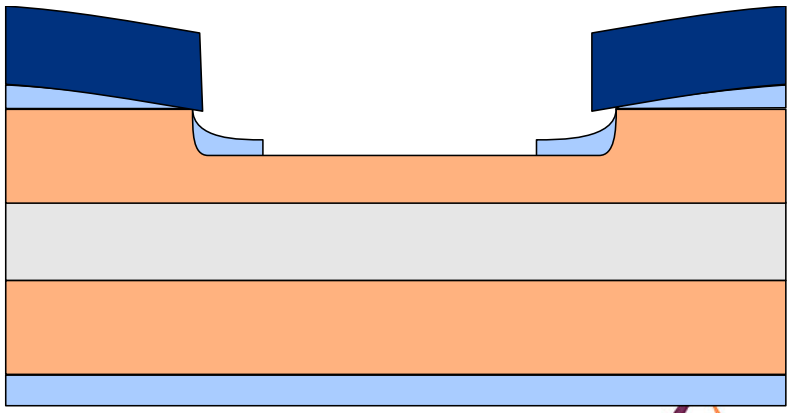
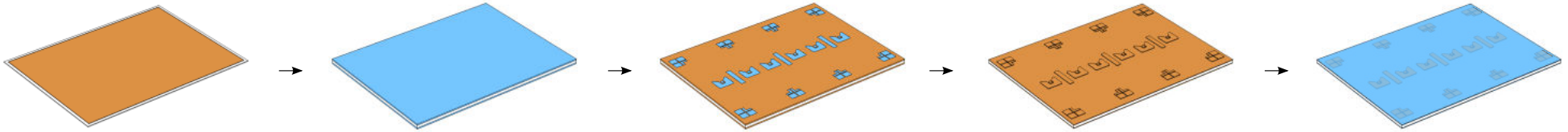
  - Die top metallized (PVD) with Ti/Ag
- Total copper thickness 300 μm, $\approx$ 150 μm per step



New Structures – Macro post (R Riva) [8, 9]



plain DBC board

1a - Photosensitive resin coating

1b - Exposure and Development

2 - Etching

3a - resin coating

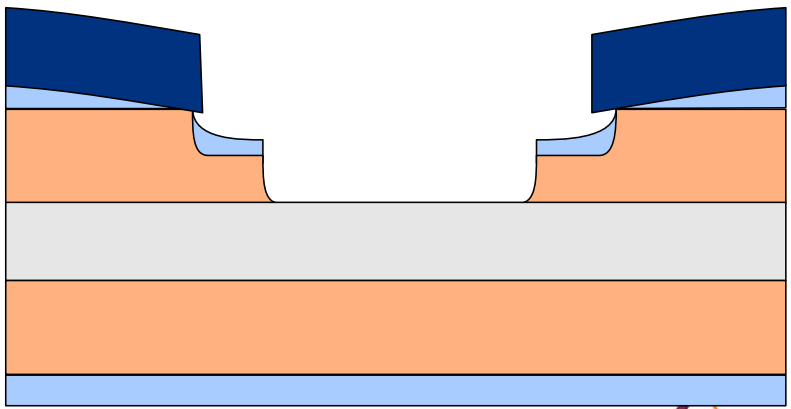
3b - Exposure and Developpment

4a - Photosentive film laminating

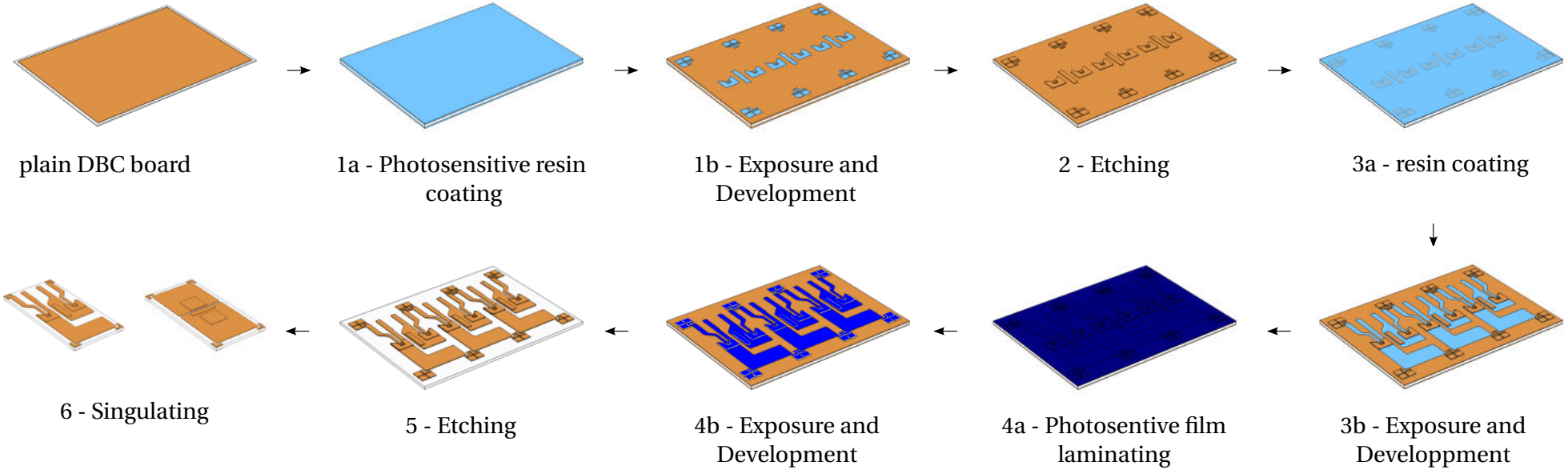
4b - Exposure and Development

5 - Etching

- Final patterns within 50 μm of desired size
- Two designs, for 2.4 mm and 4 mm dies
  - Die top metallized (PVD) with Ti/Ag
- Total copper thickness 300 μm, $\approx$ 150 μm per step



New Structures – Macro post (R Riva) [8, 9]



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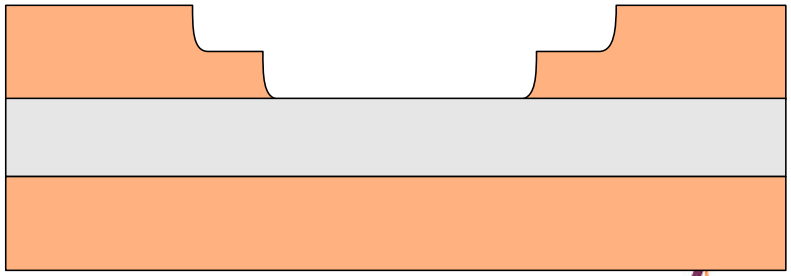

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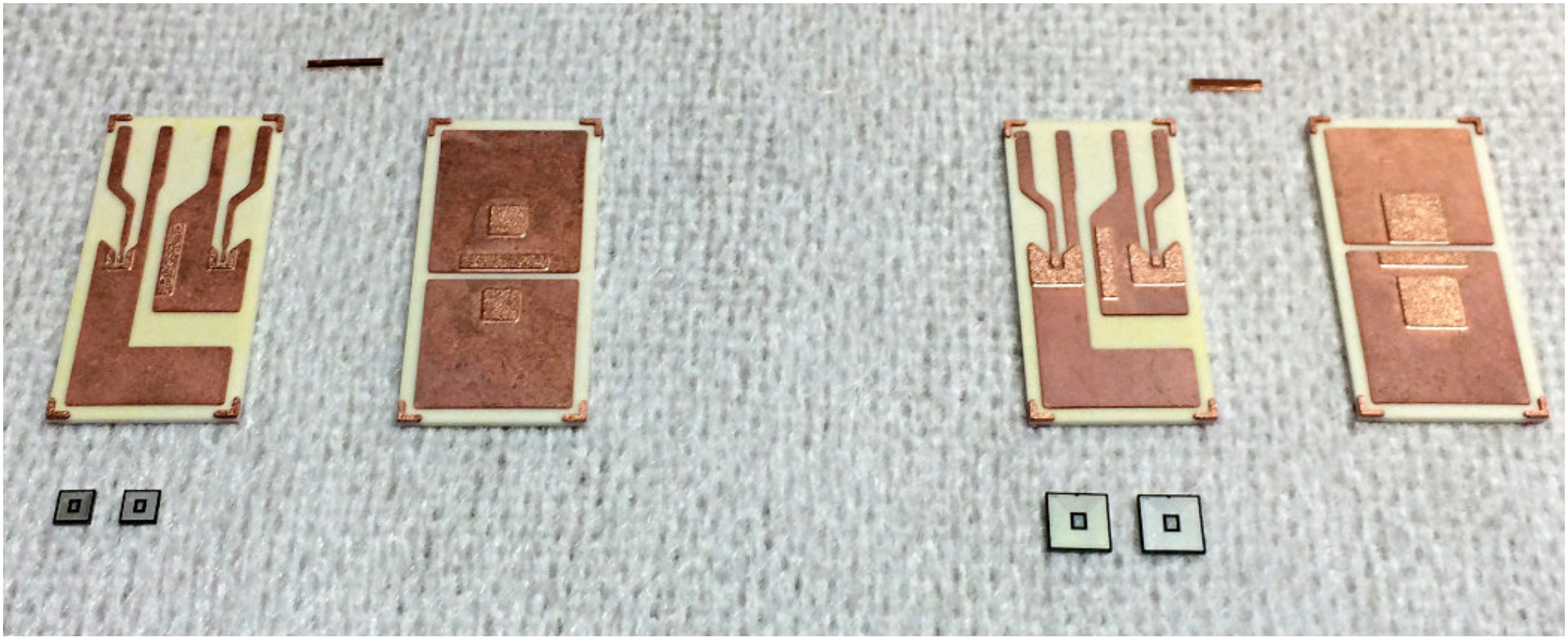

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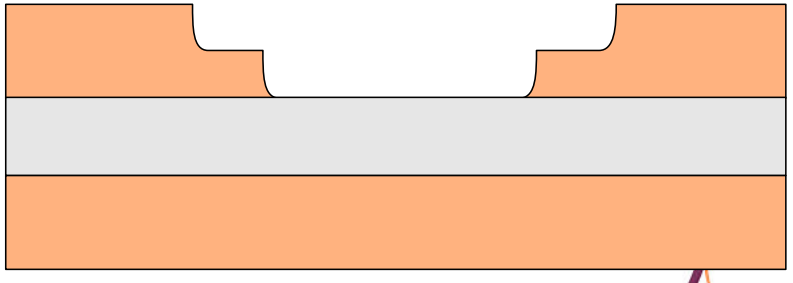

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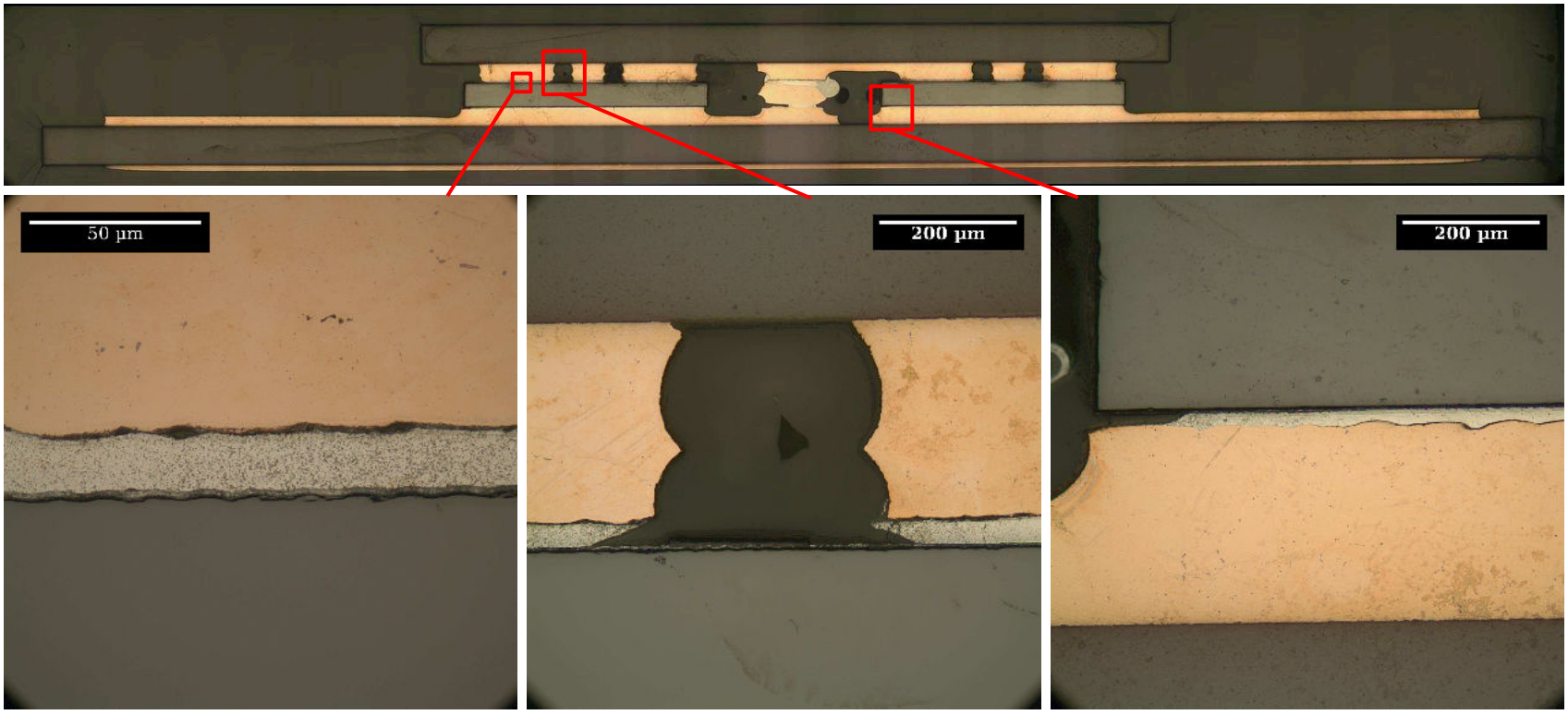
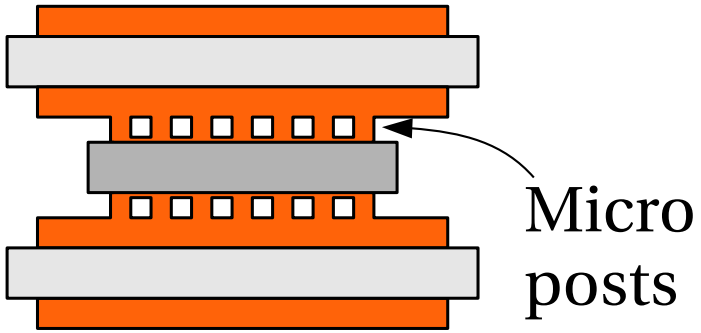


- Good form factor achieved using the two-step copper etching process
- Satisfying alignment
- Poor quality of Al-Cu attach

Outline

New Structures – Micro posts (B Mouawad) [10, 11]



- First studies during L. Ménager's PhD
  - Copper posts growth on die (electroplating)
  - Original die/DBC assembly technology: SnCu diffusion bonding
- Proposition of M. Soueidan: **direct copper bonding**

New Packaging Structures – Micro posts

(B Mouawad) [10, 11]

Direct Copper-to-Copper Bonding [12]

Parameters:

- SPS press
- Cu/Cu bonding
- 5 or 20 min
- 200 or 300°C
- 16 or 77 MPa

- **Very good bond**, without any interface material
  - All configuration but one yield to bonding
  - Tensile strenght 106 to 261 MPa (365 MPa for bulk copper)
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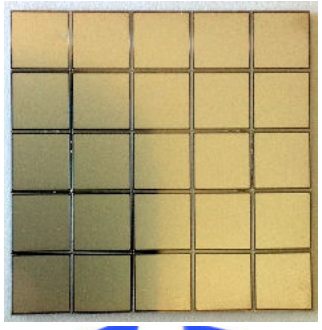
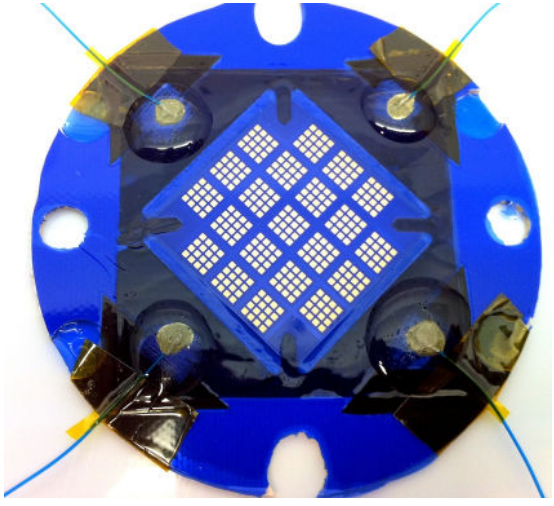
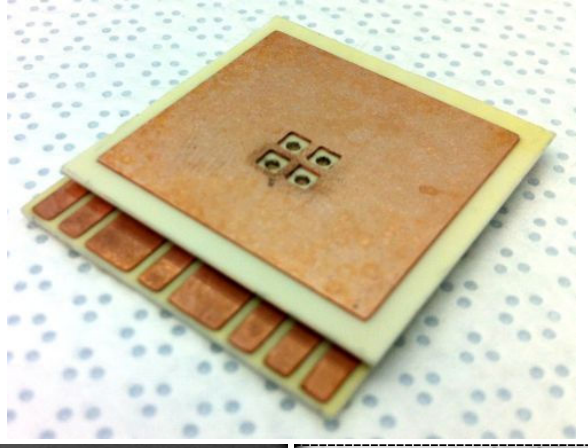
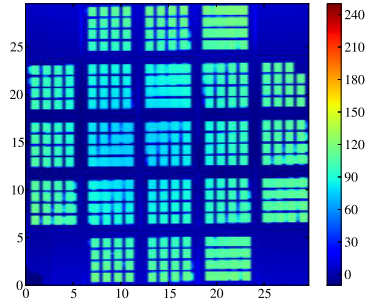
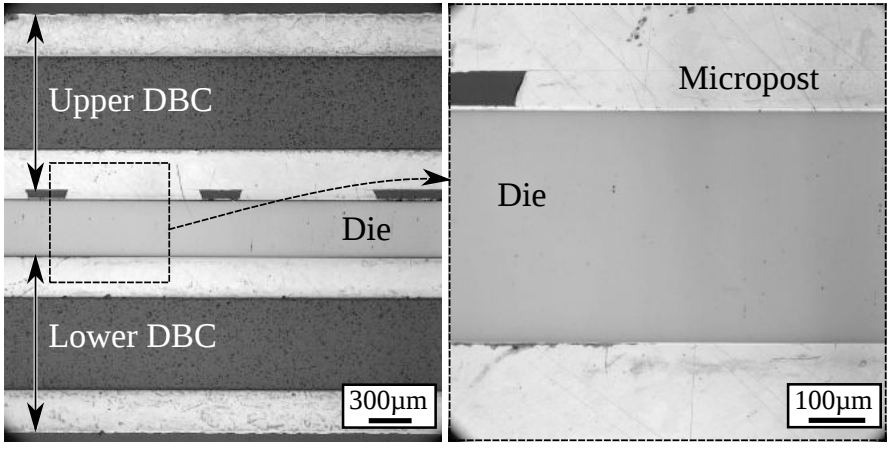


- "Wafer"-level process
- Based on copper electroplating
- Assembly of DBC/die/DBC "sandwiches"
- No damage to dies observed









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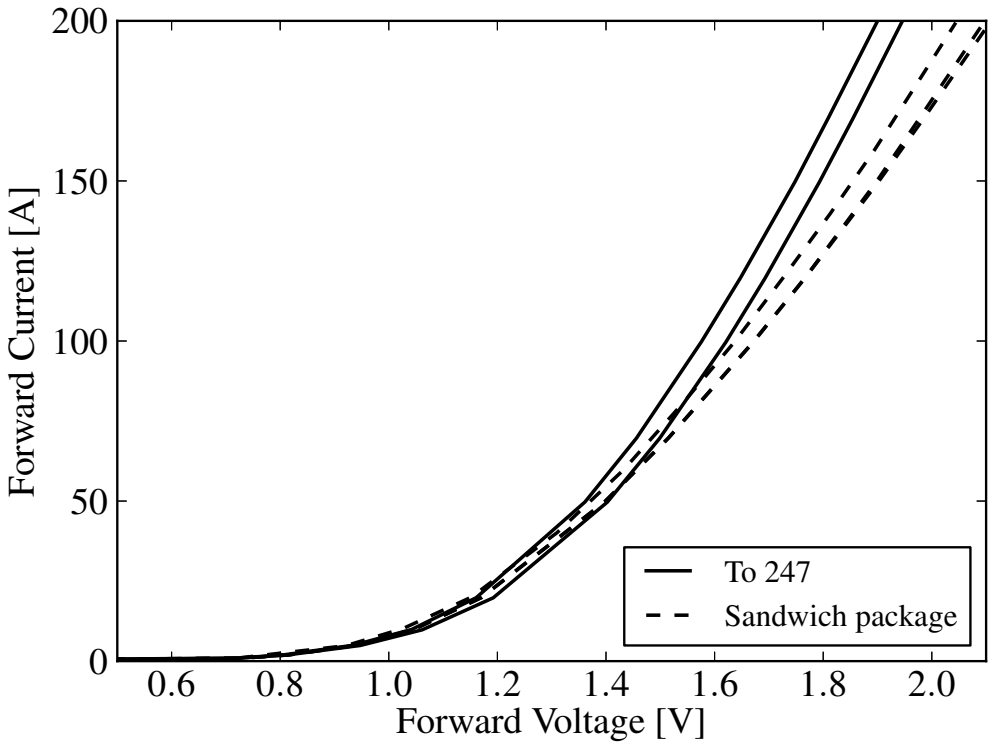
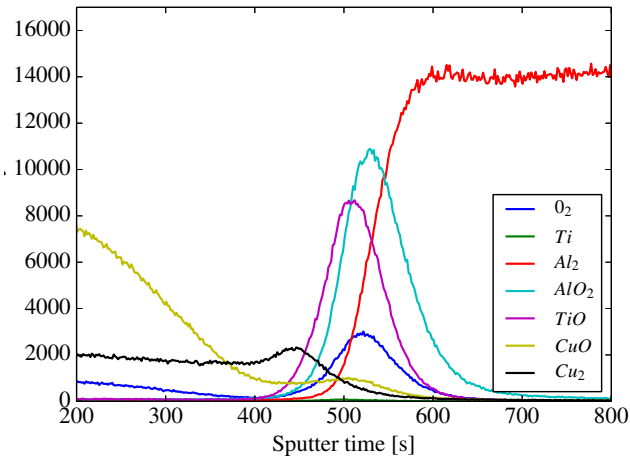


- Higher elec. resistance than expected
  - Due to seed layer/die topside interface
  - Would not happen with suitable dies
- **Simple and reproducible process**
  - Tens of samples assembled, with good yield



Conclusions on “Sandwich” ceramic structures

- Several sandwich configurations:
  - Solder [13, 14]
  - Silver sintering
  - Direct Cu/Cu bonding (Micro-posts)
- More suited to direct liquid cooling
  - Solid/liquid interface
  - Homogeneous compressing force
  - No issue with flatness
- Remaining issues:
  - Dies topside finish
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  - Intrinsic thermo-mechanical reliability

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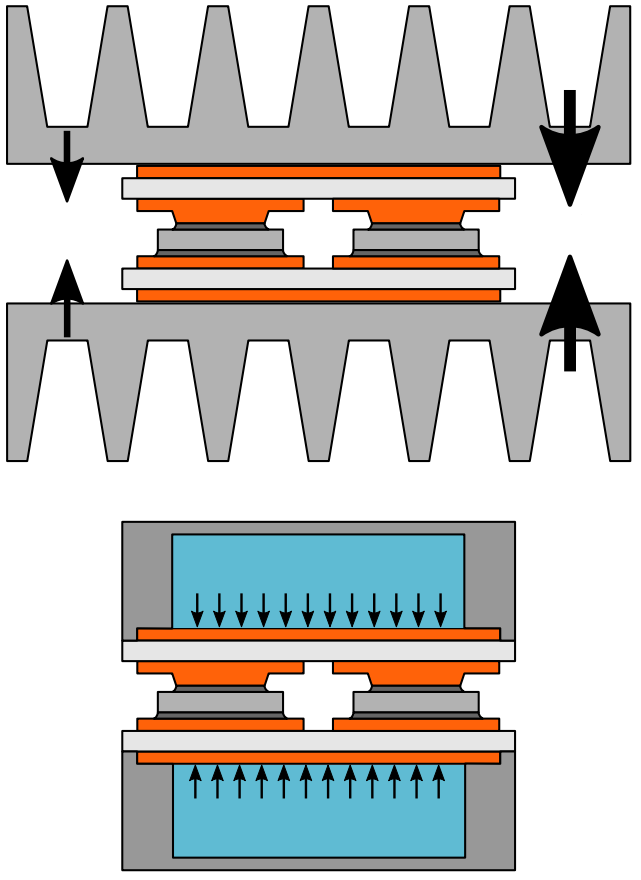

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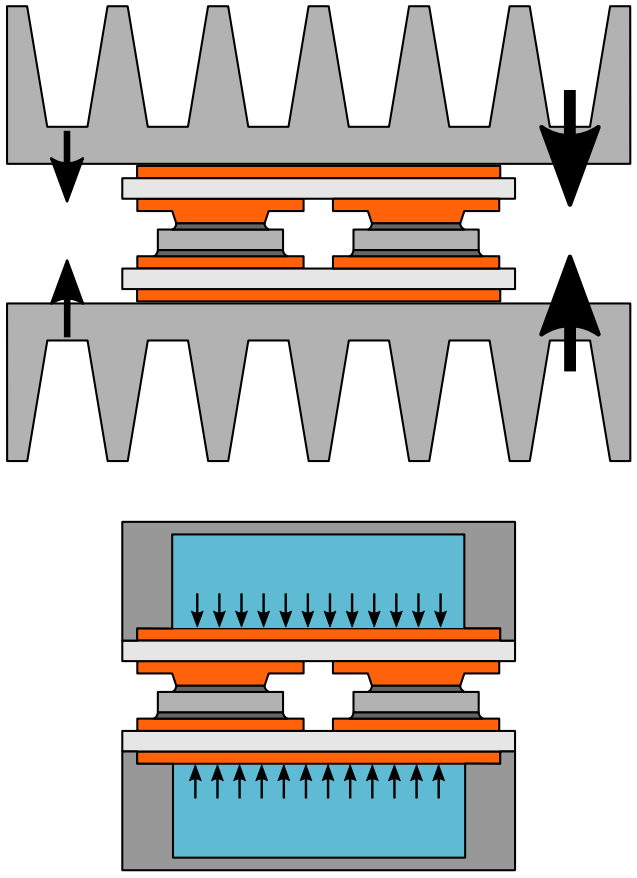
  - **Intrinsic thermo-mechanical reliability**
    - Need for further investigation



Outline

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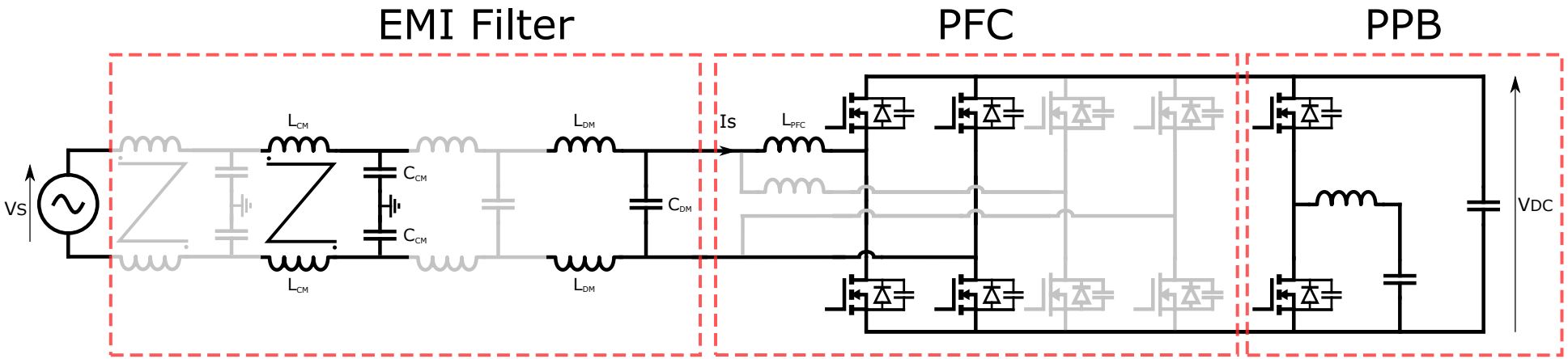
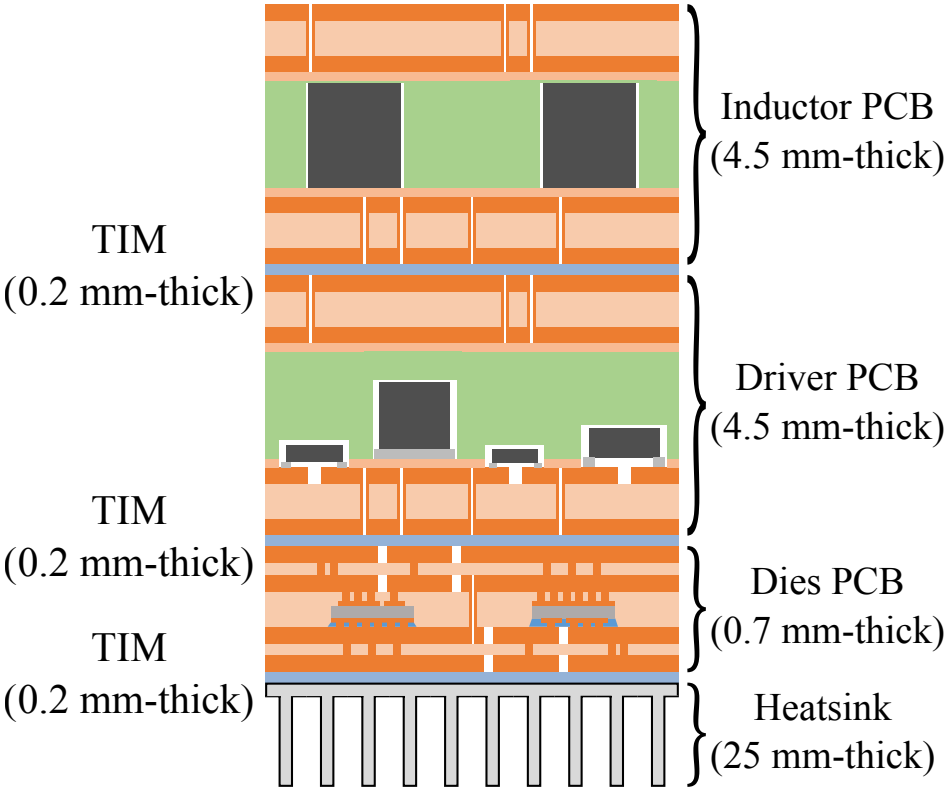
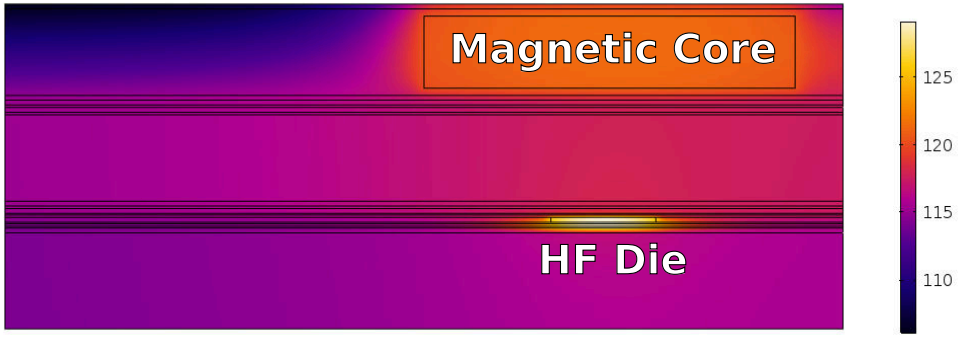


- Bidirectionnal, Power Factor Converter for 3.3 kW applications
- Designed through an optimization procedure [15, 16]
  - Based on SiC power devices
  - 180 kHz switching frequency
  - 4 interleaved cells
- Discussed here: PFC cell
- **Idea: embbed all devices** (not just semiconductor chips)

New Structures – PCB Embedding [17, 18]

Physical Structure





3-PCB structure

- Magnetic component on top
- Heatsink on bottom
  (natural convection)
- Power chips close to heatsink

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Two board structures are used:

Thin PBC (1 mm)
for bare dies

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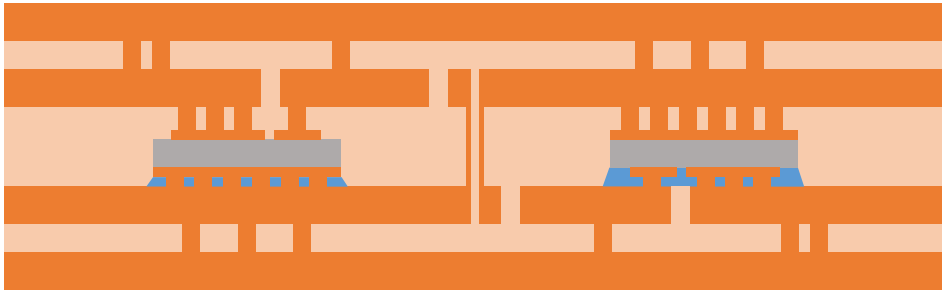

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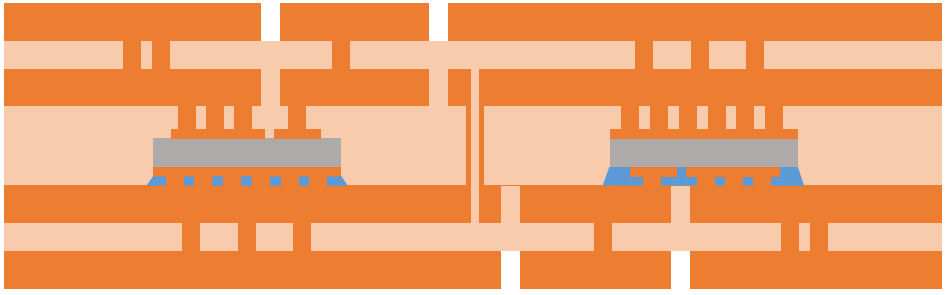

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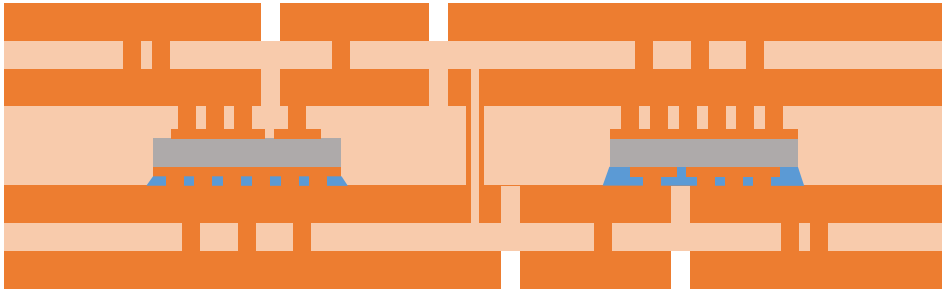

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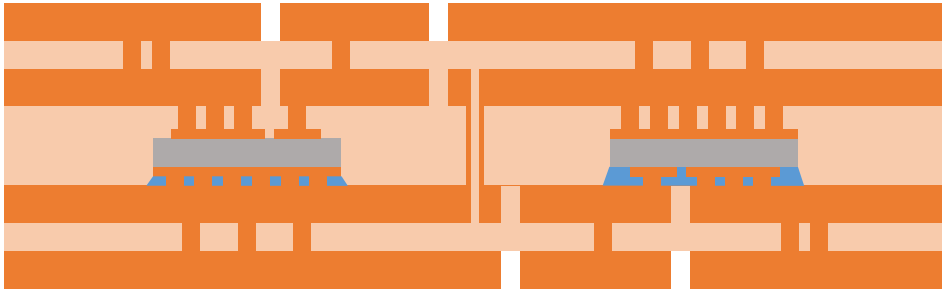

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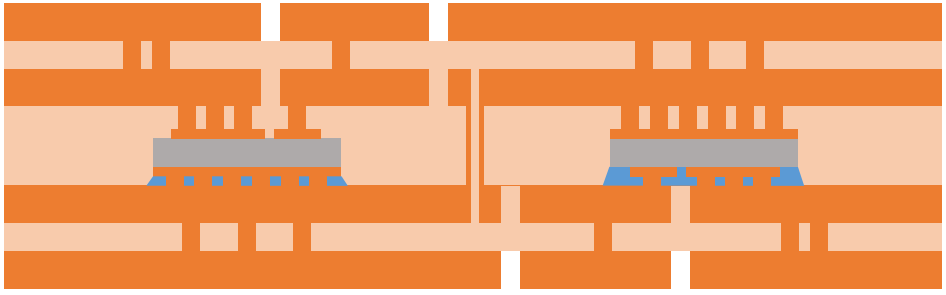

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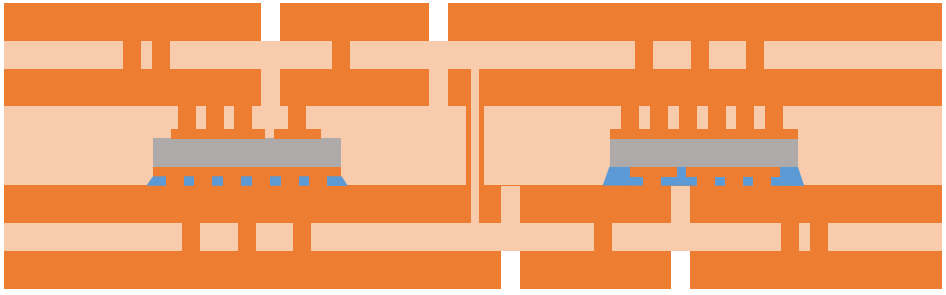

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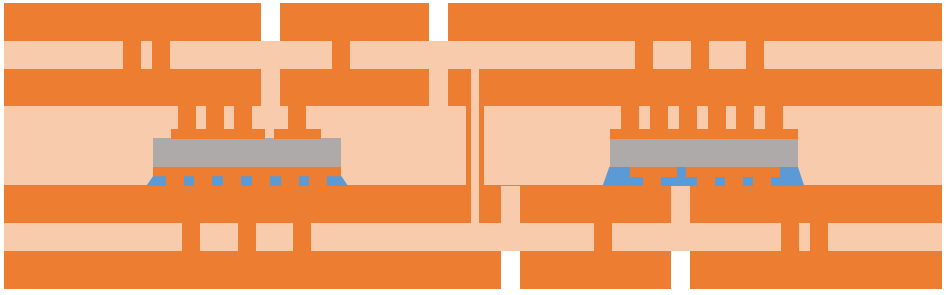

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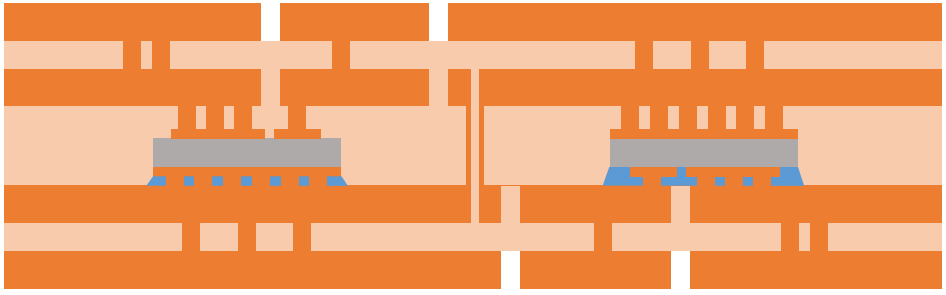

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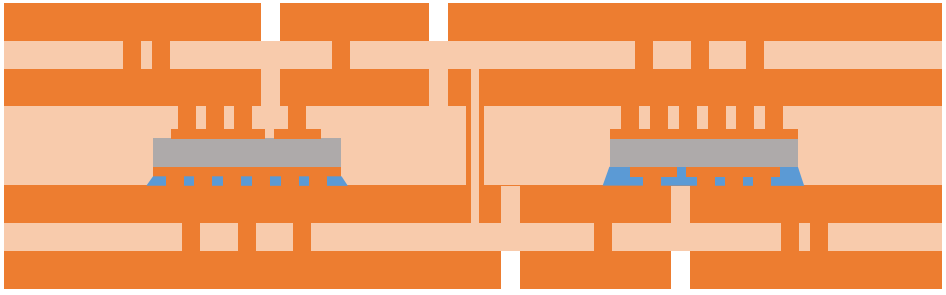

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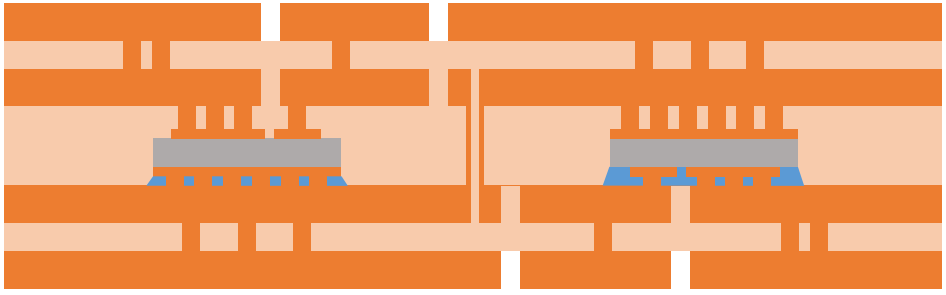

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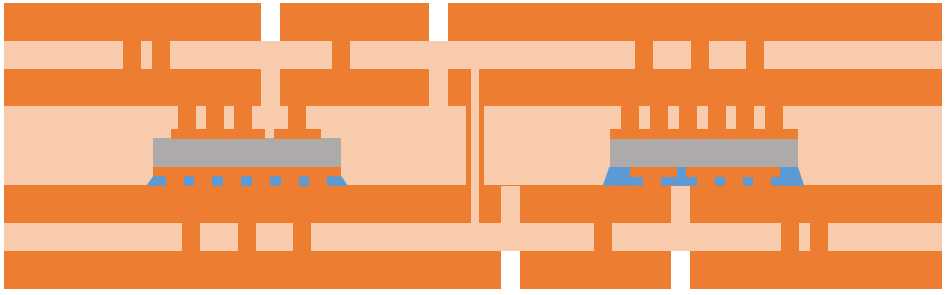

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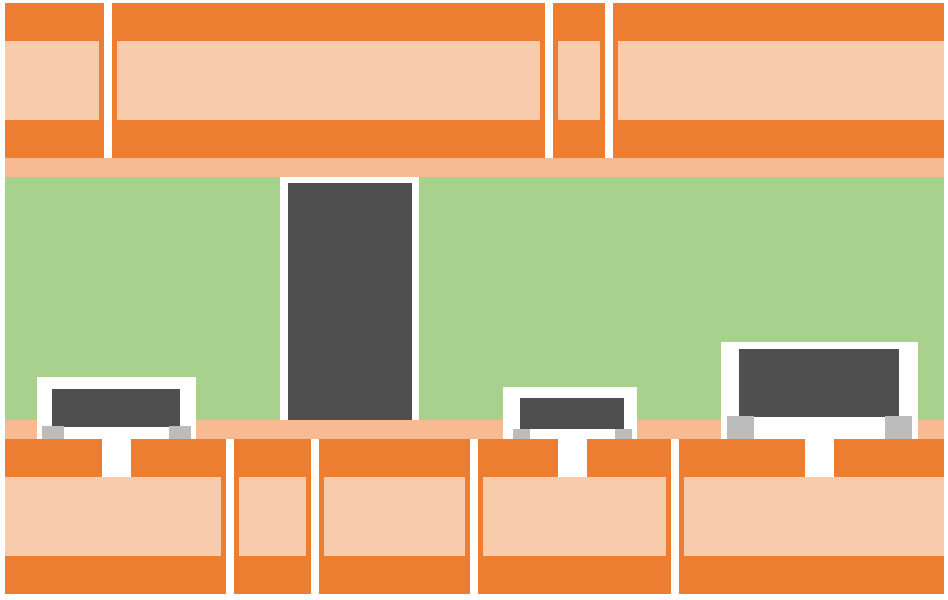

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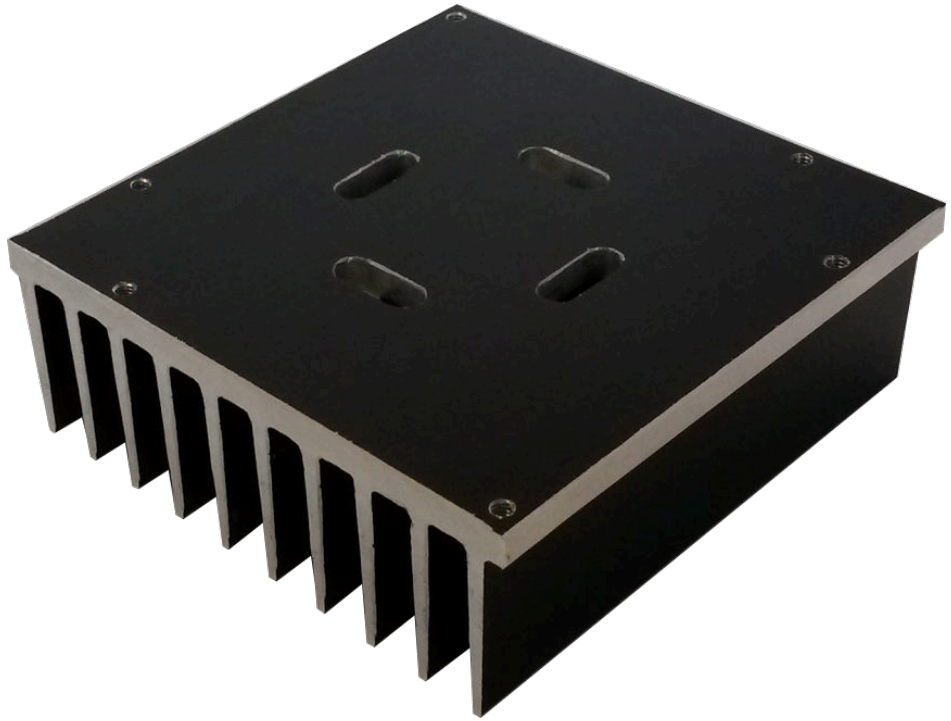
- Thermal Interface Material (TIM)
- Heatsink



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- Final cell dimensions: $7 \times 7 \times 3.5\,\mathrm{cm}^3$

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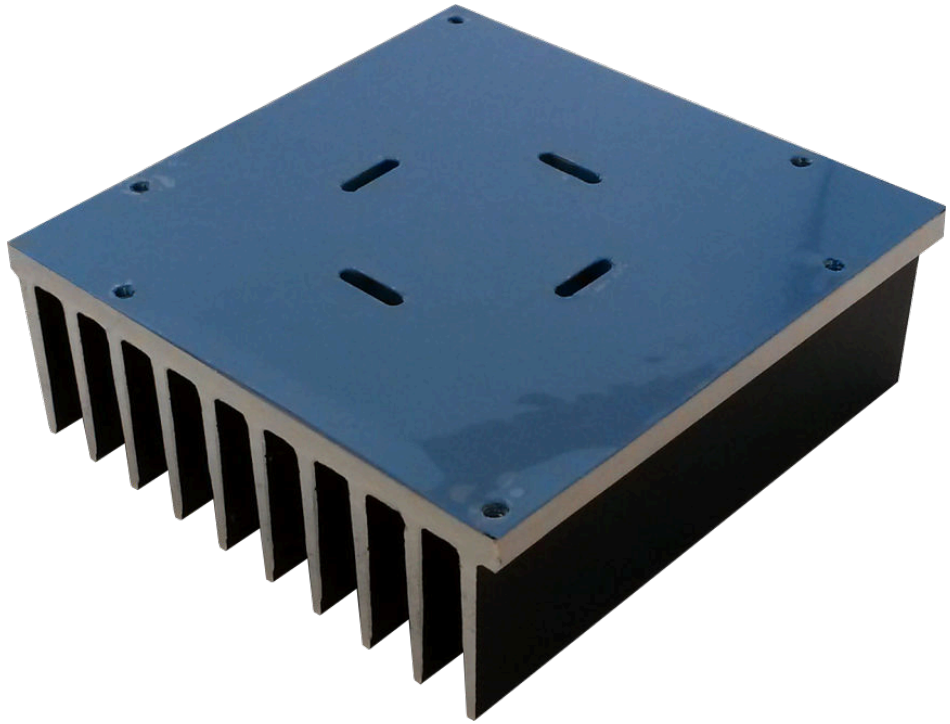

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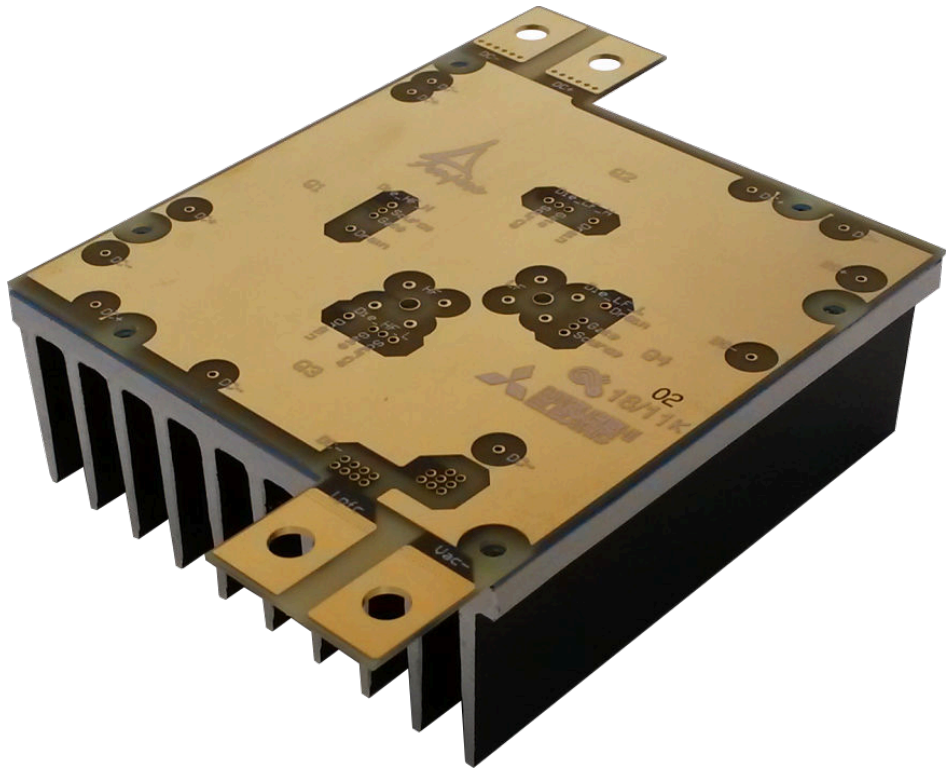

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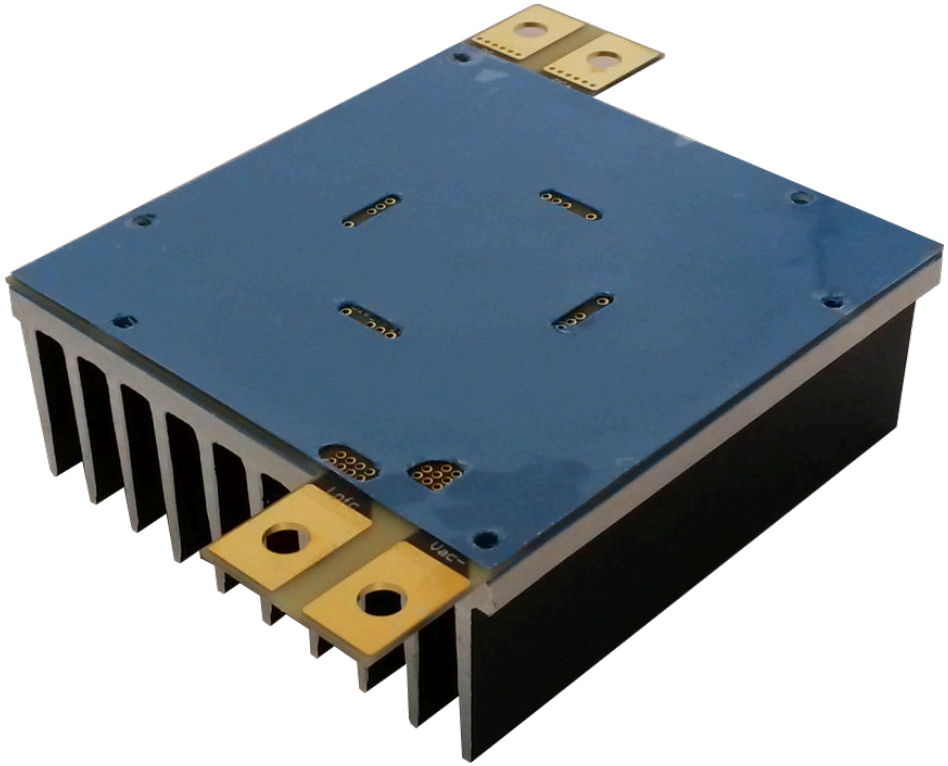

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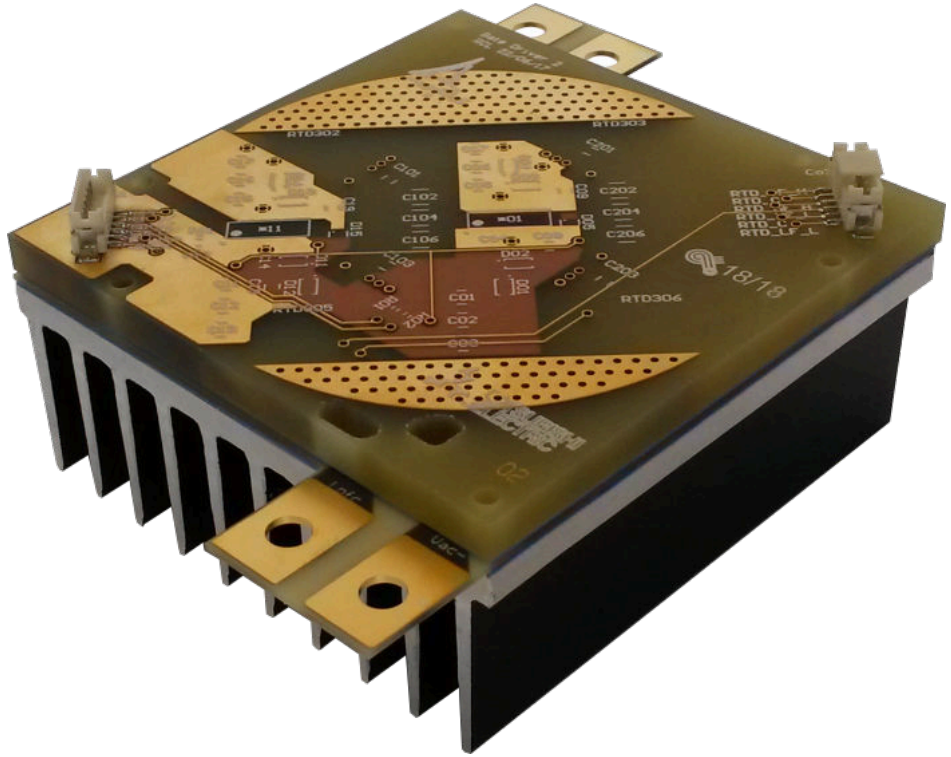

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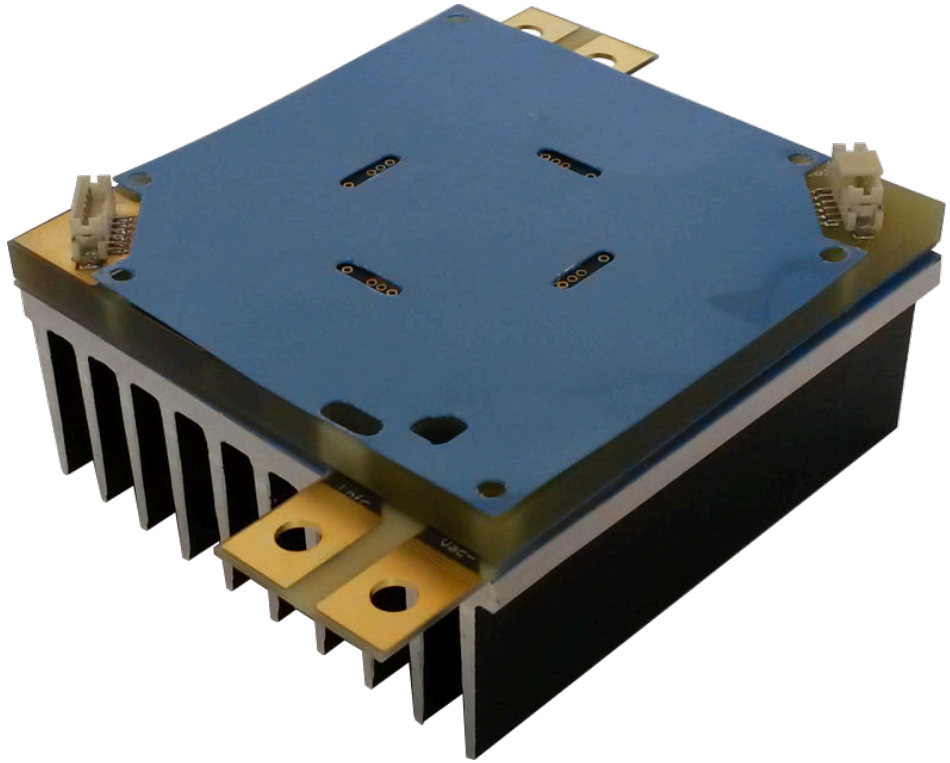

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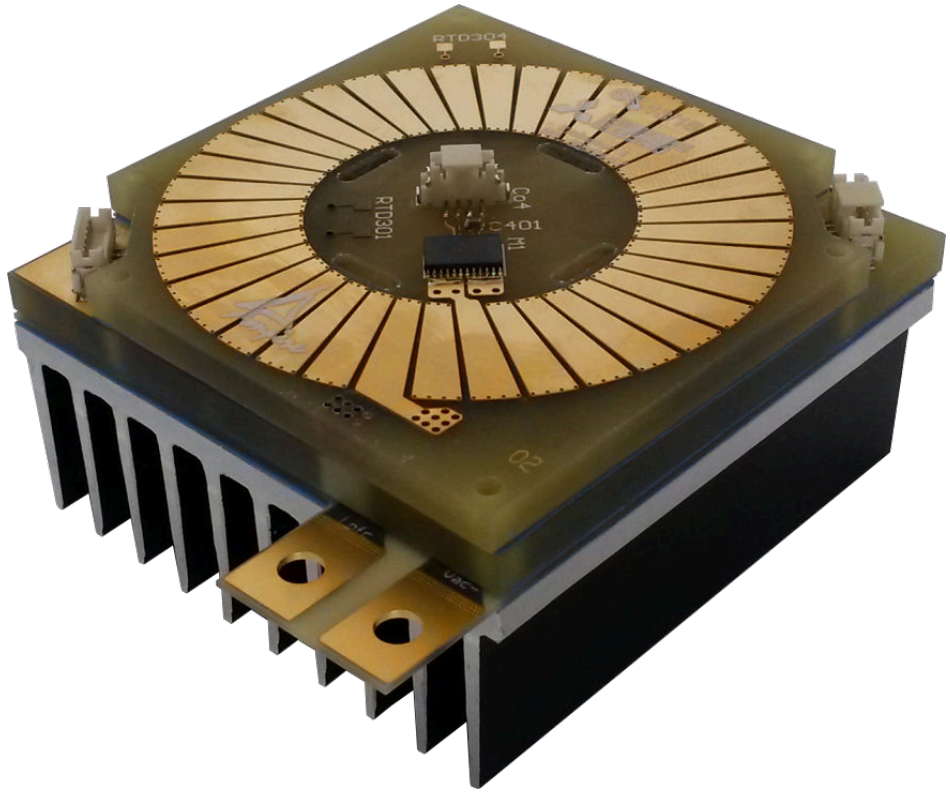

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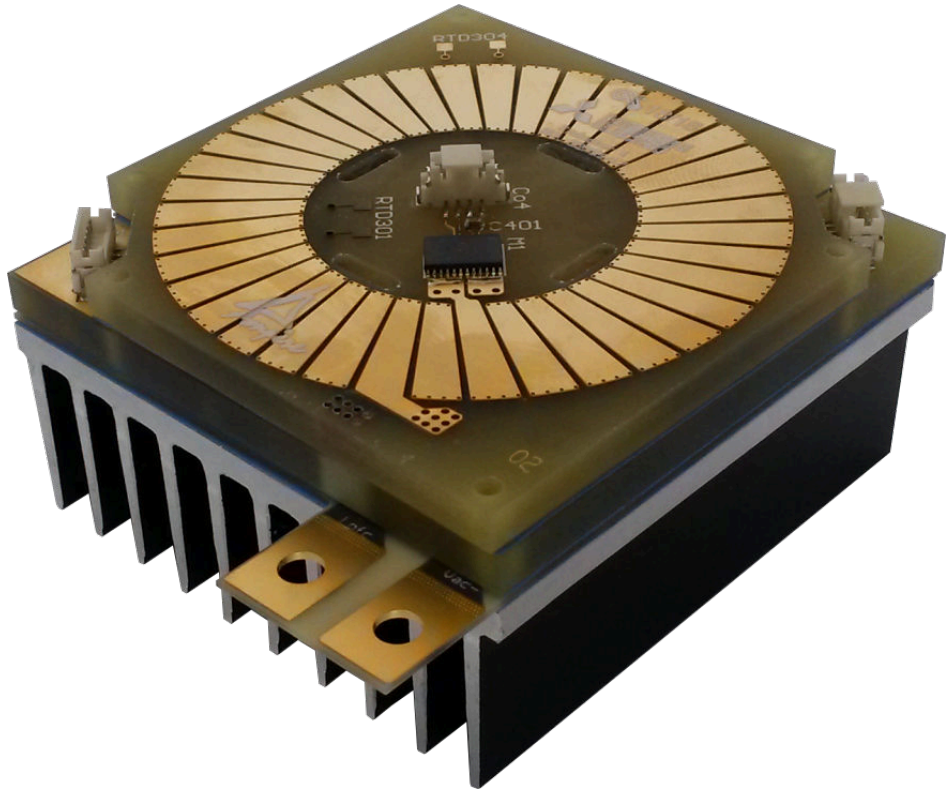


- Board-to-board interconnects using wires soldered in through-holes
- Final cell dimensions: $7 \times 7 \times 3.5\,\mathrm{cm}^3$

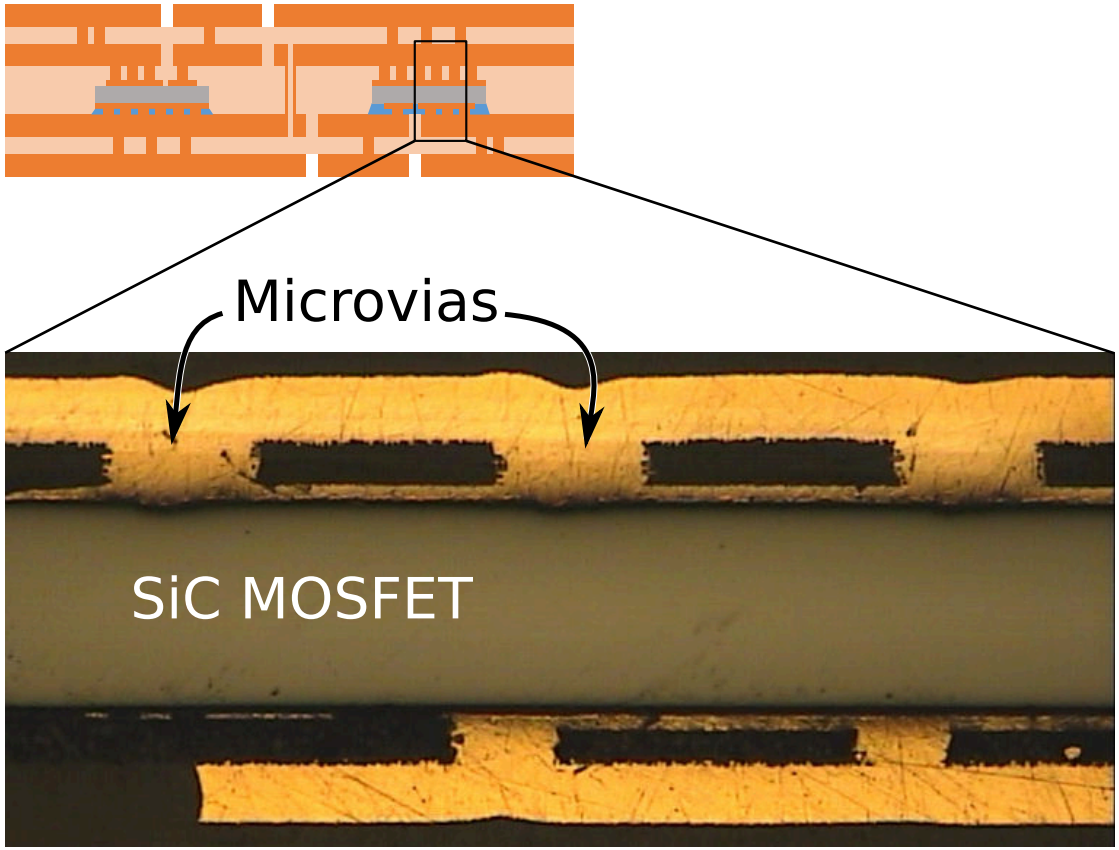
New Structures – PCB Embedding [17, 18]

- 4 PFC cells for a full converter
- DC capacitor bank for test only
- 4-stage EMC DM filter
- 28x7x5 cm^3

New Structures – PCB Embedding [17, 18]

For SiC dies

- good quality of microvias
  - No damage to dies
  - Uniform thickness
- Good alignment
  - Gate contact $500 \times 800\ \mu m^2$
- Good electrical perf.
  - Consistent $R_{DS_{on}}$ (80 mΩ)
  - No change in V_{th}
  - Low leakage current (max 1.6 nA @ 1200 V)
  - Very good yield (97% on 44 dies)



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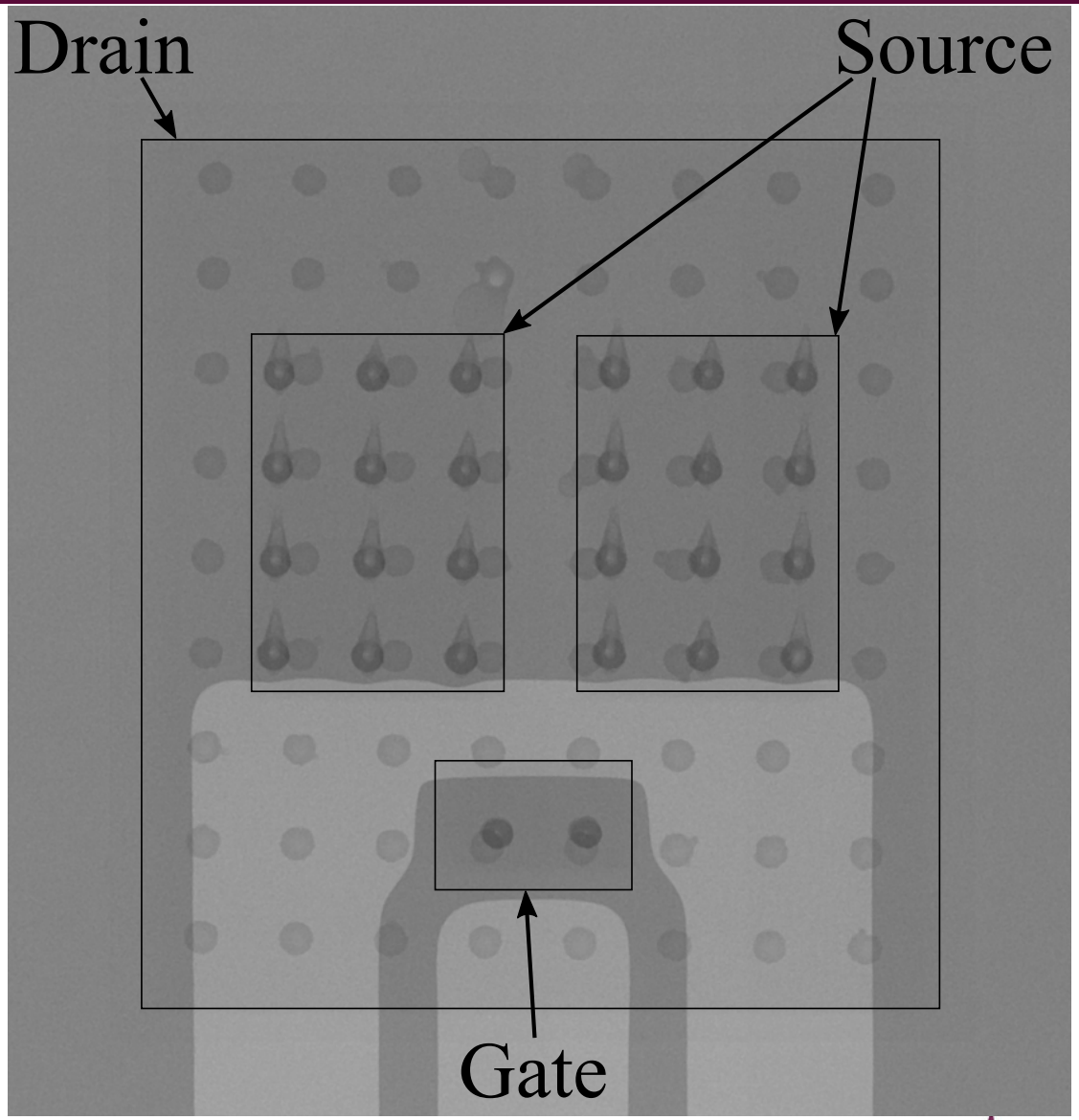

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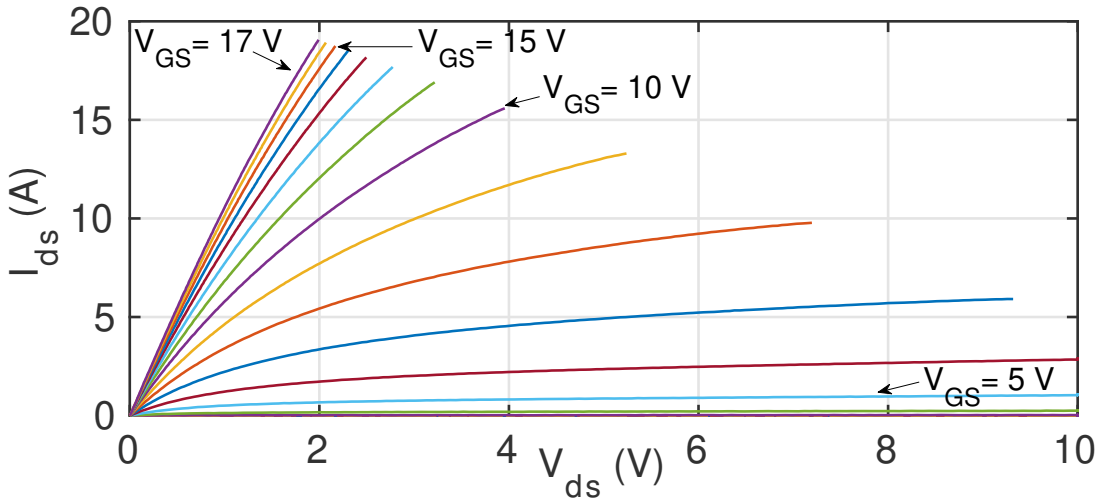

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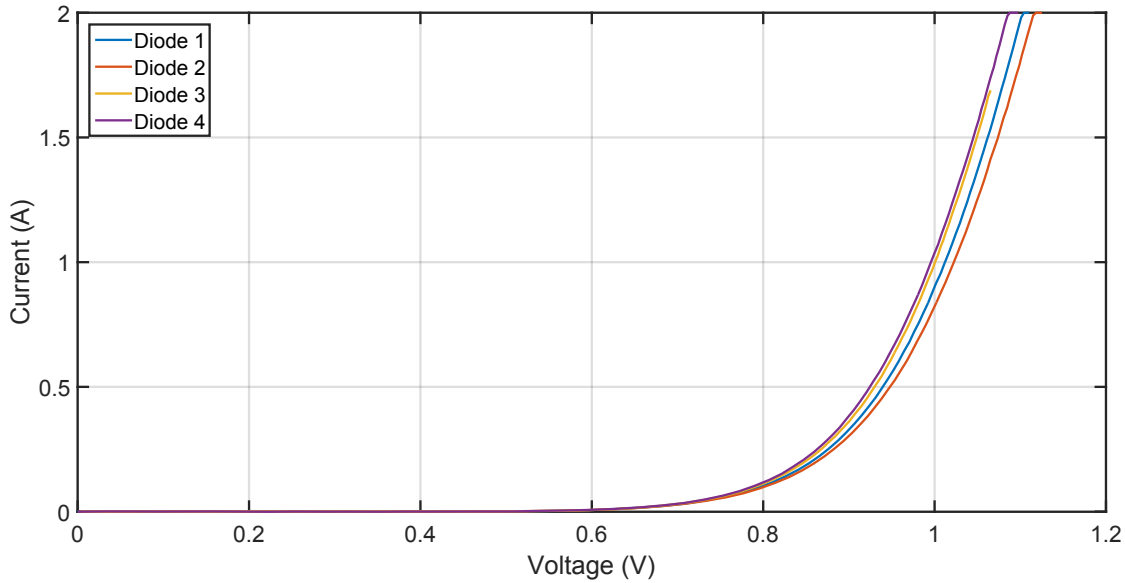
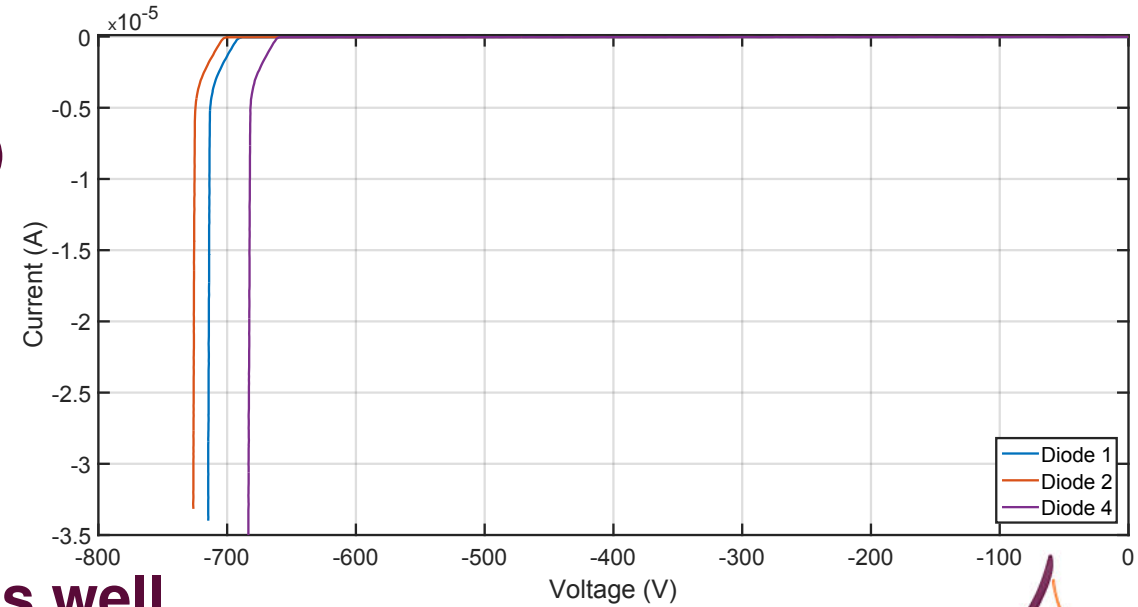
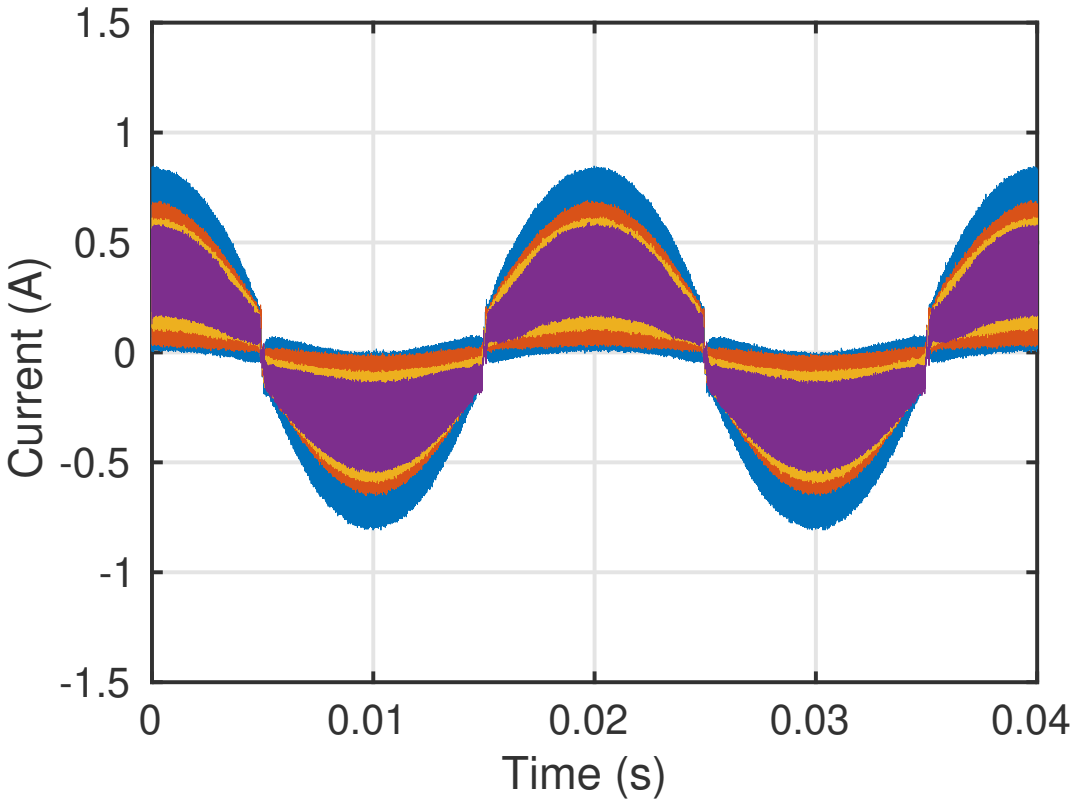




Other SMD components OK as well

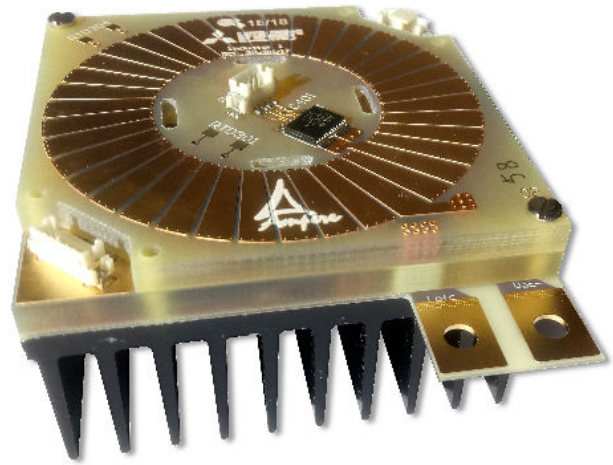
Operation of the PFC converter



- 4 interleaved PFC cells (target power $4 \times 825\,\mathrm{W} = 3.3\,\mathrm{kW}$)
- Operation at reduced power because of losses in inductors
  - Current unbalance because of differences in inductor values

Conclusions – Exploiting the PCB Embedding

- "All-embedded", interleaved PFC designed
  - includes dies, driver, inductors
  - Very good production yield
  - Only issue: embedded inductors
- Next step: better use of embedding
  - Keep some components on the surface
  - Improve design for manufacturing
  - Improve design tools



MITSUBISHI ELECTRIC
Changes for the Better

Ampère

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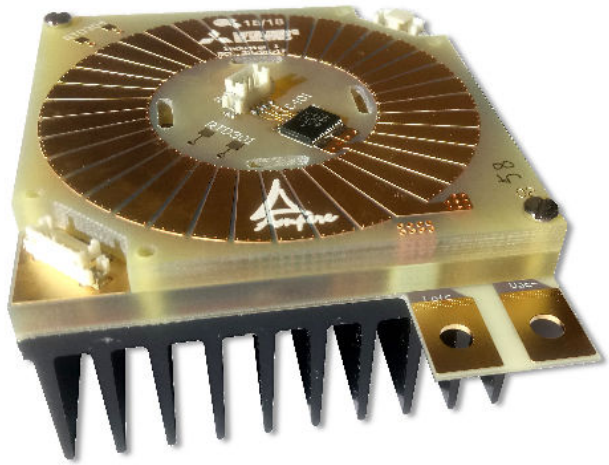
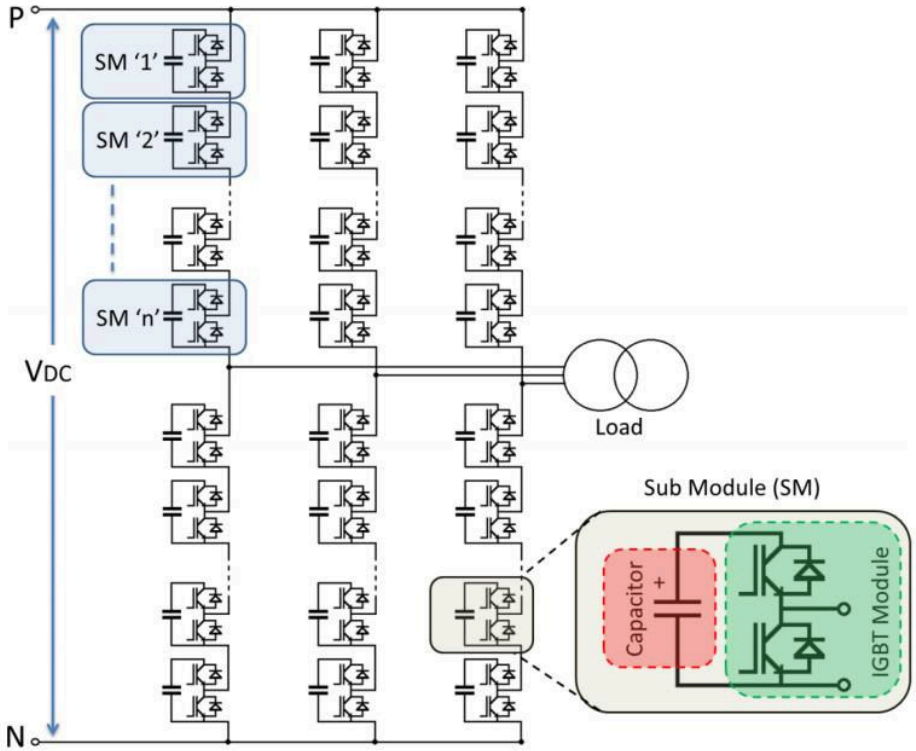


MITSUBISHI ELECTRIC
Changes for the Better

Outline

Outline

Fail-to-Short Packaging for HVDC Applications



Source: I. Yaqcub PhD thesis, 2015 [19]

HVDC Converters

- Rated at 100s kV
  (ex 320 kV for France-Spain link)
- Series of 100s of transistors
  (800 for same converter)
- Transistors fail randomly
  - Should not stop converter
  - Failed device turned to short circuit

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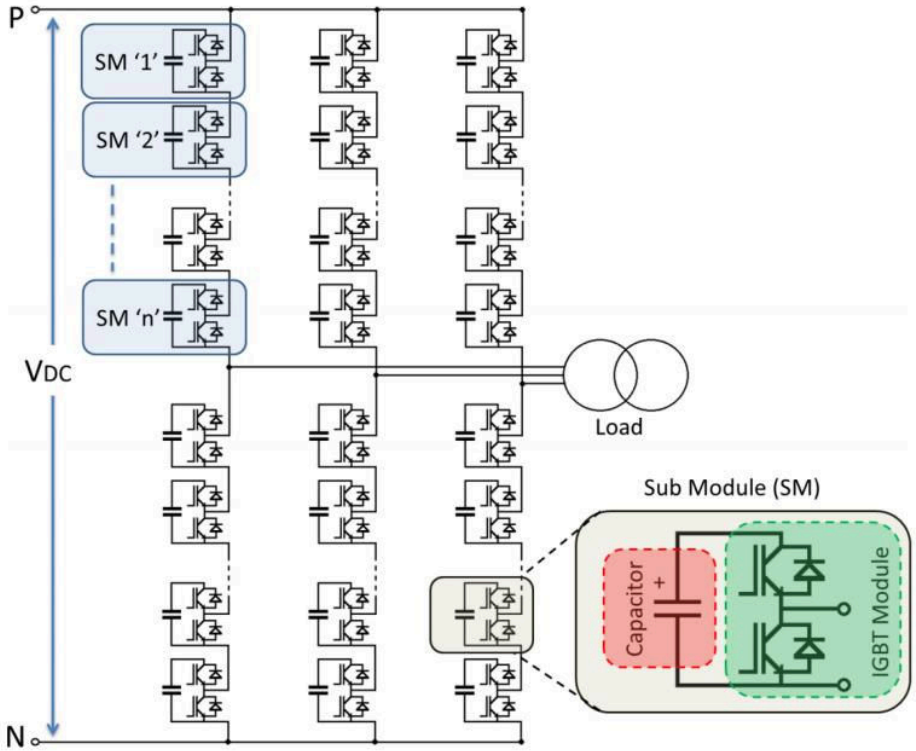

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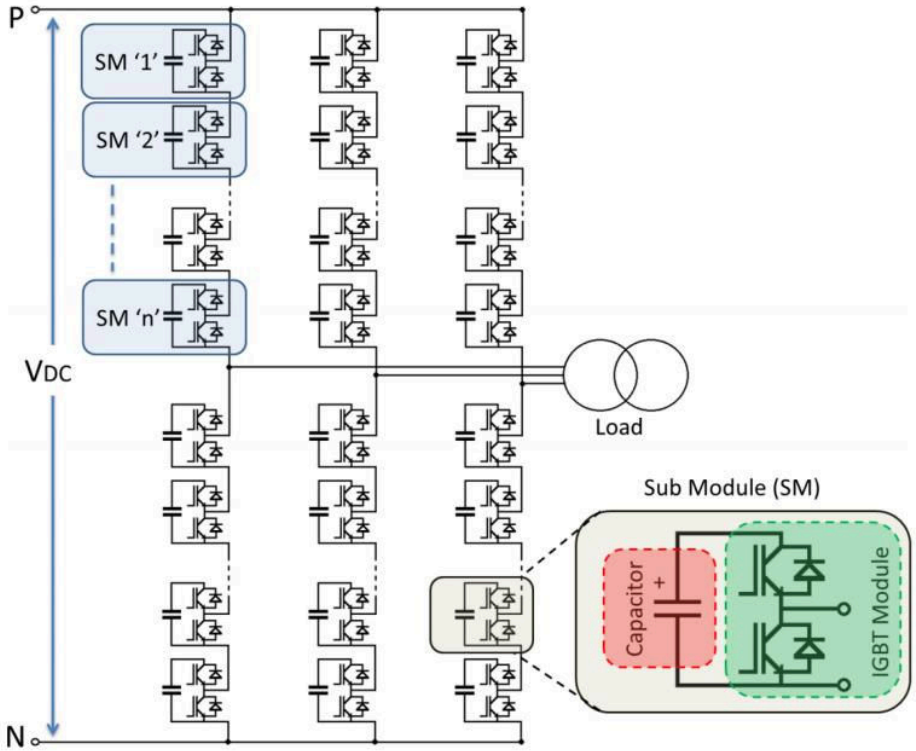

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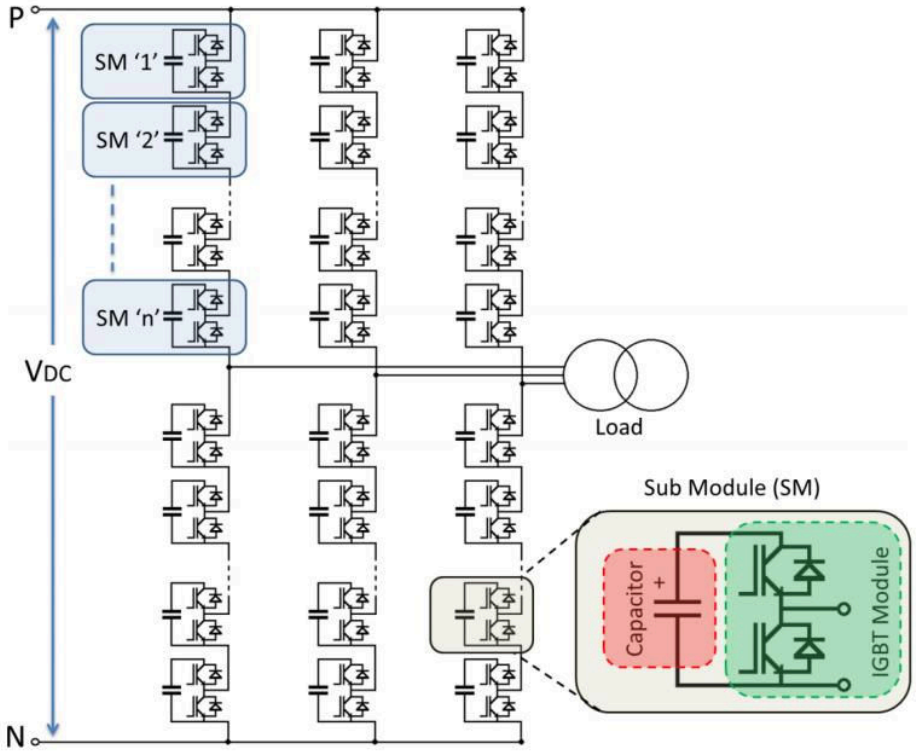

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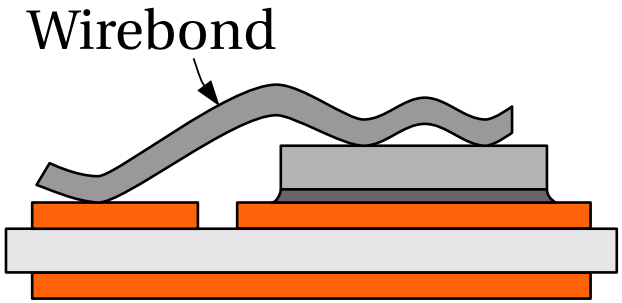
➜ Need for Fail-To-Short Packaging

Fail-to-Short Packaging



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- Wirebonds act as fuses or blown away

➜ Need for massive contacts

- "Press pack"-type packages introduced
- Initially for single die, now for multichip
- When failure occurs:
  - Temperature rises
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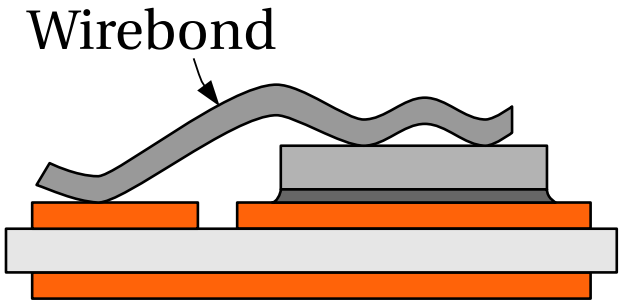
  - Strong package contains explosion

Fail-to-Short Packaging



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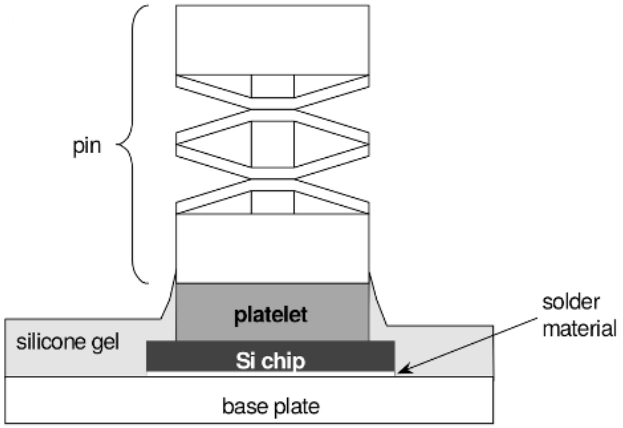

source: Gunturi, S. *et al.* Innovative Metal System for IGBT Press Pack Modules (ISPSD 2003) [20]

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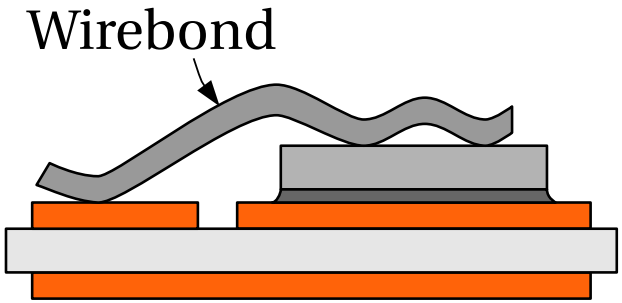

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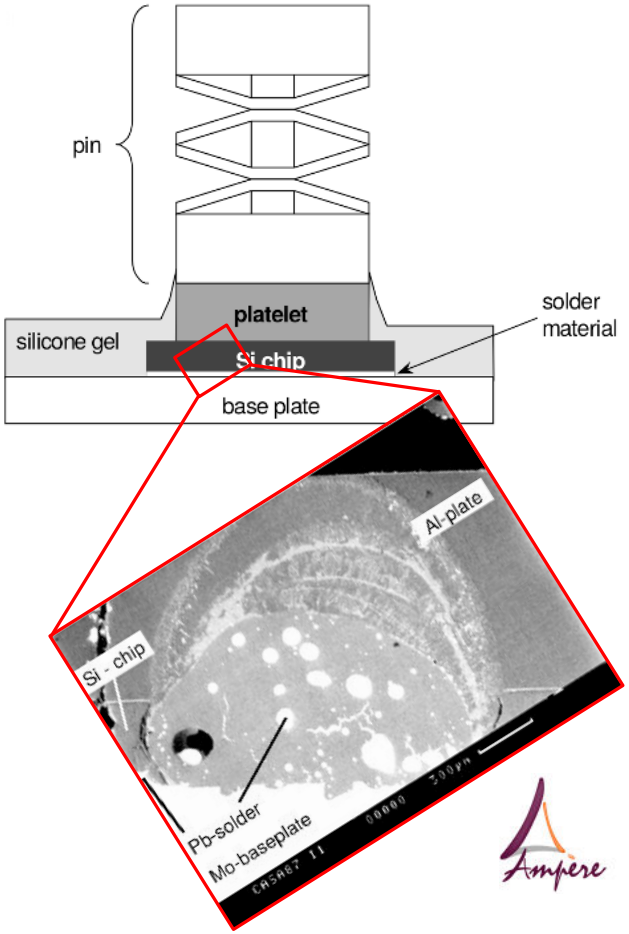

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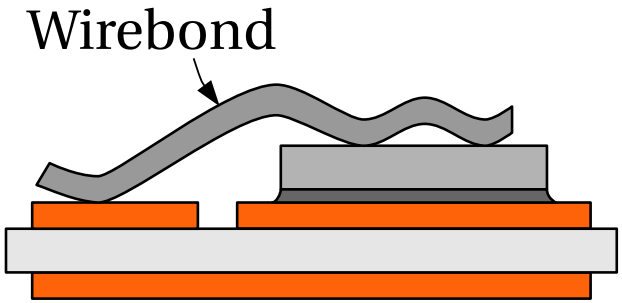

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Is a FTS package Possible for SiC?

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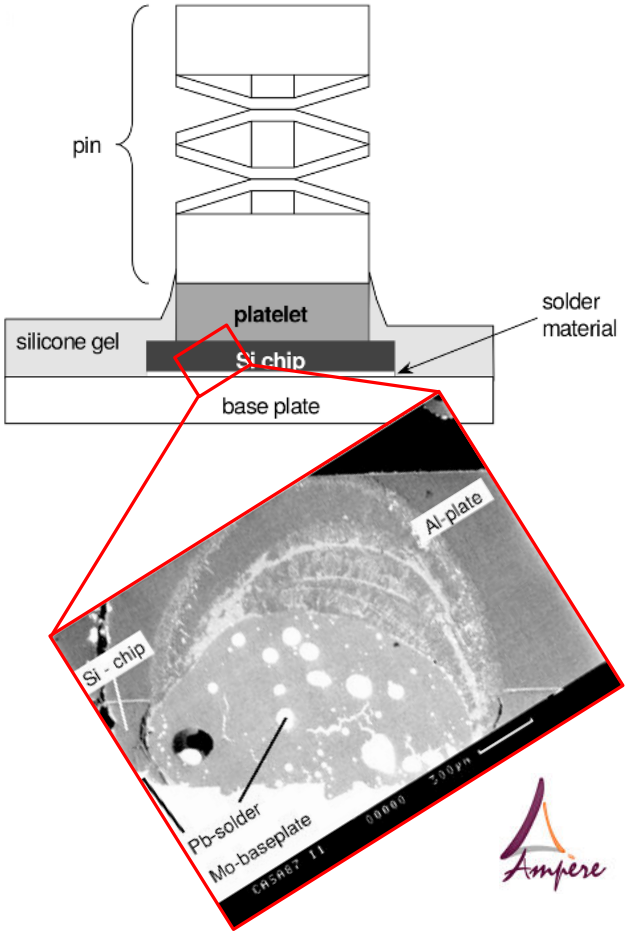
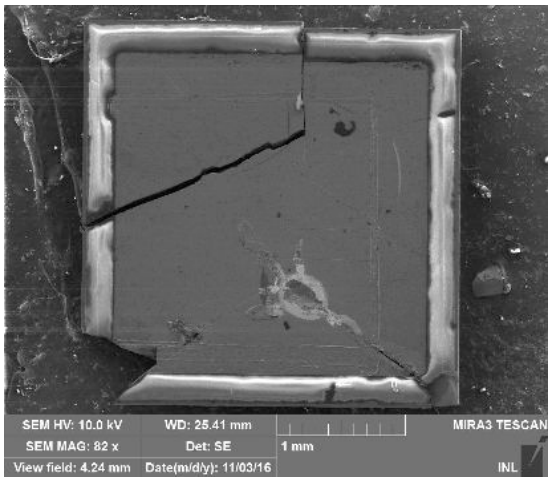


Fail-to-Short Packaging – test on SiC dies [21]



- Dies fracture because of failure
- SiC and metal remain separate
- Tiny metal filaments form

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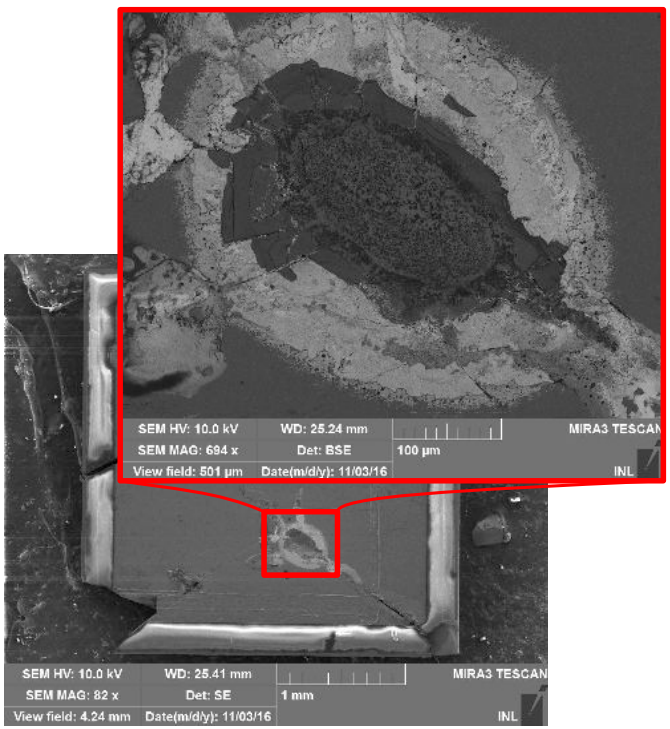

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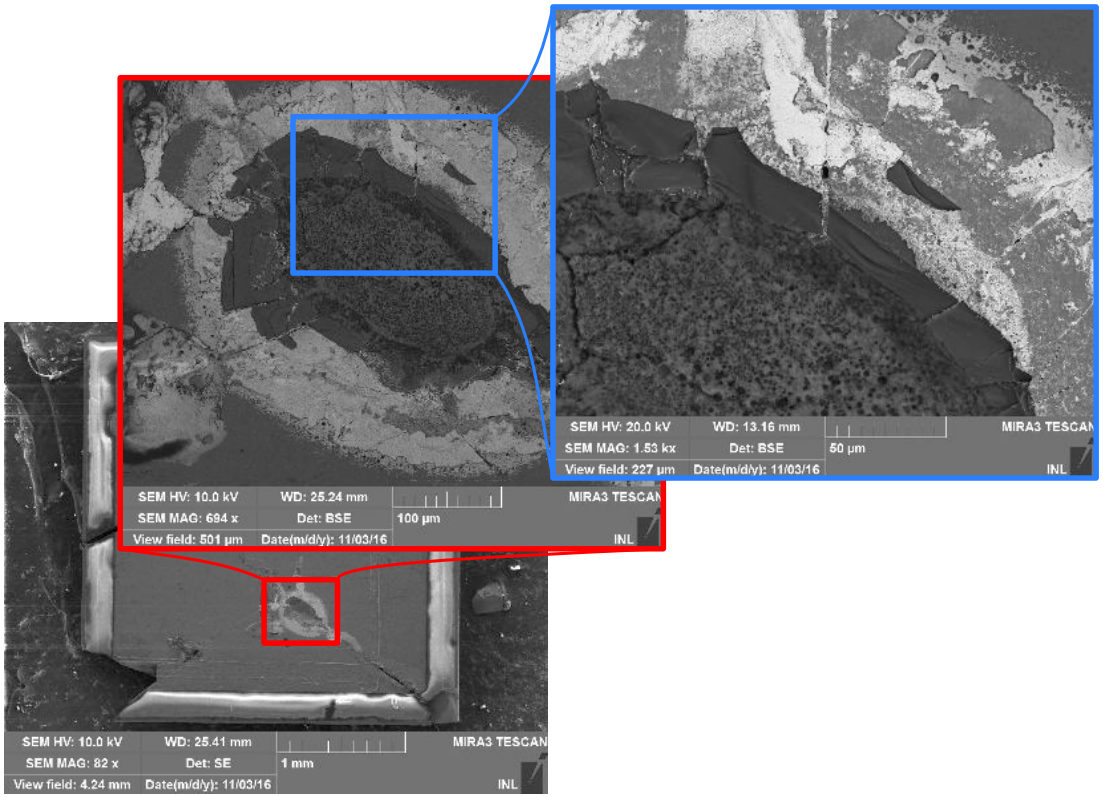

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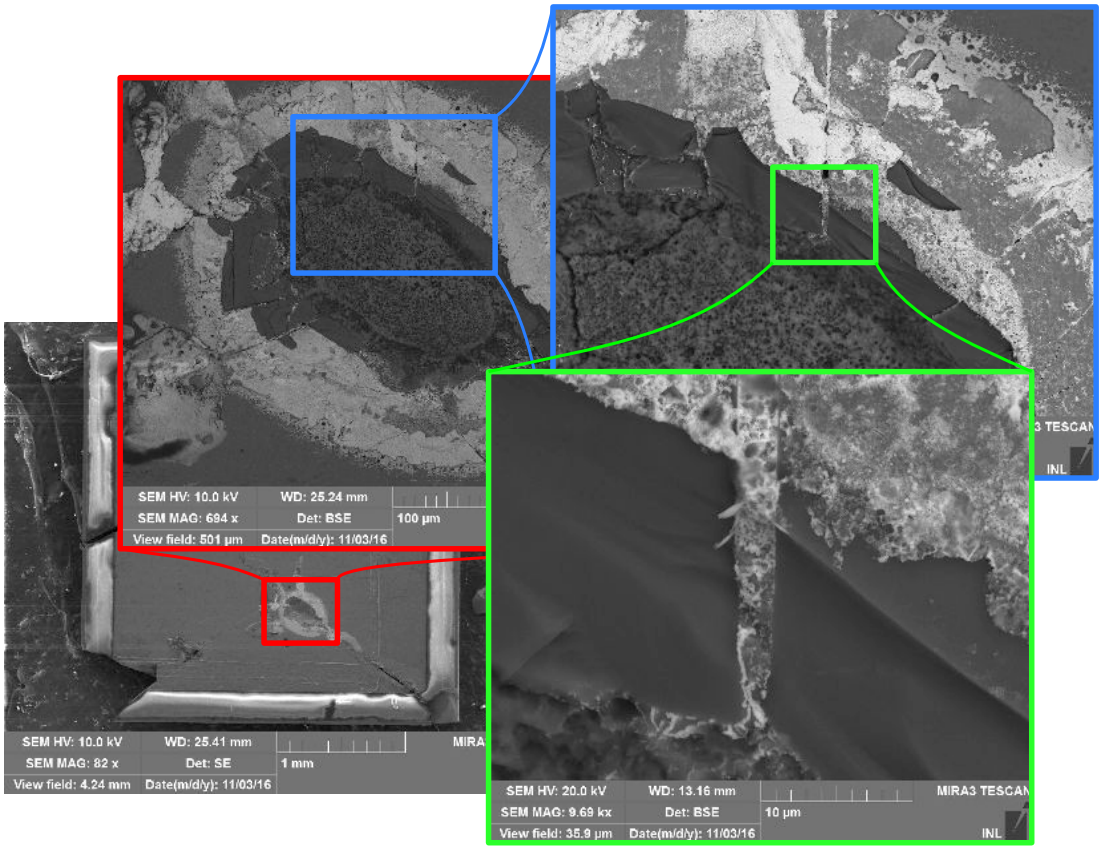

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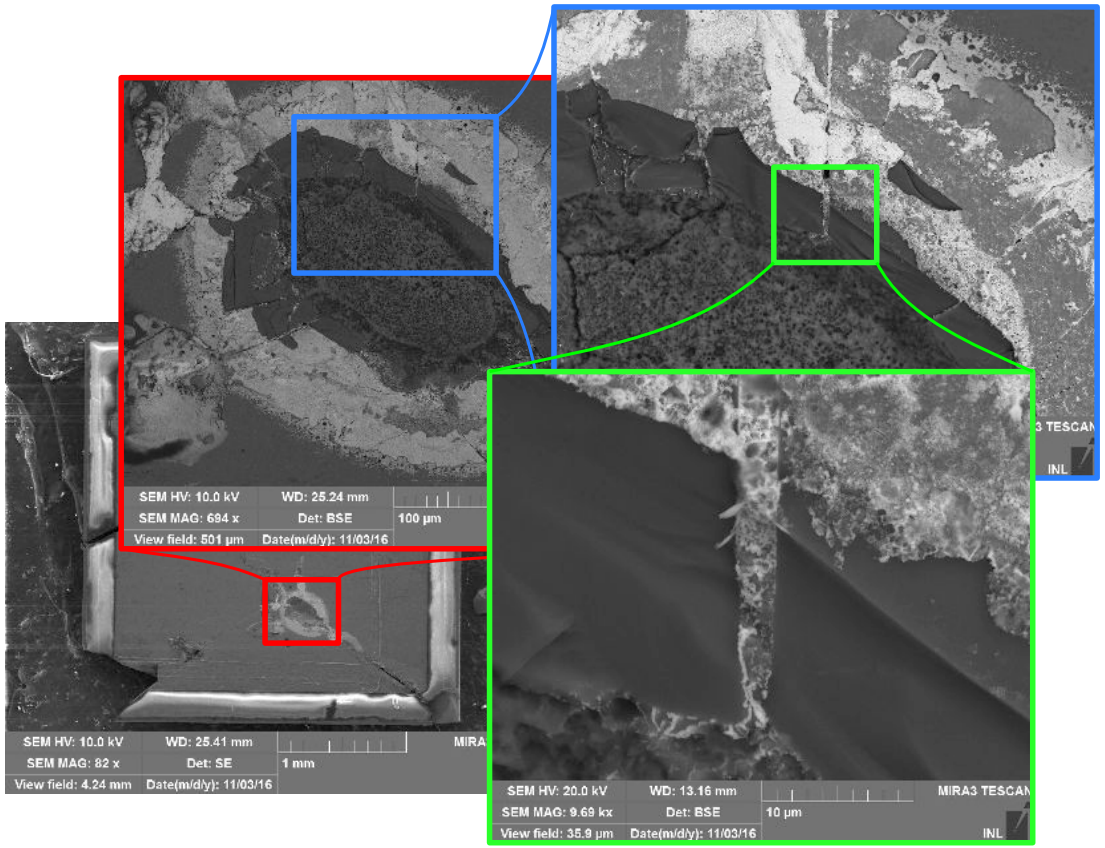

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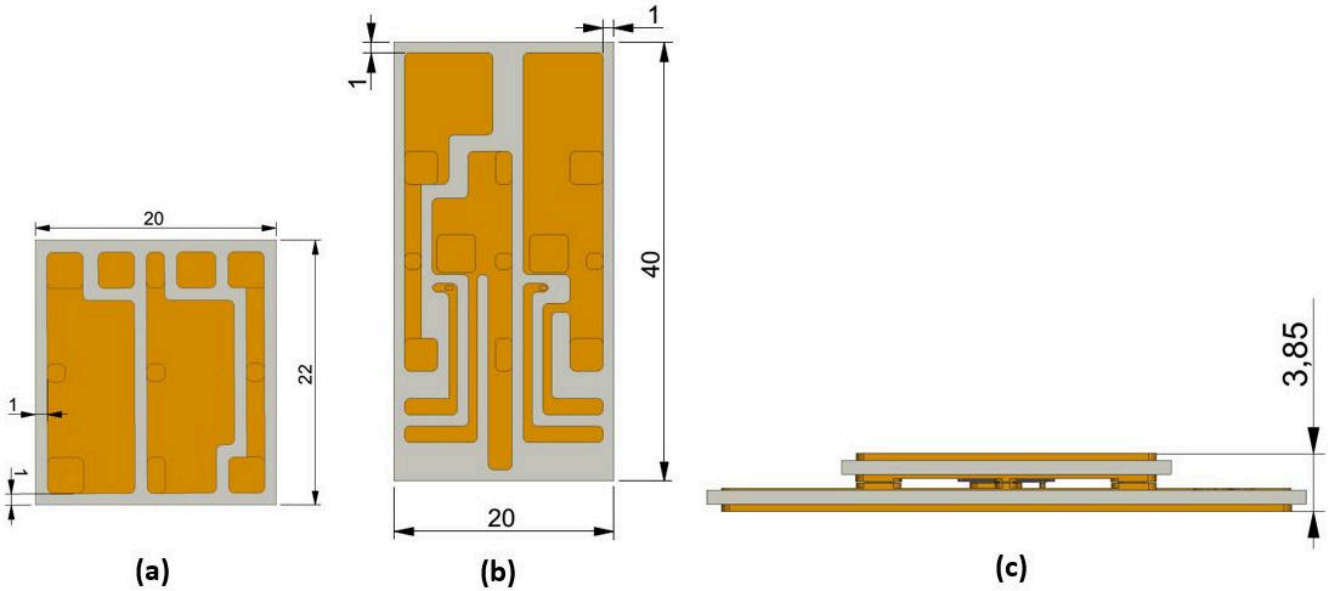
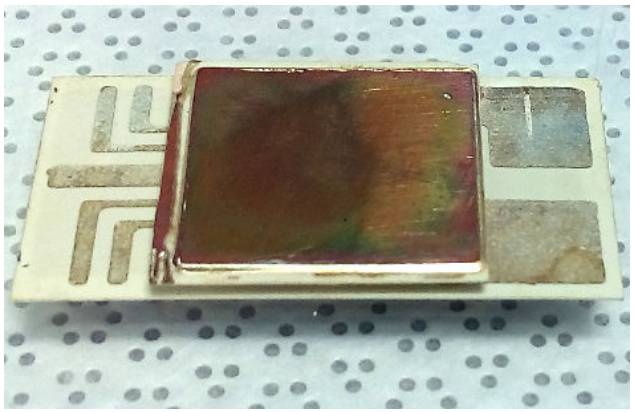
➜ **Fail-to-short behaviour possible with SiC**

Fail-to-Short Packaging – Design of a module [22]

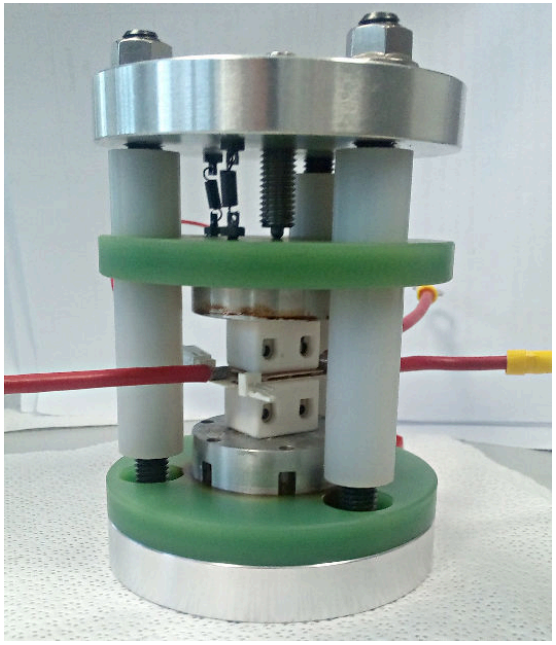


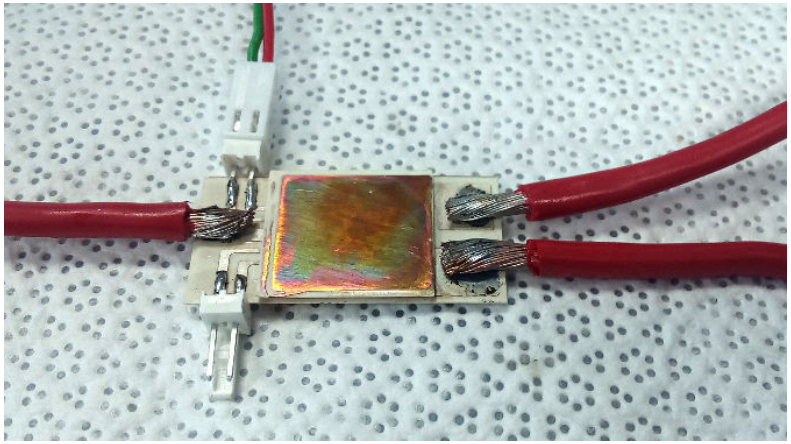
- **“Micro-Posts”**: massive interconnects
- **Silver sintering**: high temperature bonding
- **Salient features**: for topside contact



Fail-to-Short Packaging – Test samples [22]

Sample	Encapsulant	Clamp	Switch
Module A	None	Yes	MOS 1
			MOS 2
Module B	Silicone	Yes	MOS 1
			MOS 2
Module C	Epoxy	No	MOS 1
			MOS 2
Module D	Silicone	Yes	MOS 1
			–





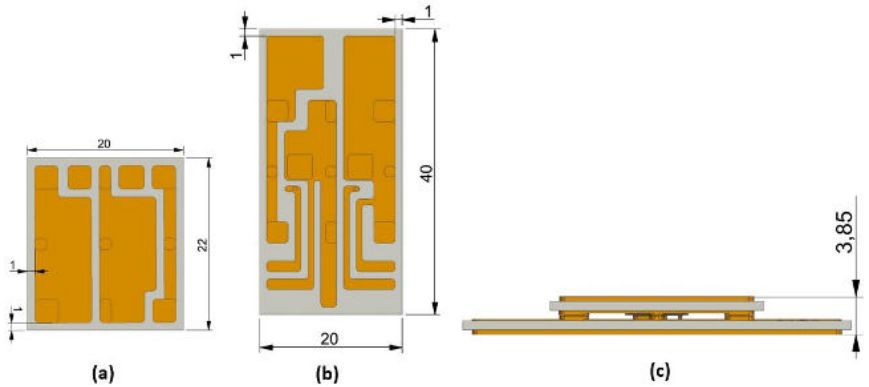
- Dies tested individually
- “Clamp” used for modules A, B and D
- MOS 2 of module D not connected

Fail-to-Short Packaging – Results [22]

	Encapsulant	Clamp	Switch	E [J]	R_{init} [mΩ]	R_{final} [mΩ]	Failure mode
A	None	Yes	MOS 1	–	186	77	SC
			MOS 2	8.8	201	128	SC
B	Silicone	Yes	MOS 1	20	165	120	SC
			MOS 2	1	188	167	SC
C	Epoxy	No	MOS 1	9.7	–	–	OC
			MOS 2	–	–	–	–
D	Silicone	Yes	MOS 1	2.24	180	158	SC
			–	–	–	–	–

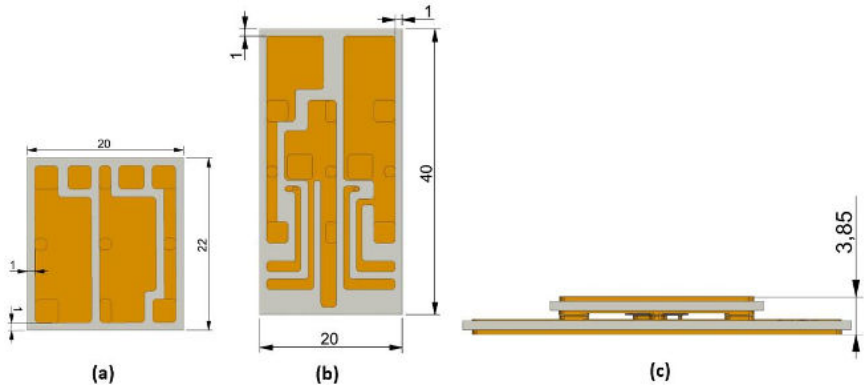
- Module C separated during first test, causing open circuit
- All other modules exhibited stable short circuit

Fail-To-Short Packaging – Conclusions



- Fail-to-Short behaviour with SiC dies requires:
  - to prevent the Ceramic tiles from separating
  - ➜ a strong mechanical clamp/frame
  - ➜ soft encapsulant probably better for gases to escape
- To provide massive interconnects:
  - wirebonds would act as fuses
  - to supply metal to fill the cracks in the dies
  - heat dissipation at failure points helps reducing the resistance

Fail-To-Short Packaging – Conclusions



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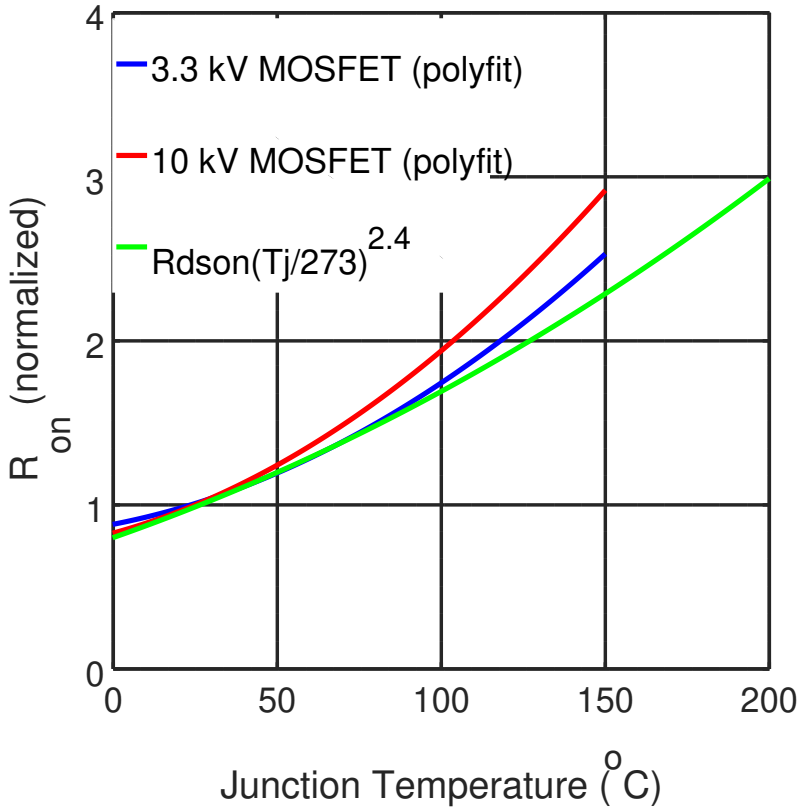
Outline

HV Substrates – Thermal stability of SiC MOSFETs

- Considering only conduction losses
  - $P = R_{DS_{on}} I_D^2$
- Considering only mobility reduction
  - $R_{DS_{on}}(T_J) = R_{DS_{on},273} \times \left(\frac{T_J}{273}\right)^{2.4}$ [23]

➜ Strong increase of losses with T_J



➜ Need for Low R_{Th}/High voltage substrate

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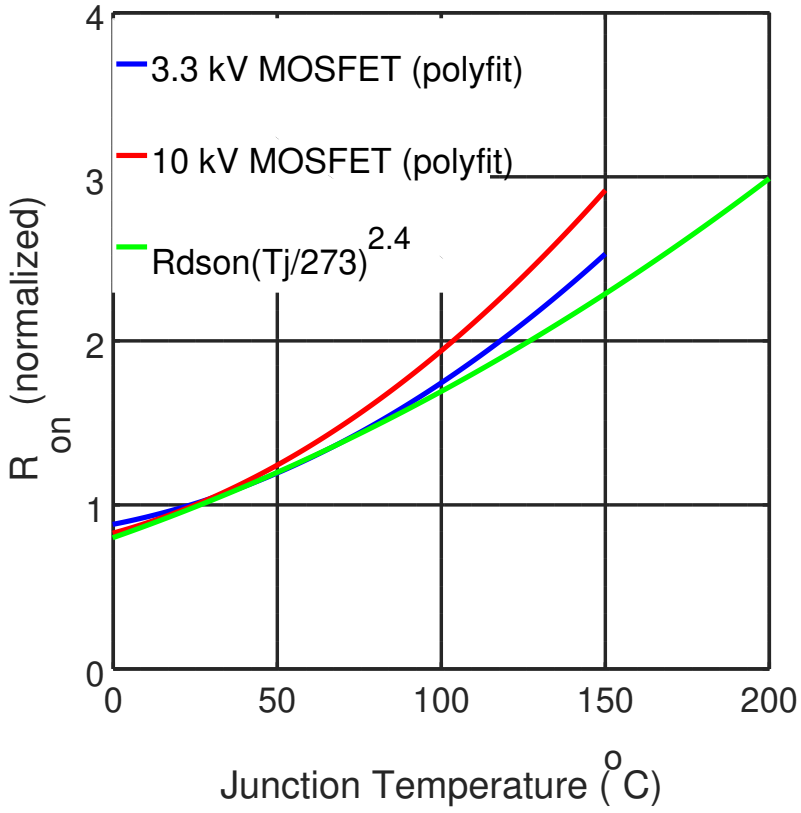
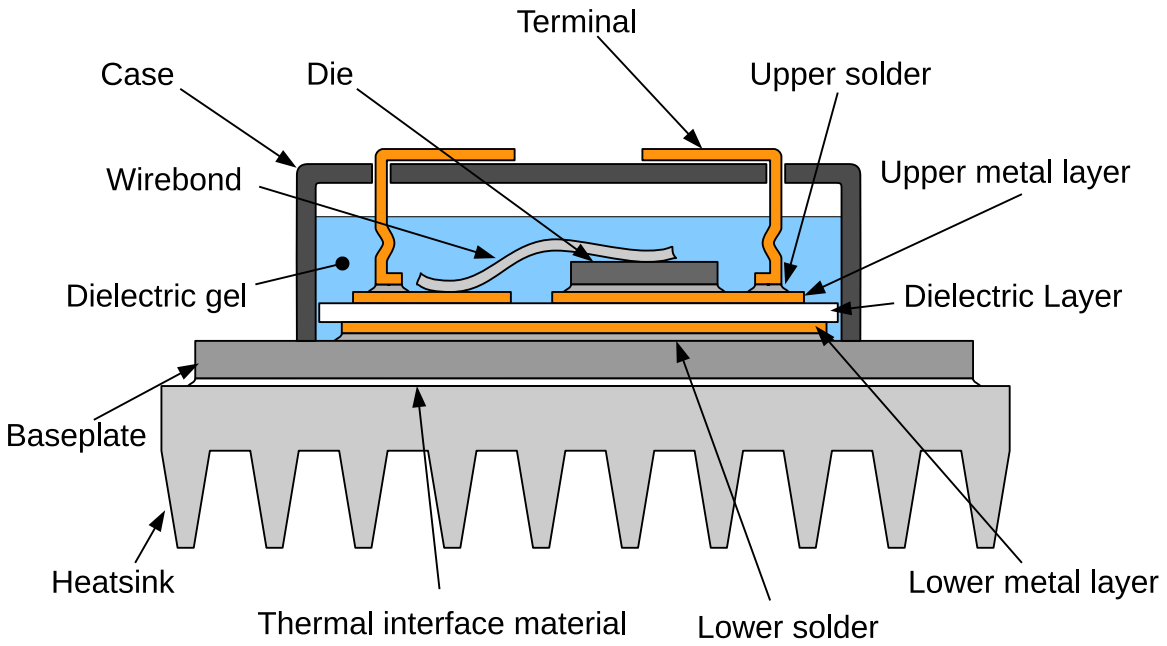


➜ Need for Low R_{Th}/High voltage substrate

HV Substrates – Thermal/Electrical trade-off

Packaging of SiC dies

- Backside cooling
- Electrical insulation of baseplate



HV Substrates – Thermal/Electrical trade-off

Packaging of SiC dies

- Backside cooling
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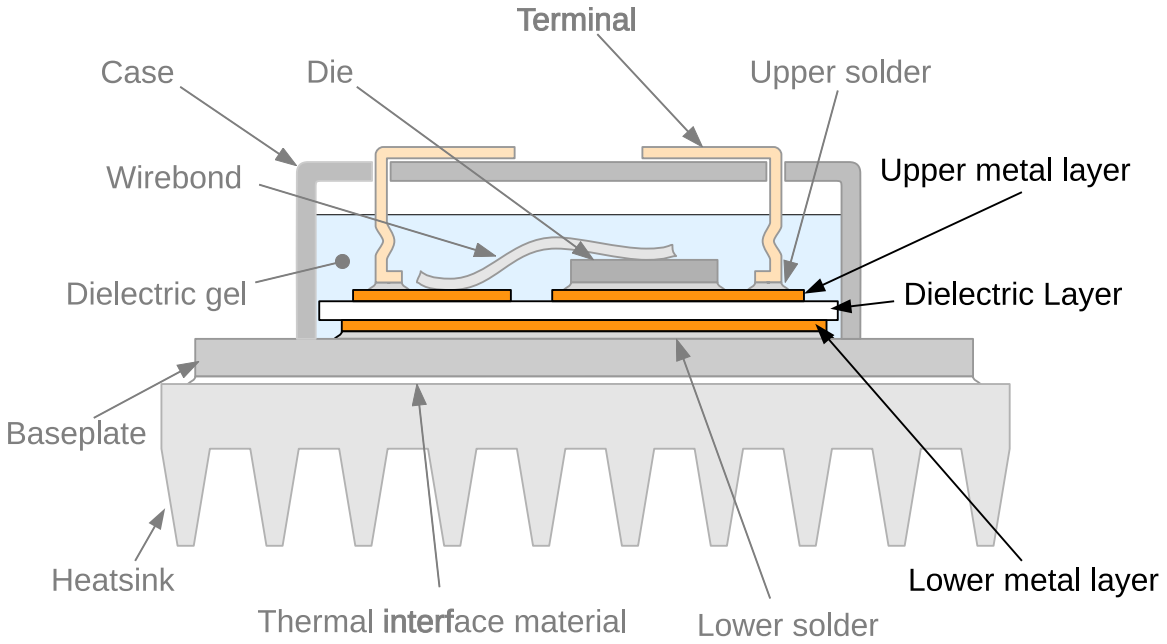
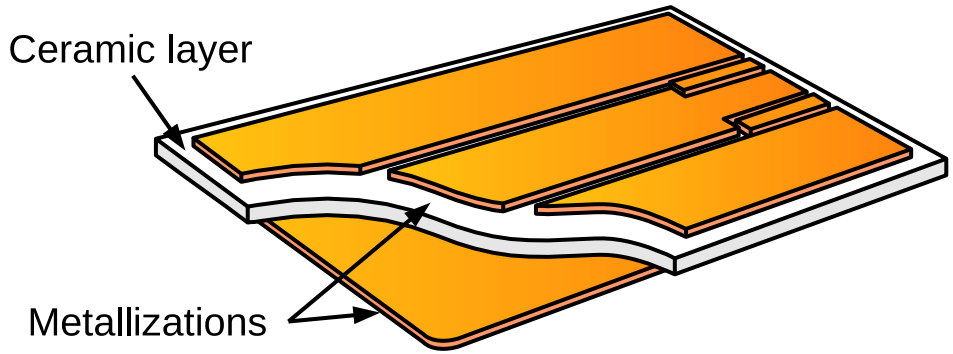
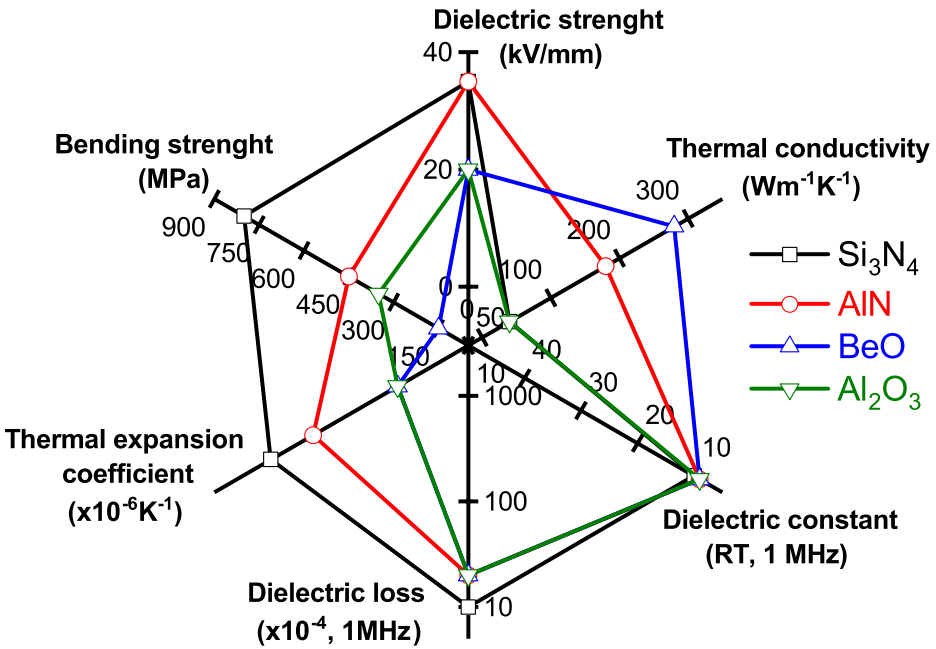
Ceramic substrate Ensures

- Electrical insulation
- Heat conduction





HV Substrates – Materials and Geometric Issues [24]

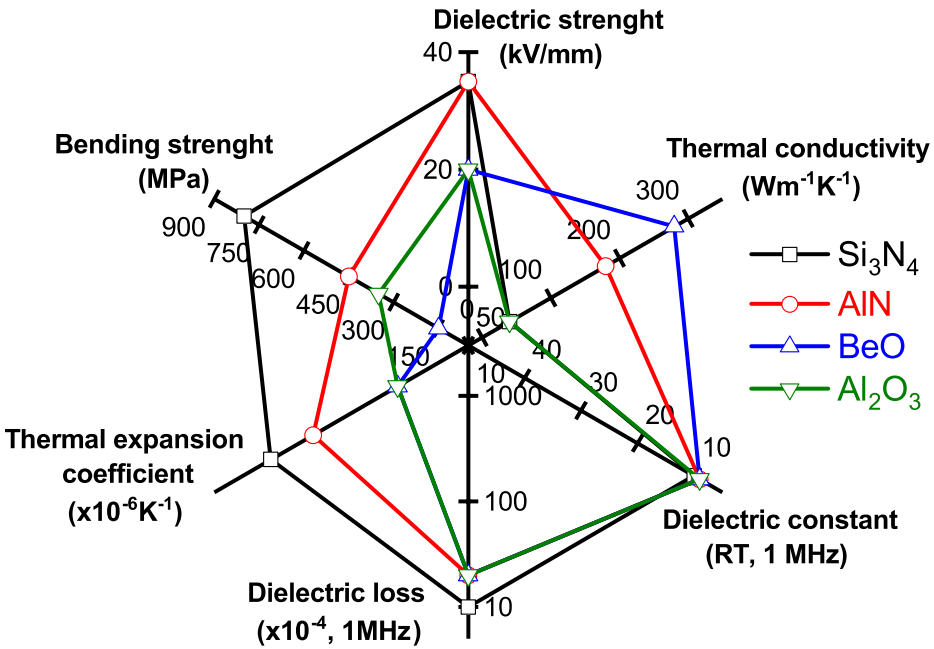


Source: Dielectric properties of ceramic substrates and current developments for medium voltage applications, L. Laudebat et al., MVDC Workshop 2017

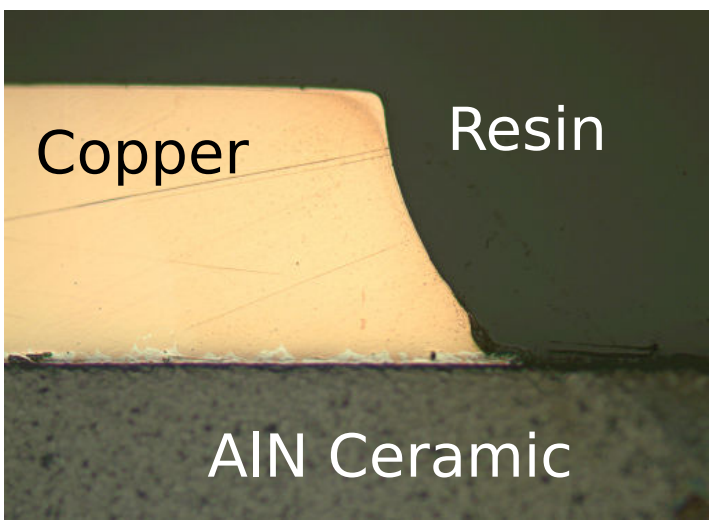
Ceramic materials

- BeO discarded (toxic)
- AlN next best thermal conductivity
- AlN best electrical strength

HV Substrates – Materials and Geometric Issues [24]



Source: Dielectric properties of ceramic substrates and current developments for medium voltage applications, L. Laudebat et al., MVDC Workshop 2017



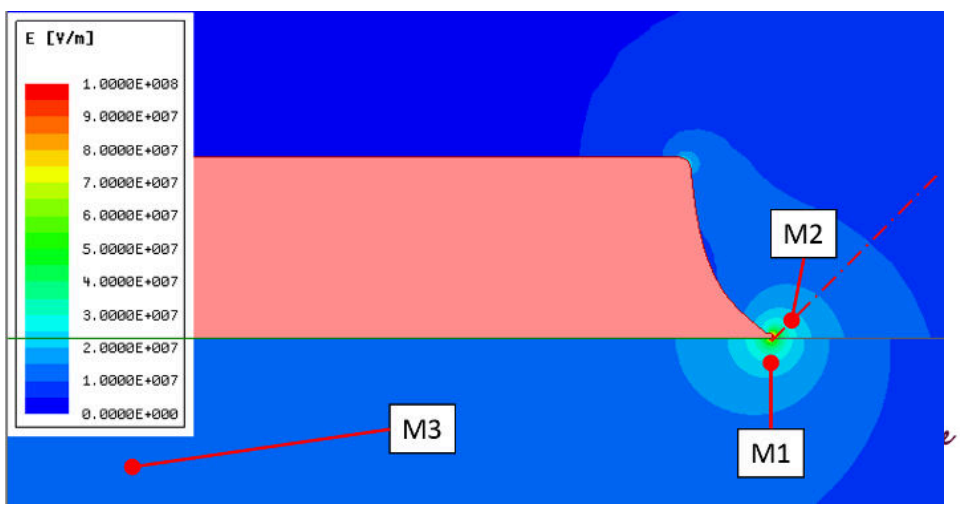
Ceramic materials

- BeO discarded (toxic)
- AlN next best thermal conductivity
- AlN best electrical strength

Substrate structure

- "Triple point"
- Sharp edge of metallization

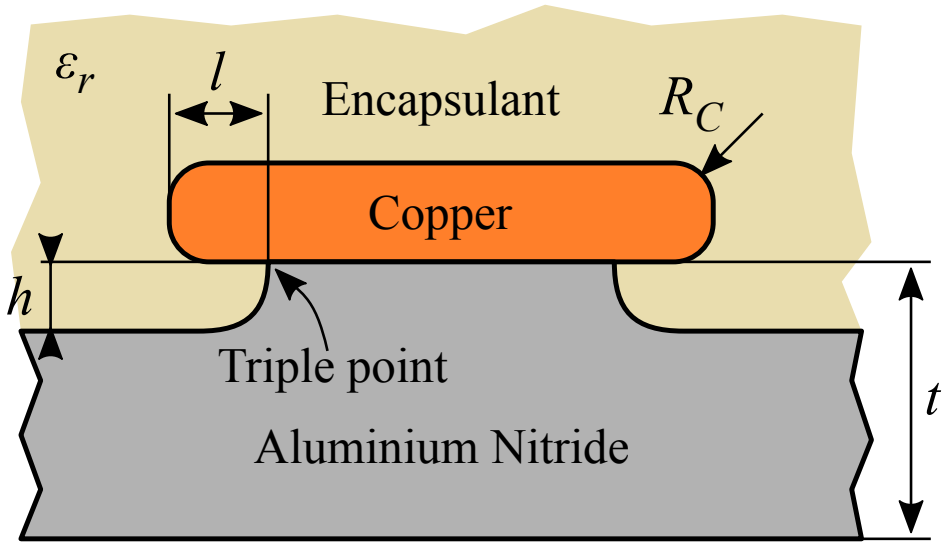
➜ Electric field reinforcement

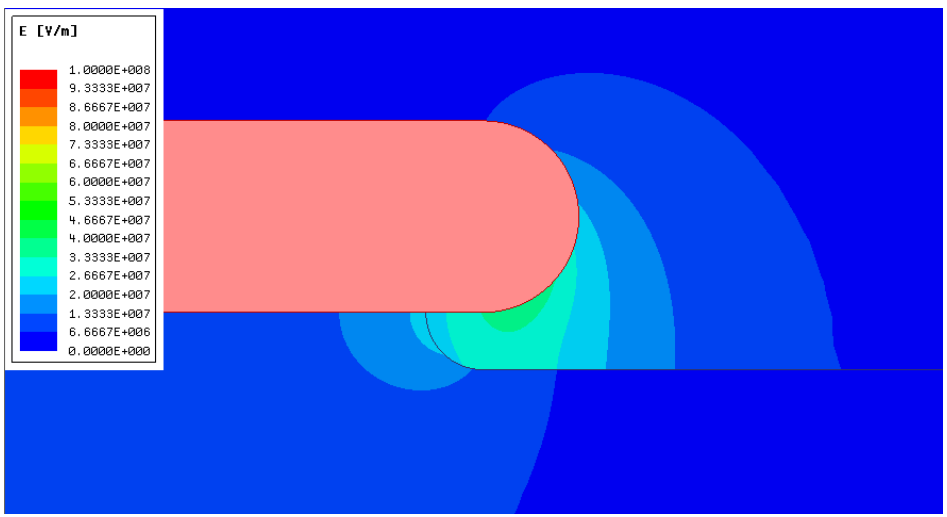


HV Substrates – New Geometry [24]

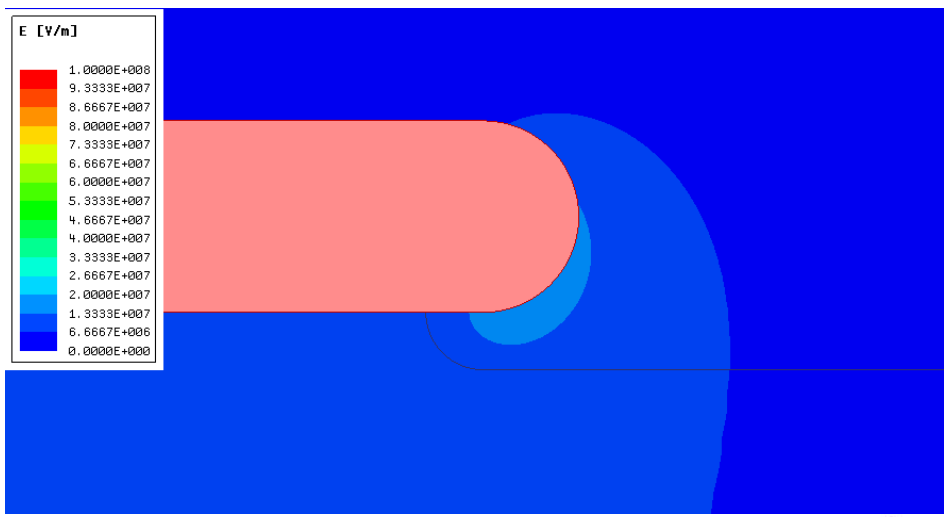
“Protruding” structure

- Shielding of triple point
- Rounded electrodes
- Ideally, encapsulant and ceramic with matched ϵ_R



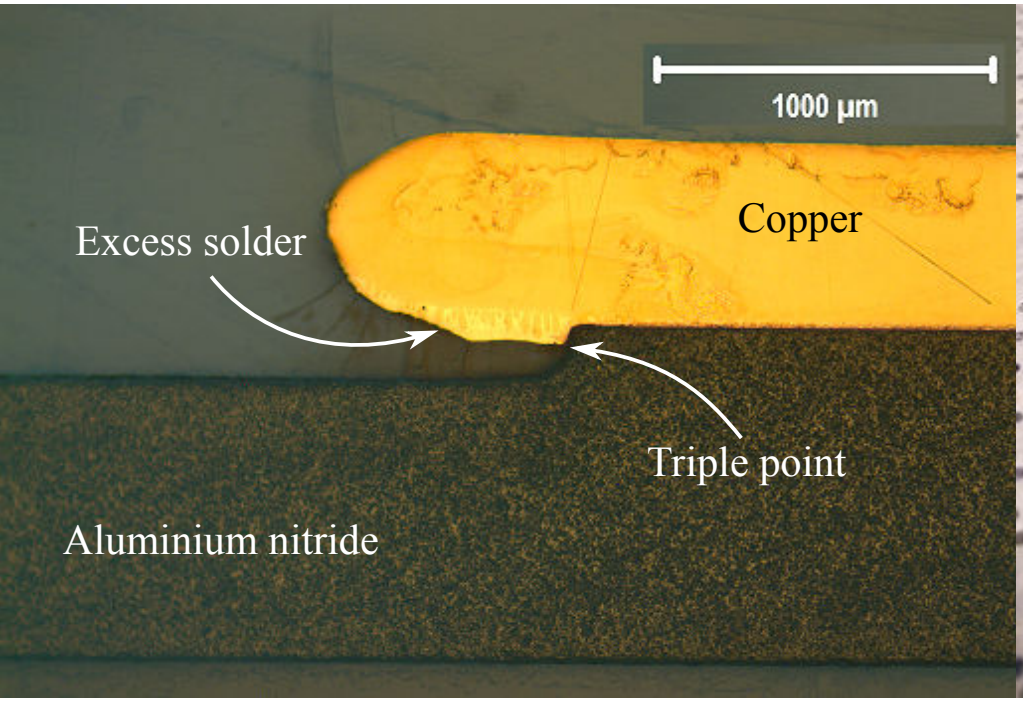


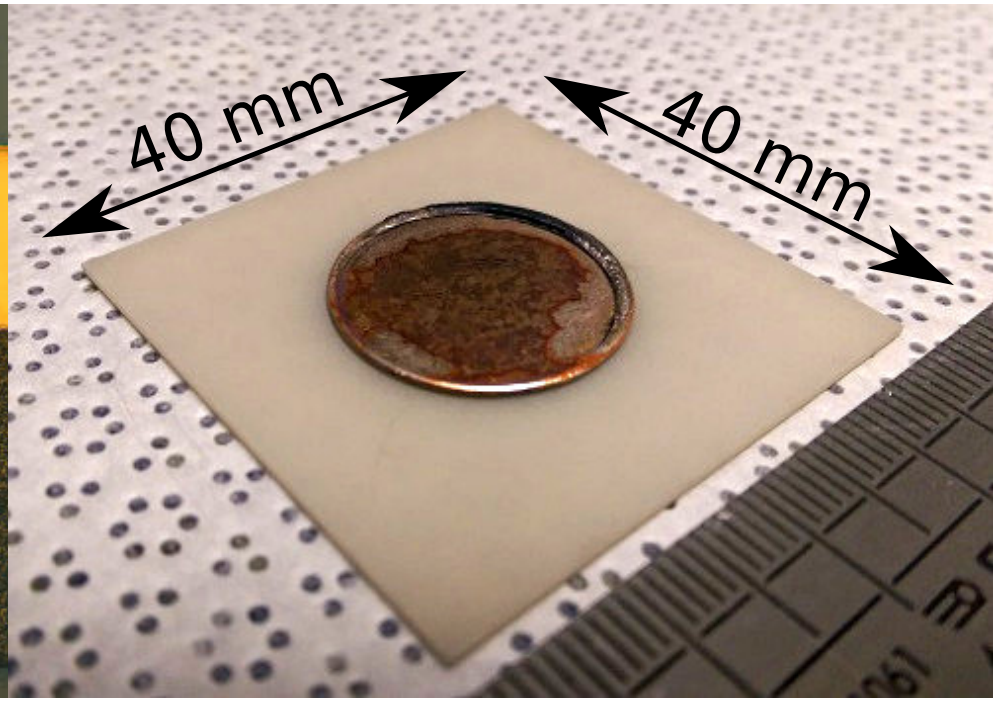
ϵ_R encapsulant=1



ϵ_R encapsulant=9

HV Substrate – Manufacturing [24]

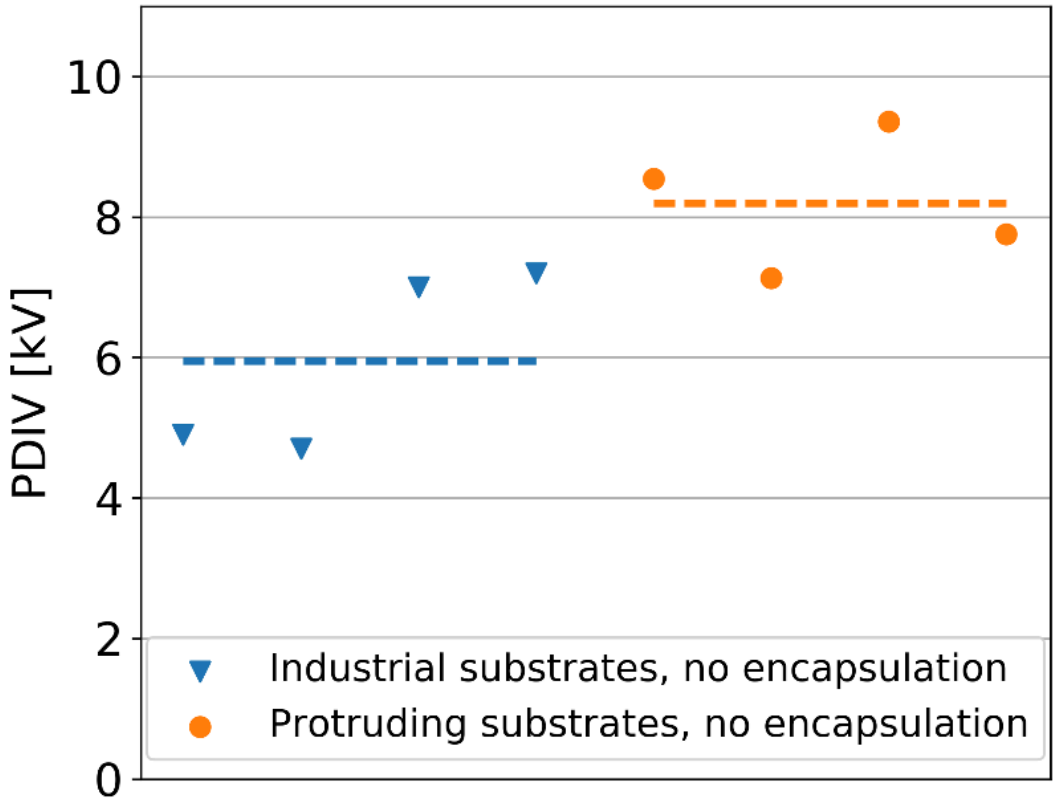




- Active Metal Brazing between ceramic and copper (no voiding observed)
- Excess solder flowed along copper, not ceramic
- Substrate backside coated with Ti/Ag by PVD for testing

HV Substrate – Results and conclusion [24]

- Clear improvement of protruding over “standard” substrate
  - Same total ceramic thickness (1 mm), same ceramic provider



- Further improvement possible:
  - Use of encapsulant with $\epsilon_R \approx 9$ (ϵ_R Novec 649: 1.8)
  - Better manufacturing process (smoother ceramic surface)

Outline

Summary

- Packaging for high temperature, high voltage or high density
  - Ceramic and silver sintering technologies for HT/HV
    - Currently: development of a HVDC "MMC submodule" (A. Boutry)
    - Converter-level rather than pure packaging
  - Printed Circuit board for integration
    - Fully custom designs (no more modules)
    - Embedding to overcome thermal/electrical limitations
- Any of these topics is open for discussion/collaboration
  - Please see me for more information on any of them
  - References at the end of the presentation
- And thanks for your attention!

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Acknowledgements

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