Packaging and Integration Activities at Laboratoire Ampère – CPES Seminar
Cyril Buttay

To cite this version:
Cyril Buttay. Packaging and Integration Activities at Laboratoire Ampère – CPES Seminar. Doctoral. United States. 2019. hal-02968805

HAL Id: hal-02968805
https://hal.science/hal-02968805
Submitted on 16 Oct 2020

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Packaging and Integration Activities at Laboratoire Ampère

CPES Seminar

Cyril BUTTAY

Laboratoire Ampère, Lyon, France

09/06/2019
Who am I?

2004
PhD Electrical Engineering
(Lyon, France)

2005 – 2007
Research associate
(Sheffield and Nottingham, UK)

2008 – 2019
Researcher at CNRS
(Lyon, France)

Since 2019
Senior Researcher (eq. Prof.)
at CNRS

You can contact me at

- cyril.buttay@insa-lyon.fr
- (540) 998 6694
- Office 151, Whittemore Hall
- scholar.google.fr/citations?user=-gMeCUkAAAAJ
- I’m here until July, 2020!
Where do I come from?

- Laboratoire Ampère (named after André-Marie Ampère, born in Lyon)
- 180 people (Faculty, Support, PhD students)
- Academic research lab focusing on:
  - Bio-engineering, biology
  - Automation, System engineering
  - Electrical Engineering
- EE activities:
  - High voltage engineering
  - WBG devices design and test
  - Magnetics (material/design)
  - EMC, Packaging, Integration.

http://www.ampere-lab.fr
Outline

Packaging for High Temperature (> 200 °C)
  Thermal stability of SiC devices
  High Temperature Packaging

New Packaging Structures for Power Modules
  Macro-post
  Micro-Post
  PCB Embedding

Packaging for High Voltage
  Fail-to-short Packaging for SiC
  High Voltage Substrates

Conclusion
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Conclusion
Operating Temperature Limits

Some limits:

- 660°C  Aluminium melts
- ≈ 300°C   Die Solder melts
- 200 – 250 °C  Silicone gel degrades
- ≈ 200°C  Board solder melts

Source: C. Raynaud et al. “Comparison of high voltage and high temperature performances of wide bandgap semiconductors for vertical power devices” Diamond and Related Materials, 2010, 19, 1-6

- For Wide-Bandgap devices, limits set by packaging
- Additional packaging issues with thermal cycling
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High temperature behaviour of SiC devices – [1, 2]

Static Characterization of 490 mΩ JFET

\[ V_{GS} = 0 \, V, \text{ i.e. device fully-on} \]

- Large increase in on-state resistance with temperature;
- Strong sensitivity of conduction losses to temperature.
High temperature behaviour of SiC devices – [1, 2]

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Thermal Run-away mechanism

- The device characteristic
- Its associated cooling system
- Two equilibrium points: one stable and one unstable
- Above the unstable point, run-away occurs
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![Diagram showing thermal run-away mechanism with two equilibrium points: one stable and one unstable.](image-url)
High temperature behaviour of SiC devices – [1, 2]

Thermal Run-away mechanism

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Thermal run-away mechanism

Point of no return

Stable steady-state

Cooling system

Device

Always stable

Always unstable

Becoming unstable with ambient temperature rise
High temperature behaviour of SiC devices – [1, 2]
High temperature behaviour of SiC devices – [1, 2]
High temperature behaviour of SiC devices – [1, 2]

SiC JFET:
- $490 \, \text{m}\Omega, \, 1200 \, \text{V}$
- $R_{Th_{JA}} = 4.5 \, \text{K/W}$
- $135 \, ^\circ\text{C}$ ambient
- On-state losses

High temperature capability $\neq$ reduced cooling needs!
SiC JFETs must be attached to a low-$R_{Th}$ cooling system.
Outono

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High Temperature die attaches

The problem with solders

Homologous temperature:

\[ T_H = \frac{T_{Oper}[K]}{T_{Melt}[K]} \]

Example:

- AuGe solder: \( T_{Melt} = 356^\circ C = 629 \, K \)
- \( T_H = 0.8 \Rightarrow T_{Oper} = 503 \, K = 230 \, ^\circ C \)

- High temperature solder alloys not practical
- Need to decorrelate process temperature and melting point:
  - Sintering (solid state, process below melting point)
  - Diffusion soldering/TLPB (creation of a high melting point alloy)

Source: [http://www.ami.ac.uk/courses/topics/0164_homt/](http://www.ami.ac.uk/courses/topics/0164_homt/)
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High Temperature Die Attaches – PhD A. Masson

► development of the sintering process
► Nano-particles paste from NBE Tech

► Evaluation of many parameters
  ► Sintering pressure
  ► Surface roughness
  ► Thickness of stencil
  ► Substrate finish.

► Once set, process is robust
High Temperature Die Attaches – PhD A. Masson

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High Temperature Die Attaches – PhD A. Masson

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- Evaluation of many parameters
  - Sintering pressure
  - Surface roughness
  - Thickness of stencil
  - Substrate finish...

- Once set, process is robust
“Pressureless” sintering process
- Based on micro-particles
- Findings:
  - Oxygen is necessary
  - Bonding on copper (oxide)
  - Standard Ni/Au finish not ideal
    - Confirmed by several teams
    - Weak bonds at Ag/Au interface
  - Bond strength lower
  - Porosity higher
  - Can be used to attach fragile components
High Temperature Die Attaches – [3]

- All-sintered assembly
- Half-Bridge structure
- SiC JFETs
- Integrated gate drivers (Ampère)
- Ceramic capacitors
- Isolation function not integrated
Causes: electric field, high temperature and oxygen

Large differences between similar test vehicles:

- Short life without encapsulation (100–1000 h)
- Much longer life with parylene HT protection
Causes: electric field, high temperature and oxygen

Large differences between similar test vehicles:

- **Short life without encapsulation** (100–1000 h)
- **Much longer life with parylene HT protection**
SiC devices can operate at high temperature (>300 °C)

- With efficient thermal management!
- $R_{Th}$ must remain low

**Silver sintering** for high temperature die attaches

- Compatible with standard die finishes
- High thermal/electrical performance

**Research**: long-term behaviour at elevated temperature

- Pressureless processes may be a good model
- Not presented here: cycling and storage tests [5, 6, 7]
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Conclusion
New Structures

Wirebond
New Structures

- Wirebond
- Bi-metal Ribbon
- Soldered clip
- Macro Post
- Spacer
- Embossed foil
- Deposited metal
- Pressed interconnect
- Micro posts
- Nano “velcro”
New Structures – for double-side cooling

- Bi-metal Ribbon
- Bumps
- Macro Post
- Spacer
- Pressed interconnect
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New Structures – for double-side cooling – investigated here
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New Structures – Macro post (R Riva) [8, 9]

- Two ceramic substrates, in “sandwich” configuration
- Two SiC JFET dies (SiCED)
- assembled using silver sintering
- 25.4 mm × 12.7 mm (1 in × 0.5 in)
New Structures – Macro post (R Riva) [8, 9]

- Etching accuracy exceeds standard design rules
- Double-step copper etching for die contact
- Custom etching technique

Scale drawing for 2.4×2.4 mm² die
New Structures – Macro post (R Riva) [8, 9]

- Final patterns within 50 µm of desired size
- Two designs, for 2.4 mm and 4 mm dies
  - Die top metallized (PVD) with Ti/Ag
- Total copper thickness 300 µm, ≈ 150 µm per step
New Structures – Macro post \((R \text{ Riva}) [8, 9]\)

- Final patterns within 50 \(\mu m\) of desired size
- Two designs, for 2.4 mm and 4 mm dies
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- Total copper thickness 300 \(\mu m\), \(\approx 150 \mu m\) per step
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New Structures – Macro post (R Riva) [8, 9]

1. **plain DBC board**

1a. **Photosensitive resin coating**

1b. **Exposure and Development**

2. **Etching**

3. **Resin coating**

3a. **Exposure and Development**

3b. **Exposure and Development**

- **Final patterns within 50 µm of desired size**
- **Two designs, for 2.4 mm and 4 mm dies**
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1a - Photosensitive resin coating
1b - Exposure and Development
2 - Etching
3a - resin coating
3b - Exposure and Development
4a - Photosensitive film laminating
4b - Die top metallized (PVD) with Ti/Ag
New Structures – Macro post (R Riva) [8, 9]

- Plain DBC board
- 1a - Photosensitive resin coating
- 1b - Exposure and Development
- 2 - Etching
- 3a - Resin coating
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Two designs, for 2.4 mm and 4 mm dies
  - Die top metallized (PVD) with Ti/Ag

Total copper thickness 300 $\mu$m,
$\approx$ 150 $\mu$m per step
Good form factor achieved using the two-step copper etching process
Satisfying alignment
Poor quality of Al-Cu attach
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Conclusion
First studies during L. MÉNAGER’s PhD

- Copper posts growth on die (electroplating)
- Original die/DBC assembly technology: SnCu diffusion bonding

Proposition of M. SOUEIDAN: direct copper bonding
Direct Copper-to-Copper Bonding [12]

Parameters:
- SPS press
- Cu/Cu bonding
- 5 or 20 min
- 200 or 300°C
- 16 or 77 MPa

- Very good bond, without any interface material
  - All configuration but one yield to bonding
  - Tensile strength 106 to 261 MPa (365 MPa for bulk copper)
- Parameters compatible with the process of a semiconductor die
New Packaging Structures – Micro posts

(B Mouawad) [10, 11]

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New Structures – Micro posts (B MOUAWAD) [10, 11]

- “Wafer”-level process
- Based on copper electroplating
- Assembly of DBC/die/DBC “sandwiches”
- No damage to dies observed
Higher elec. resistance than expected
- Due to seed layer/die topside interface
- Would not happen with suitable dies

Simple and reproducible process
- Tens of samples assembled, with good yield
Conclusions on “Sandwich” ceramic structures

- Several sandwich configurations:
  - Solder [13, 14]
  - Silver sintering
  - Direct Cu/Cu bonding (Micro-posts)

- More suited to direct liquid cooling
  - Solid/liquid interface
  - Homogeneous compressing force
  - No issue with flatness

- Remaining issues:
  - Dies topside finish
  - Mechanical relief structures
  - Intrinsic thermo-mechanical reliability
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- Remaining issues:
  - Dies topside finish
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  - Intrinsic thermo-mechanical reliability
    - Need for further investigation
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Conclusion
Bidirectionnal, Power Factor Converter for 3.3 kW applications

- Designed through an optimization procedure [15, 16]
  - Based on SiC power devices
  - 180 kHz switching frequency
  - 4 interleaved cells

- Discussed here: PFC cell
- **Idea: embed all devices** (not just semiconductor chips)
New Structures – PCB Embedding [17, 18]

Physical Structure

3-PCB structure

- Magnetic component on top
- Heatsink on bottom (natural convection)
- Power chips close to heatsink
Two board structures are used:

**Thin** PBC (1 mm)
for bare dies
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**Thick** PCB (4 mm)  
for SMD devices and inductors
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New Structures – PCB Embedding [17, 18]

- PFC inductor (Thick)
- TIM
- Gate driver (thick)
- TIM
- Power devices PCB (thin)
- Thermal Interface Material (TIM)
- Heatsink

- Board-to-board interconnects using wires soldered in through-holes
- Final cell dimensions: $7 \times 7 \times 3.5 \text{ cm}^3$
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New Structures – PCB Embedding [17, 18]

- 4 PFC cells for a full converter
- DC capacitor bank for test only
- 4-stage EMC DM filter
- 28x7x5 cm³
For SiC dies

- good quality of microvias
  - No damage to dies
  - Uniform thickness
- Good alignment
  - Gate contact 500×800 µm²
- Good electrical perf.
  - Consistent $R_{DS,on}$ (80 mΩ)
  - No change in $V_{th}$
  - Low leakage current (max 1.6 nA @ 1200 V)
  - Very good yield (97% on 44 dies)
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New Structures – PCB Embedding [17, 18]

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Other SMD components OK as well
Operation of the PFC converter

- 4 interleaved PFC cells (target power $4 \times 825 \, \text{W} = 3.3 \, \text{kW}$)
- Operation at reduced power because of losses in inductors
  - Current unbalance because of differences in inductor values
Conclusions – Exploiting the PCB Embedding

- “All-embedded”, interleaved PFC designed
  - includes dies, driver, inductors
  - Very good production yield
  - Only issue: embedded inductors

- Next step: better use of embedding
  - Keep some components on the surface
  - Improve design for manufacturing
  - Improve design tools
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   Thermal stability of SiC devices
   High Temperature Packaging

New Packaging Structures for Power Modules
   Macro-post
   Micro-Post
   PCB Embedding

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   Fail-to-short Packaging for SiC
   High Voltage Substrates

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HVDC Converters

- Rated at 100s kV (ex 320 kV for France-Spain link)
- Series of 100s of transistors (800 for same converter)
- Transistors fail randomly
  - Should not stop converter
  - Failed device turned to short circuit

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Fail-to-Short Packaging for HVDC Applications

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→ Need for Fail-To-Short Packaging

Fail-to-Short Packaging

- Standard packaging: Fail-to-Open
- Wirebonds act as fuses or blown away
- Need for massive contacts

- “Press pack”-type packages introduced
- Initially for single die, now for multichip
- When failure occurs:
  - Temperature rises
  - Die and surrounding metal melt
  - They form a conductive area
  - Strong package contains explosion
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Is a FTS package Possible for SiC?

Fail-to-Short Packaging – test on SiC dies [21]

- Dies fracture because of failure
- SiC and metal remain separate
- Tiny metal filaments form
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Dies fracture because of failure

SiC and metal remain separate

Tiny metal filaments form

→ Fail-to-short behaviour possible with SiC
“Micro-Posts”: massive interconnects
Silver sintering: high temperature bonding
Salient features: for topside contact
## Fail-to-Short Packaging – Test samples [22]

<table>
<thead>
<tr>
<th>Sample</th>
<th>Encapsulant</th>
<th>Clamp</th>
<th>Switch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module A</td>
<td>None</td>
<td>Yes</td>
<td>MOS 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MOS 2</td>
</tr>
<tr>
<td>Module B</td>
<td>Silicone</td>
<td>Yes</td>
<td>MOS 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MOS 2</td>
</tr>
<tr>
<td>Module C</td>
<td>Epoxy</td>
<td>No</td>
<td>MOS 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MOS 2</td>
</tr>
<tr>
<td>Module D</td>
<td>Silicone</td>
<td>Yes</td>
<td>MOS 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>_</td>
</tr>
</tbody>
</table>

- Dies tested individually
- “Clamp” used for modules A, B and D
- MOS 2 of module D not connected
<table>
<thead>
<tr>
<th>Encapsulant</th>
<th>Clamp</th>
<th>Switch</th>
<th>E [J]</th>
<th>R&lt;sub&gt;init&lt;/sub&gt; [mΩ]</th>
<th>R&lt;sub&gt;final&lt;/sub&gt; [mΩ]</th>
<th>Failure mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>A None</td>
<td>Yes</td>
<td>MOS 1</td>
<td>–</td>
<td>186</td>
<td>77</td>
<td>SC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOS 2</td>
<td>8.8</td>
<td>201</td>
<td>128</td>
<td>SC</td>
</tr>
<tr>
<td>B Silicone</td>
<td>Yes</td>
<td>MOS 1</td>
<td>20</td>
<td>165</td>
<td>120</td>
<td>SC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOS 2</td>
<td>1</td>
<td>188</td>
<td>167</td>
<td>SC</td>
</tr>
<tr>
<td>C Epoxy</td>
<td>No</td>
<td>MOS 1</td>
<td>9.7</td>
<td>–</td>
<td>–</td>
<td>OC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOS 2</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>D Silicone</td>
<td>Yes</td>
<td>MOS 1</td>
<td>2.24</td>
<td>180</td>
<td>158</td>
<td>SC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>

- Module C separated during first test, causing open circuit
- All other modules exhibited stable short circuit
Fail-to-Short behaviour with SiC dies requires:
- to prevent the Ceramic tiles from separating
- a strong mechanical clamp/frame
- soft encapsulant probably better for gases to escape

To provide massive interconnects:
- wirebonds would act as fuses
- to supply metal to fill the cracks in the dies
- heat dissipation at failure points helps reducing the resistance
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Considering only conduction losses
\[ P = R_{DS_{on}} I_D^2 \]

Considering only mobility reduction
\[ R_{DS_{on}}(T_J) = R_{DS_{on,273}} \times \left( \frac{T_J}{273} \right)^{2.4} \]

[23]

Strong increase of losses with \( T_J \)

→ Need for Low \( R_{Th} \)/High voltage substrate
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[23]

Strong increase of losses with \( T_J \)

Need for Low \( R_{Th} \)/High voltage substrate
Packaging of SiC dies

- Backside cooling
- Electrical insulation of baseplate
Packaging of SiC dies

- Backside cooling
- Electrical insulation of baseplate

**Ceramic substrate Ensures**

- Electrical insulation
- Heat conduction
Ceramic materials

- BeO discarded (toxic)
- AlN next best thermal conductivity
- AlN best electrical strength

Source: Dielectric properties of ceramic substrates and current developments for medium voltage applications, L. Laudebat et al., MVDC Workshop 2017
Ceramic materials
- BeO discarded (toxic)
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- AlN best electrical strength

Substrate structure
- “Triple point”
- Sharp edge of metallization
- Electric field reinforcement

Source: Dielectric properties of ceramic substrates and current developments for medium voltage applications, L. Laudebat et al., MVDC Workshop 2017
“Protruding” structure

- Shielding of triple point
- Rounded electrodes
- Ideally, encapsulant and ceramic with matched $\varepsilon_R$
Active Metal Brazing between ceramic and copper (no voiding observed)

- Excess solder flowed along copper, not ceramic
- Substrate backside coated with Ti/Ag by PVD for testing
Clear improvement of protruding over “standard” substrate

- Same total ceramic thickness (1 mm), same ceramic provider

Further improvement possible:
- Use of encapsulant with $\epsilon_R \approx 9$ ($\epsilon_R$ Novec 649: 1.8)
- Better manufacturing process (smoother ceramic surface)
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Packaging for high temperature, high voltage or high density

- Ceramic and silver sintering technologies for HT/HV
  - Currently: development of a HVDC “MMC submodule” (A. Boutay)
  - Converter-level rather than pure packaging
- Printed Circuit board for integration
  - Fully custom designs (no more modules)
  - Embedding to overcome thermal/electrical limitations

Any of these topics is open for discussion/collaboration

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