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# A SIMULATION SYSTEM FOR A POWER INSULATED GATE BIPOLAR TRANSISTOR (IGBT) WITH TSUPREM-4 AND MEDICI SIMULATORS

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## ABSTRACT

An effective simulation system with TSUPREM-4<sup>TM</sup> and MEDICI<sup>TM</sup> simulators has been set up in this paper to simulate structures and electrical characteristics, and further to give an optimum design of a power insulated gate bipolar transistor. The latch-up effect of the device is also simulated and analyzed in different practical cases.

## INTRODUCTION

The insulated gate bipolar transistor (IGBT) is a new power switching device developed as a monolithic integration of a MOSFET and a wide base bipolar transistor. The devices have the advantages of operating at much higher current density and higher blocking capability than power MOSFET and bipolar transistors, and are now widely used in the power electronic industry.

TSUPREM-4 is a computer software that simulates the processing steps used in the manufacture of silicon integrated circuits and discrete devices, and MEDICI is a powerful device simulation program that can be used to simulate the distributions of potential and carrier concentrations in both MOS and bipolar devices and to predict its electrical characteristics for any bias condition.

The results reported in this paper were obtained with these two simulators used to simulate the processing steps structure, and further electrical characteristics of an IGBT. Otherwise, we can define a certain structure and manufacturing

processes according to the specifications given by the device users.

## MODEL AND STRUCTURE

A TSUPREM-4 simulator can present a two-dimensional cross-section of a portion of a semiconductor wafer. We define the substrate region as an initial structure with certain width and depth, and the top of the surface is exposed. All the manufacturing processes occur at the top surface. Each region of the structure is divided into mesh of non-overlapping triangular elements. The grid lines are controlled to be fine in the channel region and junction regions and to be coarse in another regions. The choice of simulation models in TSUPREM-4 should be considered before performing any processing steps. The speed and accuracy of the simulation depend strongly on the choice of models. The most fundamental process simulated by TSUPREM-4 is diffusion. In addition to simulating the diffusion of the usual impurities, it can also result in oxidation when performed in an oxidizing ambient. The compress oxidation model is used for the entire process, which simulates viscous flow of the oxide during oxidation.

In accordance with the practical processes, the fabrication steps, such as epitaxy, oxidation, ion implantation, diffusion, deposition, etching, photolithography etc., are simulated by using of relative models in the TSUPREM-4 (TMA 1995). A practical IGBT structure is obtained, which includes some information like concentrations of impurities in every region, contours of p-n junctions, channel length, gate length, configurations of the gate, emitter, and collector, and thicknesses of the gate oxide and the gate polysilicon. Fig. 1 presents cross section view and doping profile in a half cell of an

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<sup>TM</sup> TSUPREM-4 and MEDICI are trademarks of TMA, Inc., Palo Alto, CA 94303-4605, USA

IGBT. The  $p^+$  is collector,  $n_b^+$  is buffer layer,  $n$  is epitaxy layer,  $p$  is p-type well,  $p_e^+$  is enhancement layer,  $n^+$  is emitter. The simulations and analyses below are based on this structure.

All the information about the practical structure from TSUPREM-4 are successfully transported into MEDICI program by means of two special joint commands.

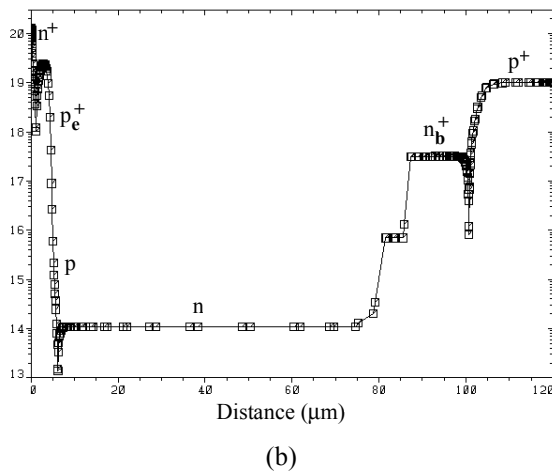
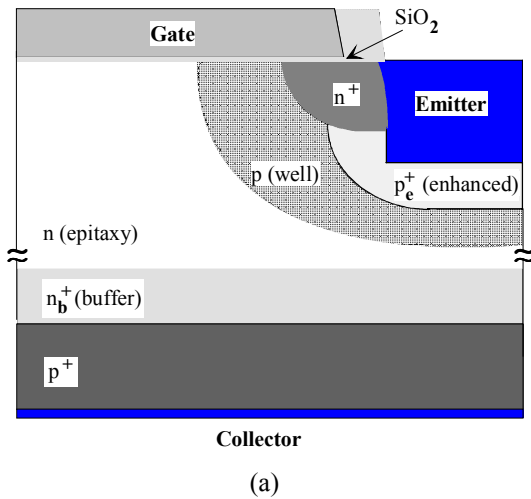


Fig. 1 : Part-sectioned view (a) and doping slice (b) of an IGBT

## ELECTRICAL CHARACTERISTICS

Because the IGBT is a high current and high voltage device controlled by a MOS gate, the effects of the impurity concentration, the temperature, the high field in the silicon bulk, and especially the surface scattering should be taken into account when mobility models are chosen (TMA 1994). The

Shokley-Read-Hall recombination, Auger recombination, and the band-gap narrowing effect are also considered. In addition, the models chosen should be used in cases where the grid spacing at the interface is smaller than the inversion layer width. The electrical characteristics are obtained by solving Poisson's equation and both continuity equations for electrons and holes using the iterative method of incomplete cholesky conjugate gradients (TMA 1994). Fig. 2 and Fig. 3 show gate characteristic and output characteristic of the device at  $T_c = 25^\circ\text{C}$  respectively.

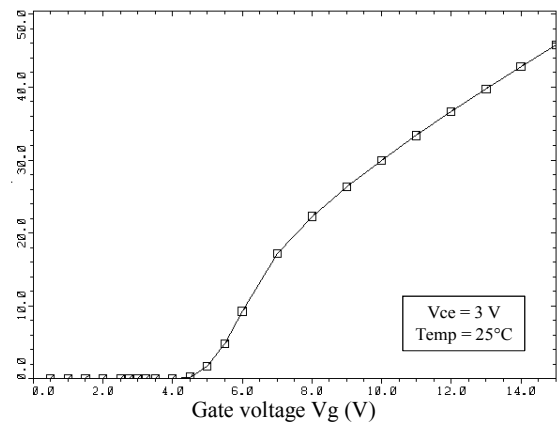


Fig. 2 : Simulated gate characteristic

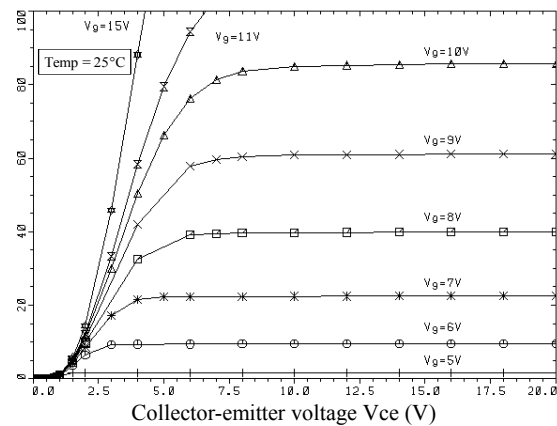


Fig. 3 : Simulated output characteristic

It can be seen that collector current at  $V_{CE} = 3\text{ V}$ ,  $V_{GE} = 15\text{ V}$  is 45.8 A, and the gate threshold voltage is about 4.5 V in figures 2. The forward voltage drop at  $V_{GE} = 15\text{ V}$ ,  $I_{CE} = 45\text{ A}$  is about 3 V in figure 3. Fig. 4 shows the blocking characteristics simulated by considering the carrier generation due to impact ionization which is included in the solution self-consistently. The breakdown voltage of

the device is about 1000 V. These simulation results agree well with the measured ones in table 1.

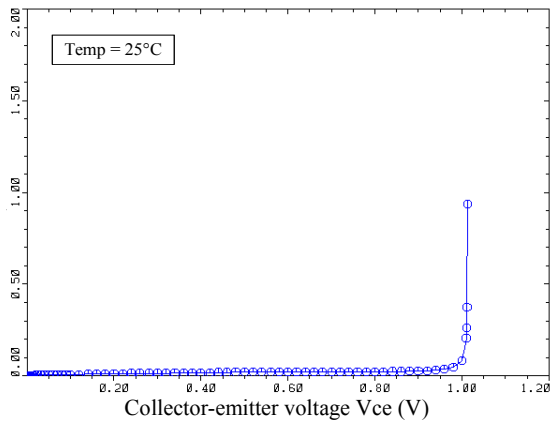


Fig. 4 : Simulated blocking characteristic

Parameters	Symbols	Values
Continuous collector current (Average current)	$I_c$	45 A $V_{CE}=3V, V_{GE}=15V$
Collector-emitter breakdown voltage	$BV_{CES}$	1000V $V_{GE}=0V, I_c=2.0mA$
Gate threshold voltage	$V_{GE(th)}$	3~6V $V_{CE}=V_{GE}, I_c=1.0mA$
Forward voltage drop	$V_{R(ON)}$	2.5~3.2V $V_{GE}=15V,$ $I_{CE}=I_c$

Table 1 : Principal electrical characteristics (measured values) at  $T_c = 25^\circ$ .

### LATCH-UP EFFECT

The presence of the parasitic four-layer thyristor structure in IGBT creates the possibility of the device latching up by regenerative action. The latch-up phenomenon is highly undesirable because it can lead to loss of control of the collector current by the applied gate voltage.

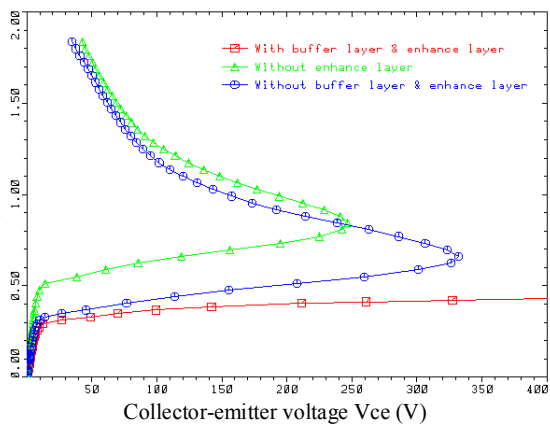


Fig. 5 Simulated latch-up effects with different structures

This phenomenon can be easily found in cases without either of  $n_b^+$  buffer layer and  $p_e^+$  enhancement layer or especially without both of them, and it is difficult to observe in the case with buffer layer and enhancement layer, as shown in fig. 5.

These simulation results were supported by the theoretical analyses (Baliga et al. 1984; Baliga 1987). Fig. 6 and Fig. 7 show the latch-up phenomena at different temperatures and different minority lifetimes in the n-epitaxy layer. It is clear that the latch-up phenomena easily occur at high temperature and large lifetime as theoretical and experimental results (Baliga 1987; Koh et al. 1990; Baliga 1985).

The distribution of current flowlines before and after latch-up in the device are shown in Fig. 8.

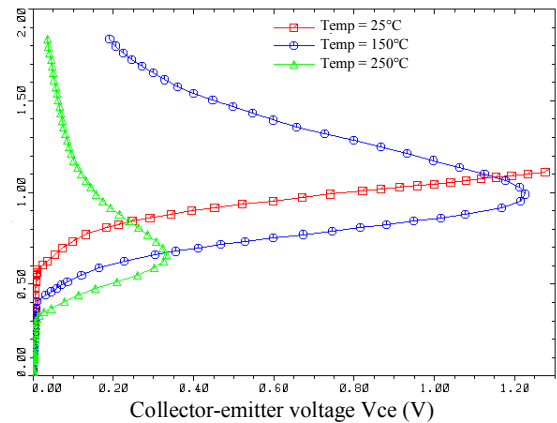


Fig. 6 : Simulated latch-up effects with different temperatures

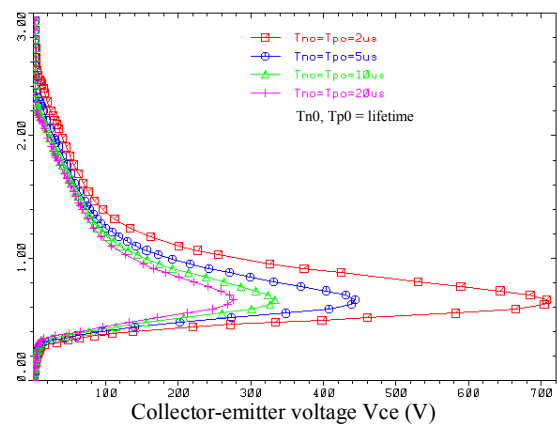
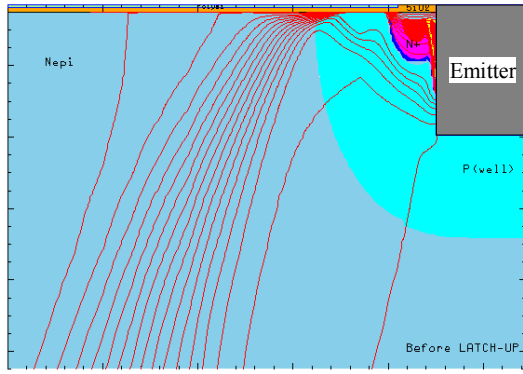
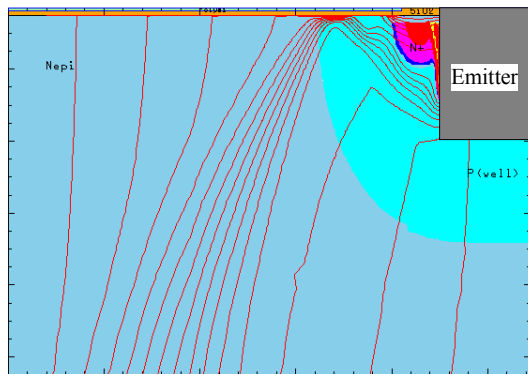


Fig. 7 Simulated latch-up effects with different lifetimes



(a) Before latch-up.



(b) After latch-up

Fig. 8 : 5% current flowlines at  $I_a = 700 \text{ A/cm}^2$

Before latch-up, the main part of current flows through the n-channel like n-MOSFET. Only about 30% current run under the  $n^+$  emitter in the p-well. However, more than 60% current does not pass through the n-channel after latch-up. In this case, the MOS-gate is out of control, and the IGBT has become latched into a thyristor-like conducting state. Therefore, in order to avoid latch-up in an IGBT, a buffer layer and p-enhancement layer should be adopted in the device structure, and operating temperature and minority lifetime in the n-epitaxy layer should be decreased with most possibility.

## DEVICE DESIGN

The electrical characteristics with different parameters from the techniques can be easily obtained with above simulation system. Fig. 9 and Fig. 10 show gate characteristics with different channel lengths and different gate lengths respectively.

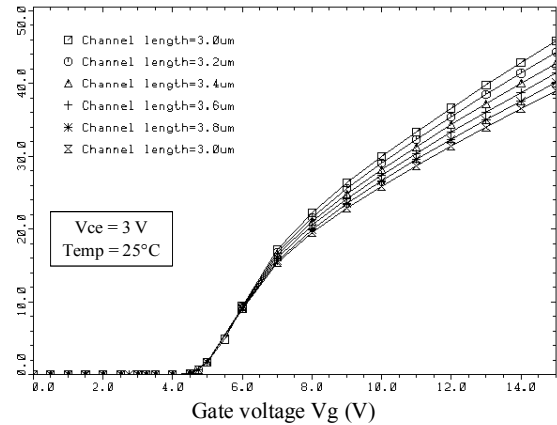


Fig. 9 : Simulated gate characteristics with different channel lengths

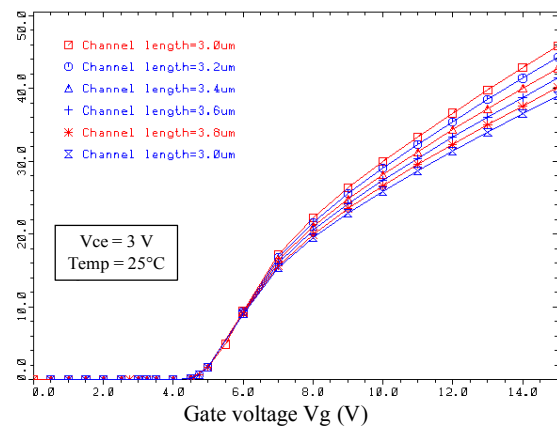


Fig.10 : Simulated gate characteristics with different gate lengths

The current decreases with an increase of channel length, and increases with gate length because forward voltage drop decreases.

In order to get a high current capability, some parts of surface area are enhanced by high doping concentration in simulation. The forward voltage drop decreases with increasing implant dose, as shown in figure 11. A high current value can be obtained when  $V_f$  is fixed. However, the breakdown voltage decreases obviously with implant doses as shown in figure 12.

There is a trade-off between breakdown voltage and forward voltage drop. For example, for a device with high switching speed and low voltage capability, a high implant dose could be chosen to get a low forward voltage drop.

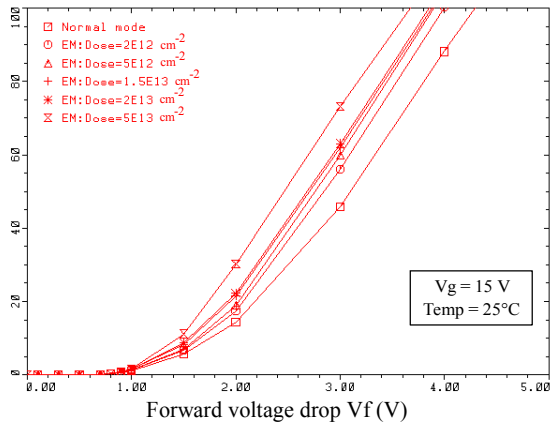


Fig. 11: Simulated forward characteristics with different implant doses

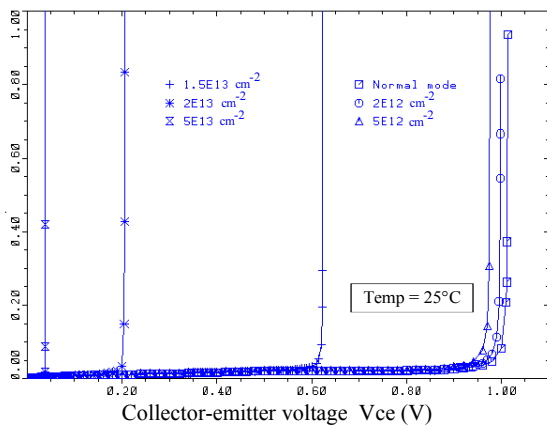


Fig. 12 : Simulated blocking characteristics with different implant doses

## CONCLUSION

The manufacturing processes, structures and electrical characteristics of an IGBT were simulated with both TSUPREM-4 and MEDICI simulators. The simulation results agree with the experimental ones. Using the simulation system, processes and structure can be easily adjusted to obtain optimum design satisfying with user's specifications.

The latch-up effects with different structures, different temperatures and different lifetimes were simulated and analyzed, and some suppression methods for latch-up phenomenon were proposed.

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