Current-sharing control technique for interleaving VRMs with coupled inductors

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Abstract

Parallel converter architecture using intercell transformers is one of the most adapted architecture for low-voltage, high-current and fast transient power conversion applications. Interleaved buck converter with intercell transformers main interest is the current ripple reduction in each converter arms which is not the case with non-coupled inductor architectures. As a consequence, current constraints on switches and inductors are less severe and lower Joule losses are obtained leading to a higher efficiency.
This paper highlights a fundamental limitation for those interleaved converters using intercell transformers. A differential current error through transformer causes flux drift and can lead to magnetic core saturation. In case of temporary control failure, arm currents get back to proper balance with a very slow dynamic response. State-space study allows us to calculate arm current transfer function and deduce the differential current time constant. Finally, a stability study with standard filters is presented and a proper current-sharing loop regulator filter is proposed in order to speed up system return to equilibrium.

Introduction

Many papers deal with current-sharing technique for non-coupled inductor VRM [1]-[6], some with coupled inductor VRM advantages [7]-[14], but none with current sharing technique for VRM with intercell transformers in particular. Our study points out a very slow time constant in response to a differential current pulse. This current imbalance may come from arm property mismatch (switch on-state resistance or inductor DCR mismatch) which causes slow flux drift, or may come from PWM switching control error which causes instantaneous flux drift. Figure 1 shows a 2-arm buck converter with a differential current i flowing through coupled inductors (L_{p1}, L_{p2}). Such a differential current creates power imbalance between converter arms and average flux drift Φ_d.

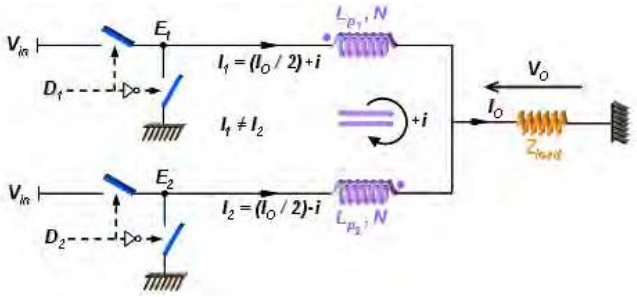

Fig. 1: Differential current error through coupled inductors.

The following formula gives average magnetic flux drift value Φ_d versus average current error i:

$$N \cdot I_1 - N \cdot I_2 = N \cdot (I_0 + i) - N \cdot (I_0 - i) = \Re \cdot \Phi_d \quad \textit{hence:} \quad \Phi_d = \frac{2 \cdot N \cdot i}{\Re} \tag{1}$$

where N is the number of winding turns, I_O is the output current and $\Re$ is the magnetic core reluctance. It should be noted that the differential current mode doesn't modify current and voltage output values. On the contrary, common mode variations affect output values but do not induce differential current error. Even if both differential and common current modes are mixed up together, in this study modes are separated in order to simplify analysis.

An average state-space study of a two-arm buck converter with intercell transformers is presented. This study allows us to determine the exact system open-loop transfer functions for common and differential modes. For current sharing closed-loop regulation purpose, proper corrector filters have to be determined. First, using standard integrator filters, a stability study is presented and emphasizes such filters incompatibility with current regulation for converter using intercell transformers topology. Then, specific filter design is proposed for a fast response and stable current-sharing loop. Finally, simulation results for a four-arm converter with intercell transformers confirm this theoretical average approach.

Differential current mode time constant study

A two-phase buck converter with intercell transformers presented in figure 2 is studied. It can be considered that switching period T_{sw} is much smaller than system time constant. This hypothesis enables to approximate switching cells to average voltage sources: $\mathrm{E}_{1,2} = \mathrm{D}_{1,2} \cdot V_{in}$, with a series equivalent resistance including on-state switching resistor R_{on} and inductor's DCR. $D_{1,2}$ are the arm duty-cycles, and V_{in} the power supply voltage source. Intercell transformer is considered ideal, and basic formulas are:

$$\begin{cases} V_{L1} = L_{p1} \cdot \dot{I}_1 - M \cdot \dot{I}_2 \\ V_{L2} = L_{p2} \cdot \dot{I}_2 - M \cdot \dot{I}_1 \end{cases} \tag{2}$$

where $\mathrm{Lp_i} = \mathrm{Lm_i} + \mathrm{L}\ell_i$ is the inductor, Lm is the magnetizing inductance, $L\ell$ is the leakage inductance and $\mathrm{M} = \sqrt{\mathrm{Lm}_1 \cdot \mathrm{Lm}_2}$ is the mutual inductance. It should be noted that output capacitor equivalent series resistor R_{esr} is considered in the design.

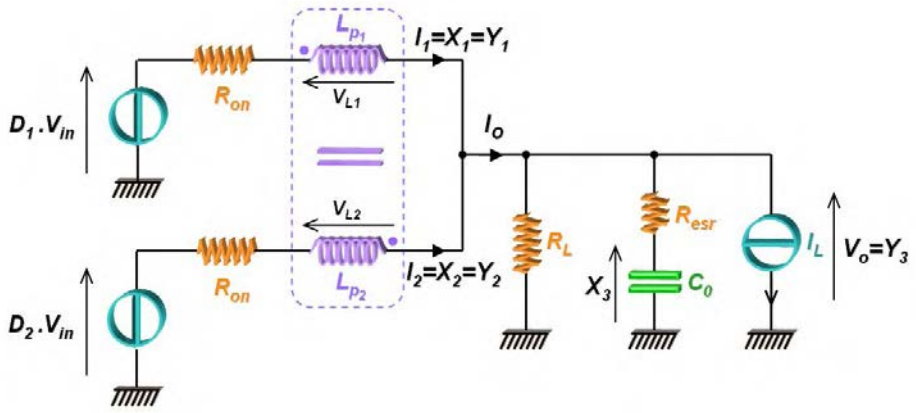

Fig. 2: average behaviour of a two-phase buck converter with intercell transformer

The following set of equation can be deduced from the previous figure:

$$\begin{cases} D_1 \cdot V_{in} = R_{on} \cdot X_1 + Lp \cdot \dot{X}_1 - M \cdot \dot{X}_2 + X_3 + C_o \cdot \dot{X}_3 \cdot R_{esr} \\ D_2 \cdot V_{in} = R_{on} \cdot X_2 + Lp \cdot \dot{X}_2 - M \cdot \dot{X}_1 + X_3 + C_o \cdot \dot{X}_3 \cdot R_{esr} \\ I_L = X_1 + X_2 - \dfrac{X_3 + C_o \cdot \dot{X}_3 \cdot R_{esr}}{R_L} - C_o \cdot \dot{X}_3 \end{cases} \quad (3)$$

From this circuit (fig.2), an equivalent state-space study, allowing exact differential current mode transfer function determination is presented. The average state-space representation enables much more complex system studies, for instance the case of n-arm buck converter with intercell transformers.

Set of equation (3) related to open-loop electrical circuit (Fig. 2) allow us to determine the open-loop state-space representation. Indeed, it can be described with the following matrix equation:

$$[E] = [R] \cdot [X] + [LM] \cdot \left[\dot{X}\right] \quad (4)$$

where $[E] = \begin{bmatrix} D_1 \cdot V_{in} \\ D_2 \cdot V_{in} \\ I_L \end{bmatrix}$ is the exciting vector, $[X] = \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ V_C \end{bmatrix}$ is the system state variable vector composed of arm current and output capacitor voltage,

$[R] = \begin{bmatrix} Ron & 0 & 1 \\ 0 & Ron & 1 \\ 1 & 1 & \dfrac{-1}{R_L} \end{bmatrix}$ and $[LM] = \begin{bmatrix} Lp & -M & C_o \cdot R_{esr} \\ -M & Lp & C_o \cdot R_{esr} \\ 0 & 0 & -C_o \cdot \left(\dfrac{R_{esr}}{R_L} + 1\right) \end{bmatrix}$ are the impedance matrix.

From this point, classic matrixes for state equation are deduced:

$$\left[\dot{X}\right] = [A] \times [X] + [B] \times [E] \quad (5)$$

with $[A] = -[LM]^{-1} \cdot [R]$ and $[B] = [LM]^{-1}$

where [A] and [B] are respectively the state and input matrix. Assuming: $R_{eq} = R_L \,//\, R_{esr}$, $Lm_1 = Lm_2 = Lm$ and $L\ell_1 = L\ell_2 = L\ell$, it follows:

$$[A] = \begin{bmatrix} -\dfrac{(Lm + L\ell) \cdot R_{on}}{L\ell \cdot (L\ell + 2 \cdot Lm)} - \dfrac{1}{L\ell} \cdot R_{eq} & -\dfrac{Lm \cdot R_{on}}{L\ell \cdot (L\ell + 2 \cdot Lm)} - \dfrac{1}{L\ell} \cdot R_{eq} & \dfrac{1}{L\ell} \cdot (R_{eq} - 1) \\ -\dfrac{Lm \cdot R_{on}}{L\ell \cdot (L\ell + 2 \cdot Lm)} - \dfrac{1}{L\ell} \cdot R_{eq} & -\dfrac{(Lm + L\ell) \cdot R_{on}}{L\ell \cdot (L\ell + 2 \cdot Lm)} - \dfrac{1}{L\ell} \cdot R_{eq} & \dfrac{1}{L\ell} \cdot (R_{eq} - 1) \\ \dfrac{R_L}{R_L + R_{esr}} \cdot \dfrac{1}{C_o} & \dfrac{R_L}{R_L + R_{esr}} \cdot \dfrac{1}{C_o} & -\dfrac{1}{C_o \cdot (R_L + R_{esr})} \end{bmatrix};$$

$$[B] = \begin{bmatrix} \dfrac{(Lm + L\ell)}{L\ell \cdot (L\ell + 2 \cdot Lm)} & \dfrac{Lm}{L\ell \cdot (L\ell + 2 \cdot Lm)} & \dfrac{1}{L\ell} \cdot R_{eq} \\ \dfrac{Lm}{L\ell \cdot (L\ell + 2 \cdot Lm)} & \dfrac{(Lm + L\ell)}{L\ell \cdot (L\ell + 2 \cdot Lm)} & \dfrac{1}{L\ell} \cdot R_{eq} \\ 0 & 0 & \dfrac{-R_L}{R_L + R_{esr}} \cdot \dfrac{1}{C_o} \end{bmatrix} \quad (6)$$

Now, a closed-loop state-space representation is presented figure 3.

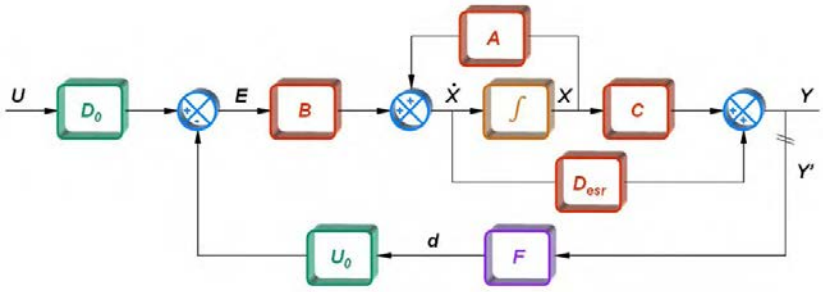

Fig. 3: State-space representation of the closed-loop system

In this system, F matrix stands for corrector filters used to reach expected values. This matrix implements filters for a correct current sharing regulation.
Matrix expressions system is deduced from equation (5) related to closed-loop state-space representation (Fig. 3).

$[U]=\begin{bmatrix} V_{in} \\ I_L \end{bmatrix}$: Input vector. $[E]=[D_0]\cdot[U]-[U_0]\cdot[d]$, hence: $[E]=\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}=\begin{bmatrix} (D_{01}-d_1)\cdot V_{in} \\ (D_{02}-d_2)\cdot V_{in} \\ I_L \end{bmatrix}$: Exciting vector.

$[d]=\begin{bmatrix} d_1 \\ d_2 \end{bmatrix}$: Duty cycle variation vector composed of the duty cycle variations for each phase.

$[C]=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$, $[D_{esr}]=\begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_{esr}\cdot C_o \end{bmatrix}$: Output matrix building output vector $[Y]$. $[D_{esr}]$ adds voltage across R_{esr} to the voltage output capacitor C_O in order to obtain output voltage.

$[D_0]=\begin{bmatrix} D_{01} & 0 \\ D_{02} & 0 \\ 0 & 1 \end{bmatrix}$: Reference duty cycle matrix for each phase; $[U_0]=\begin{bmatrix} V_{in} & 0 \\ 0 & V_{in} \\ 0 & 0 \end{bmatrix}$ is the power supply matrix.

$[F]=\begin{bmatrix} K_{i_1}(s) & 0 & K_v(s) \\ 0 & K_{i_2}(s) & K_v(s) \end{bmatrix}$: Control matrix composed of current filters $K_{i_i}(s)$ and voltage filter $K_v(s)$.
s is the Laplace variable. This matrix provides the duty cycle variation vector [d]. Each duty cycle d_i is the addition of the voltage loop correction given by filter $K_v(s)$ (common mode component) and the current sharing correction given by filters $K_{i_i}(s)$ (differential mode component).

In order to determine filter design, the system open-loop transfer function has to be calculated.
Open-loop transfer function $H_{YY'}(s)$ is deduced when loop is opened on the diagram (fig.3) between output vectors [Y] and input variation vector [Y'].
State variable matrixes are:

$[Y]=\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \end{bmatrix}=\begin{bmatrix} I_1 \\ I_2 \\ V_O \end{bmatrix}$: Output vector composed of current through each phase and output voltage.

$[Y']=\begin{bmatrix} Y'_1 \\ Y'_2 \\ Y'_3 \end{bmatrix}$: Input variation. It is composed of small-signal variations.

$H_{YY'}(s)$ is a 3×3 matrix built in order to observe [Y'] small-signal variation impact on output vector [Y]
Its expression is:

$$[H_{YY'}] = ([C] + [D_{esr}] \cdot s) \cdot ([I] \cdot s - [A])^{-1} \cdot [B] \cdot [U_0] \cdot [F] \quad (7)$$

where [*I*] is the identity matrix.
In that study case, input vector [*U*] is null.

[*Y*] vector is related to [*Y'*] vector through [$H_{YY'}$] matrix as described bellow:

$$\begin{bmatrix} Y_1 \\ Y_2 \\ Y_3 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} & h_{13} \\ h_{21} & h_{22} & h_{23} \\ h_{31} & h_{32} & h_{33} \end{bmatrix} \times \begin{bmatrix} Y'_1 \\ Y'_2 \\ Y'_3 \end{bmatrix} = [H_{YY'}] \times [Y'] \quad (8)$$

where h_{ij} are the matrix terms of the open-loop transfer function.

For a small signal differential variation i flowing through arm inductors (see fig.1), one can note $Y'_1=+1$, $Y'_2=-1$ and $Y'_3=0$. The obtained value of small-signal vector *Y* in that case can be noted:
$Y(s) = H_{ol\ diff}(s).Y'(s)$
With:

$$H_{ol\ diff}(s) = h_{11} - h_{12} = h_{21} - h_{22} = \frac{\frac{V_{in}}{R_{on}}}{\frac{2 \cdot L_m + L\ell}{R_{on}} \cdot s + 1} \cdot K_i(s) = H_{diff}(s) \cdot K_i(s) \quad (9)$$

$H_{ol\ diff}(s)$ is the open-loop transfer function deduced from $H_{YY'}$ for a current differential mode stimulus.

$$H_{diff}(s) = \frac{\frac{V_{in}}{R_{on}}}{\tau_{coupled} \cdot s + 1}$$

$H_{diff}(s)$ is a first order transfer function with high gain and very low time constant. Then, as R_{on} is taken as low as possible, $\tau_{coupled}$ can reach very high values.
However, it should be noted that $H_{diff}(s)$ gain-bandwidth has a constant value whatever the R_{on} value.

$H_{YY'}$ matrix can also allow us to determine voltage loop transfer function. We consider a perfect current balance in order to observe a common mode impact on Y_3 generated by Y'_3 small signal voltage source. For a small signal common mode variation, one can note $Y'_1=Y'_2=0$ and $Y'_3=1$. The obtained value of small-signal vector *Y* in that case can be noted:
$Y(s) = H_{ol\ com}(s).Y'(s)$
With:

$$H_{ol\ com}(s) = h_{33} \cong \frac{V_{in} \cdot (1 + R_{esr} \cdot C_O \cdot s)}{\left(1 + \frac{R_{esr}}{R_L}\right) \cdot C_O \cdot \frac{L\ell}{2} \cdot s^2 + \left(\left(R_{esr} + \frac{R_{on}}{2}\right) \cdot C_O + \frac{L\ell}{2 \cdot R_L}\right) \cdot s + 1} \cdot K_v(s) \cong H_{com}(s) \cdot K_v(s) \quad (10)$$

It is important to note that the transfer function has been simplified considering that $R_L >> R_{on}$ and $R_L >> R_{esr}$.
$H_{com}(s)$ is a second order transfer function similar to a two-arm buck converter transfer function without intercell transformer. In that case, leakage inductance $L\ell$ is replaced by the inductor *L*. The study of voltage filter $K_V(s)$ is well-known.

Current sharing loop filter design

As presented in equation 1, magnetic core flux is proportional to the differential current error *i*. The regulator must quickly cancel the differential current error so that the magnetic core will not saturate.

A local current regulation is proposed in order to avoid slow dynamic response due to large current differential time constant $\tau_{coupled}$. It is based on the current-sharing technique. It consists in comparing each sensed current I_i with the average arm current I_O/n, and cancelling error ε_i between the currents

with specific regulators $Ki_i(s)$ by correcting each phase duty cycle d_i. The local current correction d_i is added to the global average duty cycle D which is provided by a classic voltage loop. As mentioned in specific control circuit datasheets [6], current-sharing loop bandwidth f_{cI} is at least one decade lower than the voltage loop bandwidth f_{cV} in order to cancel the interaction between the two loops.

Common mode is regulated through the voltage loop and differential mode errors are corrected by means of current loop filters. This principle is illustrated in figure 4 with an n-arm buck converter with intercell transformers.

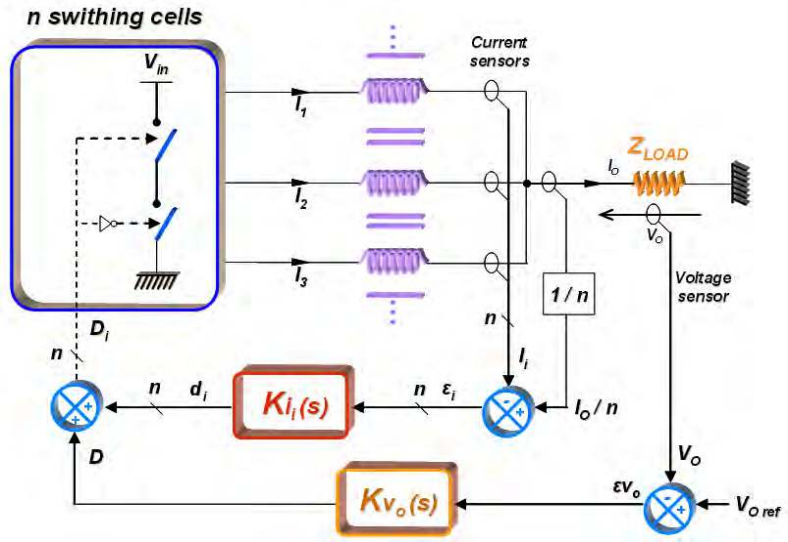

Fig. 4: current sharing and voltage regulation for n-arm buck converter.

$H_{diff}(s)$ has been calculated previously by mean of state space study. Now, $Ki_i(s)$ must be determined in order to balance arm currents.
A simple proportional correction is not suitable because it can lead to an important steady state error. Figure 5 describes two cases of simple integrator correction, one with a low cut off frequency (case A) and the other with a high cut off frequency (case B). Each integrator filter is added to $H_{diff}(s)$ transfer function illustrated by solid-line curve. As a result two open-loop transfer functions (dashed lines) are obtained H_{oldiff_slow} and $H_{oldiff\_unstable}$.

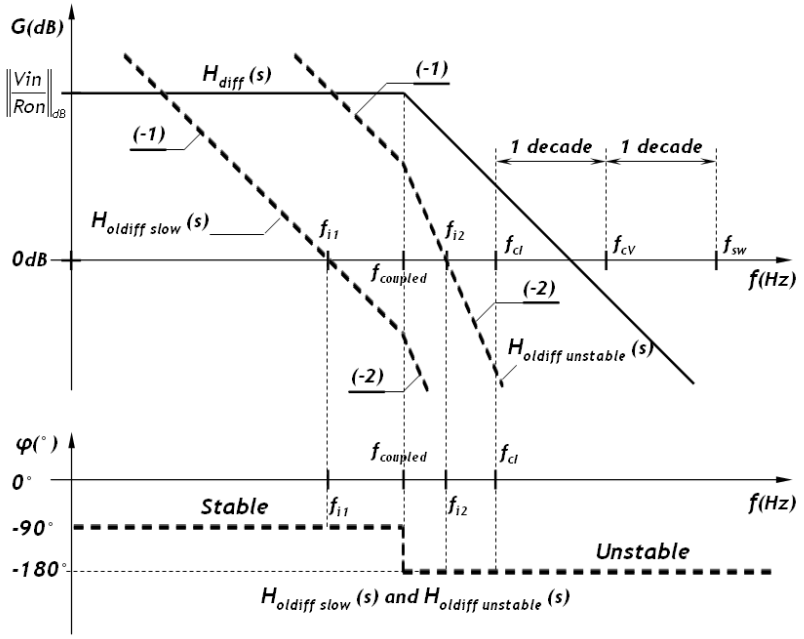

Fig. 5: Bode diagram of current differential transfer function (solid-line) and two open-loop transfer function using integrator corrector filters (dashed-line).

On the one hand, if the integrator cut off frequency is low, current error cancelling is stable but slow. On the other hand, if the integrator cut off frequency is higher than $f_{coupled} \Big/ \left(\frac{V_{in}}{R_{on}} \right)$, current error cancelling is unstable (as shown in figure 5). Then, basic integrator filters are not suitable for a fast and stable differential mode correction.

In order to improve $H_{ol\ diff}$ time response, a lead and lag filter is proposed figure 6. It allows us to fix the expected cut off frequency and to cancel steady state error with a very high DC gain. Cut off frequency doesn't depend on R_{on} value. Moreover, system is unconditionally stable. Open-loop transfer function $H_{ol\ diff}(s)$ (dashed line) is obtained by adding differential mode transfer function $H_{diff}(s)$ (solid line) to lead and lag filter $Ki(s)$ (dotted line).

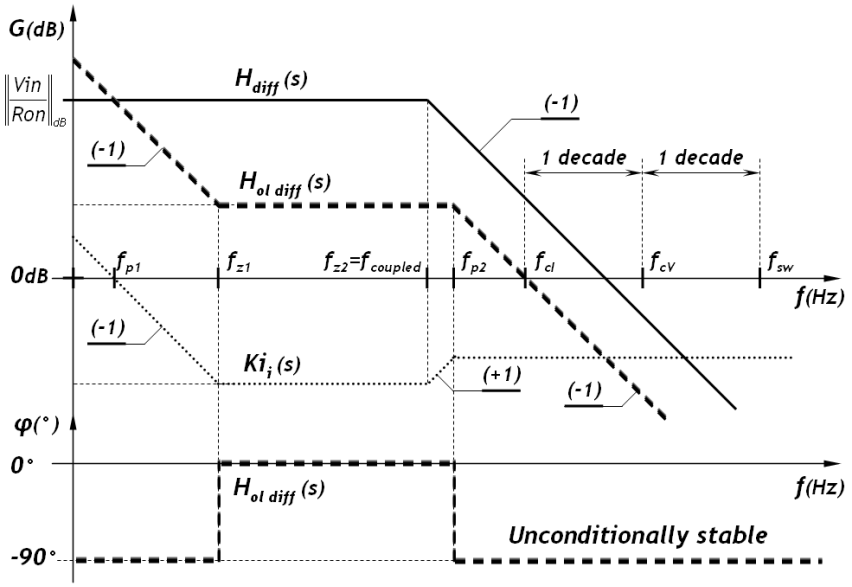

Fig. 6: Bode diagram of open-loop current differential transfer function (dashed-line) using a lead and lag corrector filter (dotted-line).

Simulation results

In order to validate state-space study and filter design, a four coupled-arm buck converter is studied. Figure 7 shows this converter electrical scheme in cyclic cascade configuration [13]. Even arms number is chosen because it is the only configuration permitting perfect differential mode in a cyclic cascade configuration. On the contrary, odd arms number automatically generates a common mode if differential current error occurs.

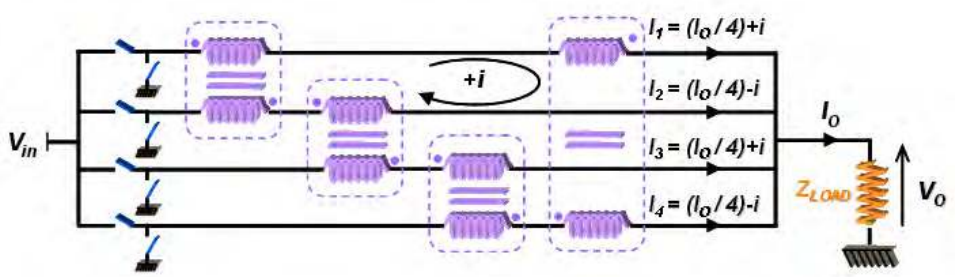

Fig. 7: Electrical scheme of a four coupled-arm buck converter in cyclic cascade configuration

The parallel converter presented in figure 7 consists of four switching cells with interleaved switching control commands. Switches on-state resistor: $R_{on} = 10\,m\Omega$, inductor DCR is considered insignificant compared with R_{on}, power supply: $V_{in} = 12\,V$. As voltage loop is not the point of this article, load is a simple resistance $R_O = 8\,m\Omega$. Then output current is: $I_O = 112\,A$ and voltage output: $V_O = 0{,}9\,V$. Inductors have all the same values: $L_m = 558\,nH$, $L_\ell = 80\,nH$.

Figure 7 differs from electrical scheme presented in figure 2. Indeed, in this architecture, two intercell transformers appear in each arm. Identical previous state space study, applied to this converter, shows that differential time constant is two times higher than figure 2 simple case. Other equation components are the same. Following cyclic cascade configuration differential current time constant $\tau_{coupled\ cyclic}$ can be computed:

$$\tau_{coupled\ cylic} = 2 \cdot \tau_{coupled} = 240\,\mu s \tag{11}$$

In order to validate theoretical result obtained for $H_{diff}(s)$ and closed-loop behaviour using lead and lag corrector filter, simulations are done under *Orcad-PSpice*™ environment.
Figure 8 provides simulation results for a cyclic cascade converter in open-loop configuration. Because of perfectly balance system, differential current error is quickly obtained by keeping open high side switches of the arms 1 and 3 during one switching period. This event occurs at time t=100µs when steady state is reached. Differences between arm currents are observed. As described in equation 1, flux drift is proportional to current error signal *I1-I2*.

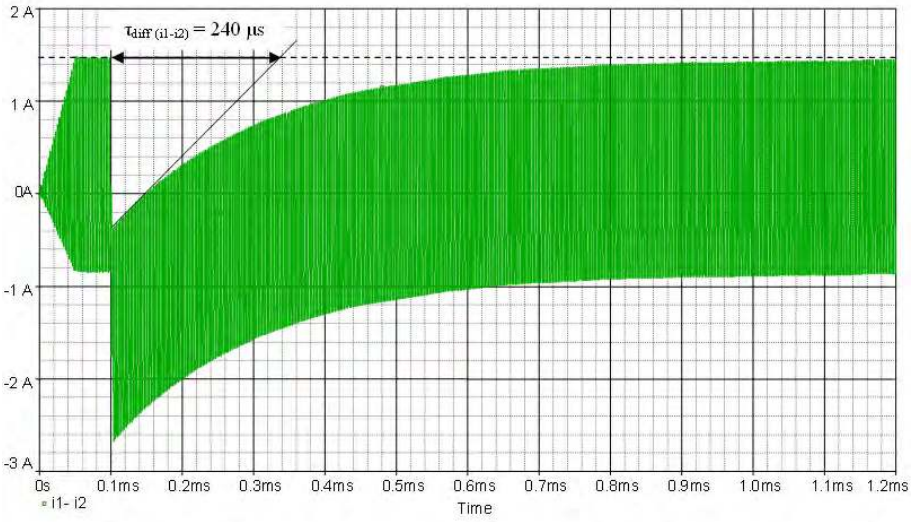

Fig. 8: Open loop simulation

Differential time constant measurement provides the same value than the theoretical one. This time constant is high. Depending on inductor value and ON-state switch resistance, it can be higher and reach few milliseconds.

Now, closed loop simulations are achieved considering block diagram presented in figure 4. Voltage loop is not designed and average duty cycle *D* is a constant parameter. Open loop unity-gain cut off frequency is calculated two decades lower than switching frequency, and its expected time constant is: $\tau_{c1} = 40\mu s$.

First, a high cut off frequency integrator corrector filter is used. Transfer function $H_{oldiff\_unstable}(s)$ of figure 5 is obtained. A closed loop simulation is performed and provides results shown on figure 9.

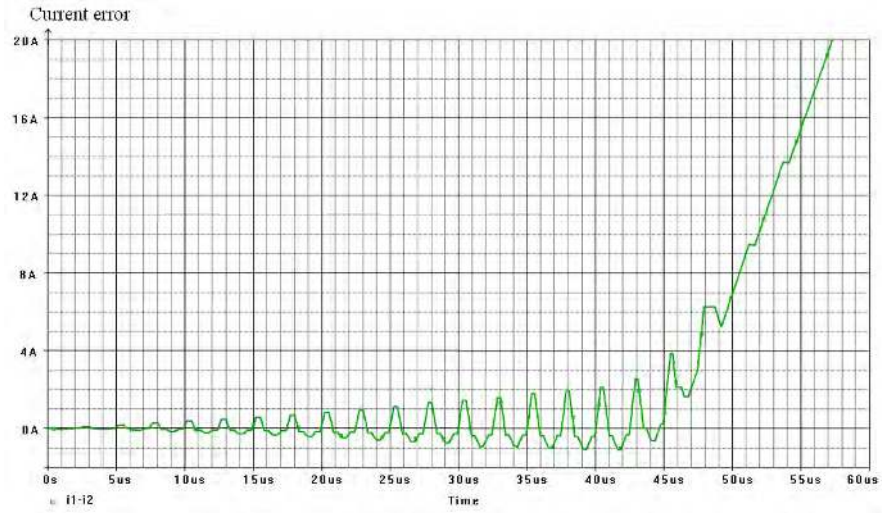

Fig. 9: Closed loop simulation with a high cut off frequency integrator corrector filter

As expected in the filter design section, too high cut off frequency integrator leads to system instability and magnetic core flux saturation. In this simulation, magnetic core saturation limit are not considered.

Then, a proper lead and lag corrector filter is used. Transfer function $H_{ol\ diff}(s)$ of figure 6 is obtained. With the same $\tau_{c1} = 40\mu s$, a closed loop simulation is performed and provides results shown on figure 10.

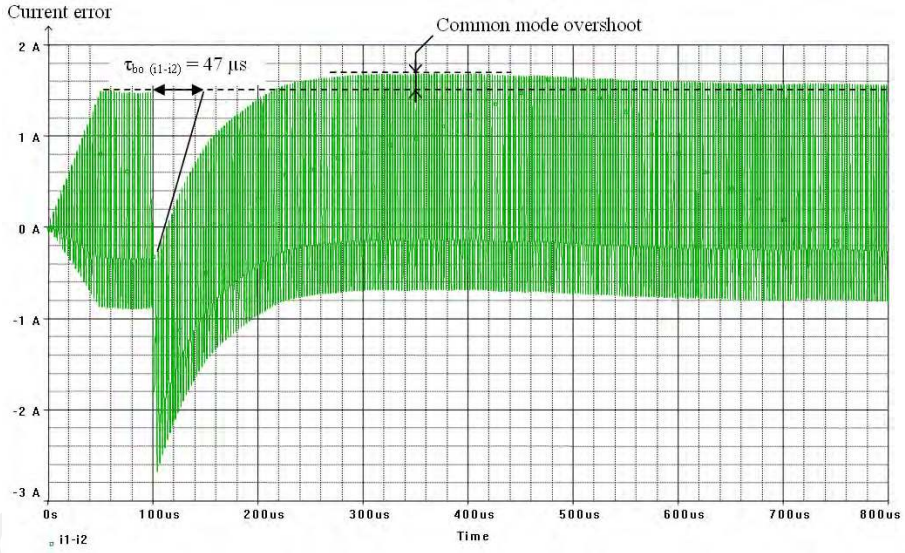

Fig. 10: Closed loop simulation with a proper PI corrector filter

The obtained time response is not exactly equal to τ_{c1} but average flux cancelling is well accelerated in comparison with open loop simulation. A slight overshoot is observed but regulation keeps stable. Those slight differences with theory can be explained by the presence of common mode component which is due to method used to get current arm mismatches. Interaction between differential and common modes currents through intercell transformers induces the observed overshoot on simulation.

Conclusion

Full theoretical state-space study of interleaved intercell transformers converter is achieved. It allows us to determine system time response in open-loop configuration when differential current mode occurs. This very high time response, linked to inductor and arm resistance values, can lead to prohibitive (unpractical) behaviour for unbalance systems. For current sharing regulation purpose,

several types of corrector filter are studied. Standard proportional or integrator filter incompatibility is demonstrated. Lead and lag corrector filter is proposed. Very fast differential current time response and stable regulation are obtained. Using this stable and fast current sharing regulation, average flux drift and magnetic core saturation are avoided.

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