New Masterless Modular Current-Sharing technique for DC/DC Parallel converters

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***Abstract*— This article presents a new Masterless Modular Current-Sharing (MMCS) technique. Current-sharing modules are identical and placed in a daisy chain configuration. Unlike classical current sharing which consists in comparing each phase current to a global computed average value, the presented masterless approach computes local current average values. Phase currents' balancing is achieved by comparing each phase current with the average value of its adjacent phase currents. This technique is validated by a mathematical demonstration and compared with the classical current sharing technique. MMCS approach is adapted to DC/DC Parallel converters with coupled inductors. Such topologies require extremely precise current-sensing technique. An accurate differential current-sensing technique with fluxgate sensor is proposed and applied to MMCS technique. Filters design and its architecture for current sharing loop are explained. Finally, experimentation on a six-phase DC/DC converter with coupled inductors is achieved and validates both MMCS and differential current sensing techniques.**

***Keywords*—Load sharing control, Voltage Regulator Module, Converter control, Interleaved converters.**

I. Introduction

Interleaved DC/DC multi-phase converters are frequently used in systems which require low supply voltage, high output current and fast load transients response, because of many advantages such as load current distribution among phases, lower inductive energy storage, reduced switching ripple in the input and output filter.

In DC/DC multi-phase converters, a currents imbalance is a result of power stage resistive path mismatches, variations caused by several junction temperature presences, non-identical connections from the converters to the shared load and turn on/off times mismatches of power MOSFETs. The current imbalance may result in increased current or thermal stresses on the components.

A number of current-sharing approaches have been proposed in the literature [1-9], those methods use analog or digital controller.

No real masterless current-sharing method with analog implementation has been proposed yet. However, method commonly referred to as 'democratic', 'autonomous' or 'single wire' [2,3] are not so different from masterless approach since they do not require specific central circuit to compute average current and have very good modularity. In these cases, the average current reference is obtained by a single sharing wire.

Most digital current-sharing methods [4-6] are master-based approach requiring dedicated connections between master controller and slaves. A digital modular and masterless architecture is proposed in [7,8]. This method is based on identical digitally controlled DC-DC converter modules that communicate over a Control Area Network (CAN) interface. A chain control algorithm is designed with reduced storage and communication requirement to perform a moving window average for masterless current-sharing.

Proposed Masterless and Modular Current-Sharing (MMCS) method is presented in Fig.1 and detailed in section II. Analogical or digital implementation for this technique is possible. Mathematical demonstration is achieved in section II in order to verify if such a local correction computation leads to the same global average current convergence as classical current-sharing technique.

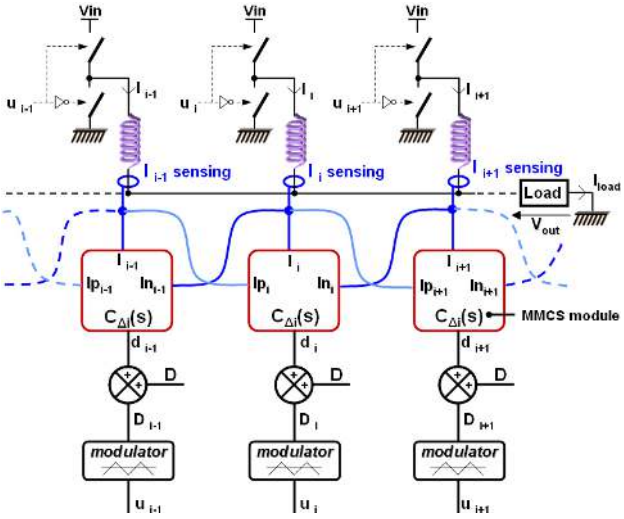

Fig. 1. MMCS approach principle, communicating modules placed in a daisy chain configuration

DC/DC parallel converters with coupled inductors can achieve faster transient response, a higher power density and a higher efficiency due to lower component stress [9, 12-16]. Nevertheless, they need a higher current-sensing accuracy for current-sharing purpose. Indeed, a slight current imbalance can lead to magnetic core saturation of coupled inductors [16]. Many current-sensing techniques are proposed in the literature [10-11], but are not suitable with coupled inductors required accuracy. A solution consists in compensating each phase resistive path

mismatch by adjusting a gain for each current sensing [9]. This technique requires manufacturing tuning and is sensitive to resistive path variation while system is running. Then, an accurate differential current sensing method seems better and is proposed in section III. Implementation of these sensors takes advantage of MMCS architecture which requires only slight modifications.

MMCS analog filters design and stability study are presented in section IV.

Finally, implementation of a six phase DC/DC buck converter demonstrator with coupled inductors is presented in section V. Persuasive experimental results are performed thanks to an extremely precise differential current-sensing technique applied to new Masterless and Modular Current-Sharing (MMCS) technique.

II. MMCS : General Case

MMCS architecture is presented in Fig. 1. Each module computes with an analog or digital controller local average current error by comparing phase current with its adjacent phase currents. Then a local duty-cycle correction is generated in order to place the local current between its adjacent currents. By placing identical MMCS modules in a daisy chain configuration, all currents will converge to the currents' global average value. One can note that MMCS method is suitable with classical current-sensing (DCR current-sensing, R_{DSon} current-sensing, etc.) [9-11]. Masterless approach avoids the use of centralize circuits which computes a global reference like in classical current sharing. This modular approach makes possible the scalability of this technique to a large number of phases and consists in placing in a daisy chain as many MMCS modules as number of phases.

A. MMCS module description

Fig. 2 describes in detail MMCS module. This module computes the difference between its dedicated phase current value and the average value of its two adjacent currents. εi error is obtained and sent to $C_{\Delta i}(s)$ corrector filter which will compute proper duty cycle correction to cancel this error.

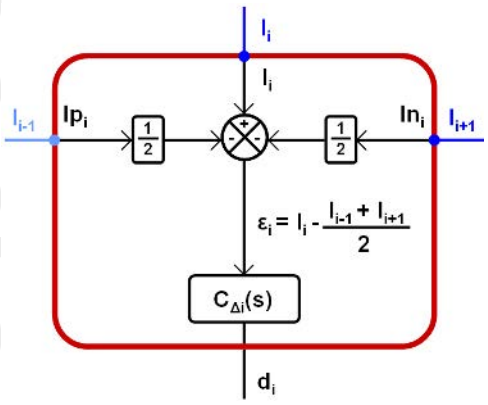

Fig. 2. MMCS module description

Proper characteristics for $C_{\Delta i}(s)$ corrector are given in Section IV. Electronic design of this module is simple and can be achieved either with analog or numeric circuit.

It is necessary to verify if such a masterless approach differs from classical current-sharing in terms of average phase current.

B. Comparison with classical current sharing

The purpose of this subsection is to demonstrate that both methods do not modify, during and after convergence, the average phase current I_{avg}. Indeed, a current-sharing method should not modify average current but should balance phase currents by adjusting local duty cycle correction d_i, on the contrary voltage loop modifies global average current by adjusting general duty cycle D.

In order to simplify calculus, we consider that phases are not coupled and $C_{\Delta i}(s)$ is a basic integrator with a time constant τ. Then local phase current I_i expression is:

$$I_i(t) = (D + d_i(t)) \cdot I_{\max} \tag{1}$$

where:

$$I_{\max} = \frac{V_{in}}{V_{out}/I_{load}} \cdot \frac{1}{k} \tag{2}$$

with D: average value of all phase duty-cycle, $d_i(t)$: local duty cycle correction, k: number of phases, V_{in}: input voltage, V_{out}: output voltage and I_{load}: output load current. $d_i(t)$ expression is:

$$d_i(t) = \frac{1}{\tau} \cdot \int_0^t \varepsilon_i(t) \cdot dt + d_i(0) \tag{3}$$

where:

$$d_i(0) = 0 \tag{4}$$

Then global average phase current can be expressed as:

$$I_{avg}(t) = \frac{1}{k}\sum_{i=1}^{k} I_i(t) = I_{\max} \cdot \left(D + \frac{1}{k}\sum_{i=1}^{k} d_i(t) \right) \tag{5}$$

with:

$$\frac{1}{k}\sum_{i=1}^{k} d_i(t) = \frac{1}{k \cdot \tau}\int_0^t \sum_{i=1}^{k} \varepsilon_i(t) \cdot dt \tag{6}$$

hence:

$$I_{avg}(t) = \frac{1}{k}\sum_{i=1}^{k} I_i = I_{\max} \cdot \left(D + \frac{1}{k \cdot \tau}\int_0^t \sum_{i=1}^{k} \varepsilon_i(t) \cdot dt \right) \tag{7}$$

ε_i formula depends on the current sharing technique used, and so does I_{avg} expression, then it is possible to compare both expressions and verify that the average current keeps constant and remains unchanged whatever time t.

1) Classical current-sharing technique

Classical current-sharing method consists in comparing each phase current to the global average current. The error is given by the basic formula:

$$\varepsilon_i(t) = I_i(t) - I_{avg}(t) \tag{8}$$

Fig. 3. presents this classical method for a six-phase DC/DC converter.

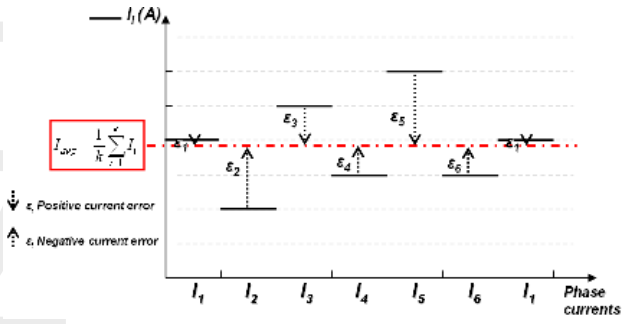

Fig. 3. Classical current-sharing method illustration

$$\sum_{i=1}^{k}\varepsilon_i(t)=\sum_{i=1}^{k}I_i(t)-k\cdot I_{avg}(t)=0\Rightarrow\frac{1}{k}\sum_{i=1}^{k}d_i(t)=0\ \forall t \quad (9)$$

$$I_{avg}(t)=D\cdot I_{\max}\ \ \forall t \quad (10)$$

As we could expect, whatever the time, the classical current-sharing method does not modify global average current. The same calculus is computed with the MMCS method.

2) MMCS technique

Masterless and modular current-sharing method consists in comparing each phase current to the average of its adjacent phase current. The error is given by the basic formula:

$$\varepsilon_i(t)=I_i(t)-\frac{I_{i-1}(t)+I_{i+1}(t)}{2} \quad (11)$$

Fig. 4. presents this modular method.

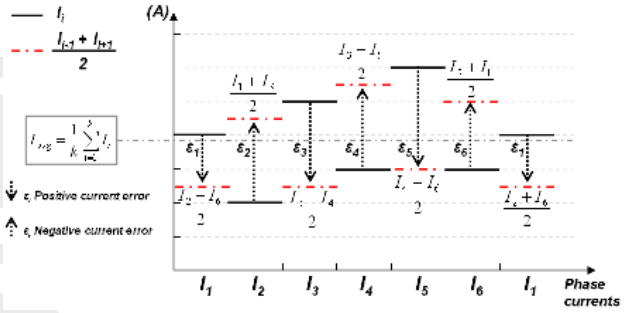

Fig. 4. MMCS method illustration

$$\sum_{i=1}^{k}\varepsilon_i(t)=\frac{1}{2}\cdot\sum_{i=1}^{k}\left(I_{i-1}(t)+I_{i+1}(t)\right)-\sum_{i=1}^{k}I_i(t)\ \forall t \quad (12)$$

$$\sum_{i=1}^{k}\left(I_{i-1}(t)+I_{i+1}(t)\right)=2\cdot\sum_{i=1}^{k}I_i(t)\Rightarrow\frac{1}{k}\sum_{i=1}^{k}\varepsilon_i(t)=0\Rightarrow\frac{1}{k}\sum_{i=1}^{k}d_i(t)=0\ \forall t \quad (13)$$

$$I_{avg}(t)=D\cdot I_{\max}\ \ \forall t \quad (14)$$

Whatever the time *t*, the MMCS approach does not modify the average global current. We can deduce from this demonstration that, even if the error to cancel is different between both methods, global average current is not modified. Stability study is presented in section IV.

III. MMCS for DC/DC Parallel Converter With Coupled Inductors

Parallel converter architecture using intercell transformers is one of the most adapted architecture for low-voltage, high-current and fast transient power conversion applications. Interleaved multi-phase converter with intercell transformers main interest is the current ripple reduction in each converter arm which is not the case with non-coupled inductor architectures. As a consequence, current constraints on switches and inductors are less severe and lower Joule losses are obtained leading to a higher efficiency.

A. Specific care related to Parallel Converters using intercell transformers

As described in [16] currents imbalance can lead to intercell magnetic core flux drifts. This issue is shown in Fig. 5 with a six phases converter with intercell transformers placed in a cyclic-cascade configuration. This is a bar graph cyclic representation of the system. Unbalanced currents (in red) lead to average flux (in blue); average value of phase currents is a red circle (dotted line). One can note that if currents were equal flux would be cancelled. Then an accurate current-sharing loop is necessary for those architectures in order to avoid magnetic core saturations. Eq. 15 illustrates this relation between average flux and currents imbalance:

$$\phi_{12}=\frac{N}{\Re}\left(I_1-I_2\right) \quad (15)$$

with I_1 and I_2 : currents flowing through transformer windings, N : winding turn number, ϕ_{12}: induced magnetic flux and $\Re$: magnetic core reluctance.

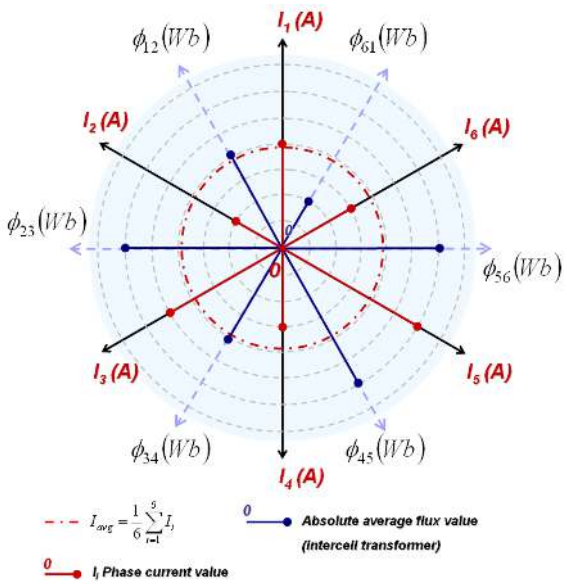

Fig. 5. Currents imbalance in a 6-phases daisy chain configuration

Classical current-sensing techniques such as DCR-sensing or R_{DSon}-sensing provide absolute phase current value whose accuracy is different among the phases. For

instance, two sensors with different accuracies can measure a current difference between two phases even if phases are balanced. Those current-sensing techniques are not acceptable for converter which requires an extremely precise balancing between phases current in order to avoid magnetic core saturation.

B. New differential current sensing technique

Instead of measuring two absolute phase current values with two different sensors and computing the difference, it can be interesting to directly measure the difference between two phases current with one sensor. Then measurement accuracy is related to the relative difference between both currents and not to the absolute current values. As presented in (15) differential current is proportional to the magnetizing current and average flux in transformer magnetic core. As a consequence, this measure allows us to control directly flux value.

Fluxgate sensors are good candidates for magnetizing current or flux measurement. Differential current measurement with Fluxgate and its schematic picturing is presented in Fig.6.

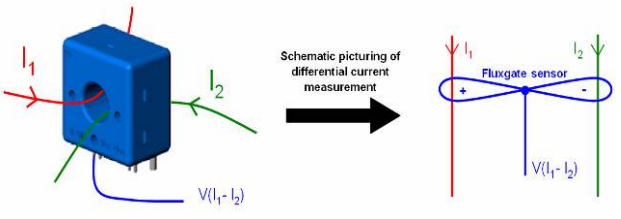

Fig. 6. Differential current sensing representation

As presented in Table 1 of section V, sensor characteristic meets a need of accuracy and presents sufficient bandwidth for many applications of current-sharing control.

Moreover, Fluxgate sensors are non-invasive sensors: impedance is not reflected to the primary and secondary phase conductors because magnetic core operates in saturate region.

C. MMCS architecture modification for differential current measurement

MMCS architecture presented in section II is not suitable with differential current measurement performed with Fluxgate sensors. Fig.7 and Fig.8 respectively presents the MMCS necessary architecture modification for differential current measurement and the detail of the MMCS module for parallel converters with coupled inductors.

This modified architecture still consists in placing identical MMCS modules in a daisy chain configuration. MMCS modules have to be adapted for differential current measurement. A simple subtraction operation is necessary to turn two differential current measurements into an error related to the difference between phase current and the average of its adjacent currents. Fig.8 presents this simple operation.

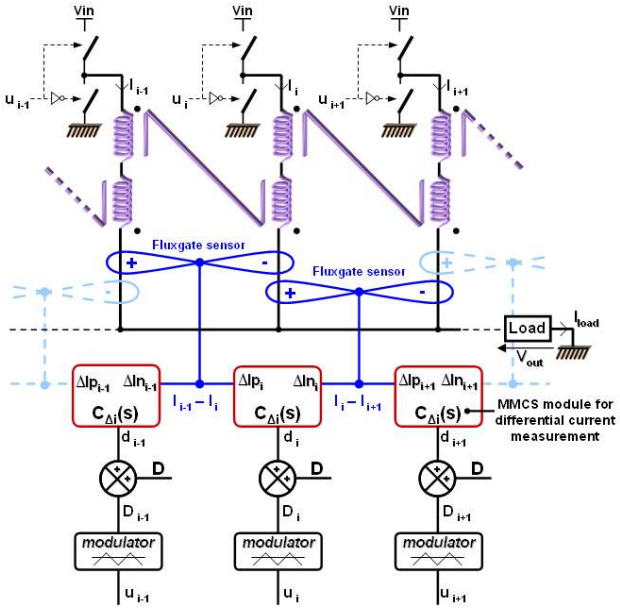

Fig. 7. MMCS principle for differential current measurement

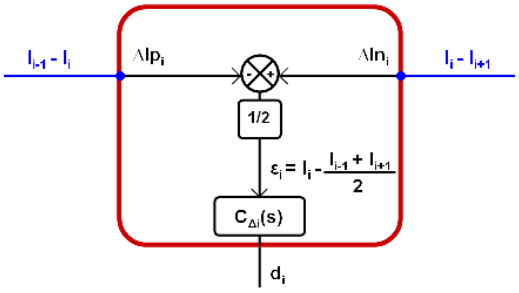

Fig. 8. MMCS Module for differential current measurement

ε_i formula for differential current measurement is identical to the MMCS general case, then current-sharing filter $C_{\Delta i}(s)$ design is not modified by this architecture modification.

One can note that differential current sensing and the appropriate MMCS architecture can be used for parallel converters without coupled inductors, and can either be implemented with analog or numeric circuits. In the presented case, inductors are coupled in a cascade cyclic configuration: first phase is magnetically coupled with second and last phases. As described in [13], this coupling configuration is the most interesting for DC/DC parallel converters.

IV. MMCS Filter Design

MMCS modules must provide the adequate differential duty cycle d_i so that the difference between the phases current I_i and the average of its adjacent currents is cancelled. Then $C_{\Delta i}(s)$ static and dynamic characteristics must be determined in order to ensure good system stability and low steady state error. This stability study is related to our application: a six-phase DC/DC buck converter with coupled inductors in a cascade cyclic configuration. Then transfer functions take into account magnetic coupling between inductors.

A. MMCS loop architecture

Loops' architecture is a very important point for current sharing control. Indeed, when using integral correctors in current-sharing loop, op-amp offset voltage causes permanent error which is integrated by the corrector. As a consequence d_i duty cycles drift and lead to phase current permanent drift. To avoid this phenomenon, specific architecture is proposed in [9] and presented in Fig.9. It is suitable with classical and differential current-sensing. It consists in compensating op-amp offset voltage with the voltage loop which is directly connected to the positive op-amp pin.

As it is presented in Fig.9, both common mode and differential mode excitations have to be separated in order to distinguish voltage loop and current-sharing loop control. Even if common and differential excitations may occur at the same time while system is running, explications isolate each phenomenon for better understanding of the architecture.

In steady state, V_e is equal to the average value of the op-amps voltage offsets and avoids currents drifts. V_{Di} from all MMCS modules allow canceling currents errors because of integral correctors. V_{out} is equal to the reference V_{ref} assuming that voltage loop correction is an integrator.

If a perfect differential mode excitation occurs, then two phase currents are unbalanced but do not modify load current. V_{out} is not modified, and V_e still compensates op-amp offset voltage. Current error appears and is cancelled by the MMCS module integral corrector.

If V_{ref} is modified and assuming that currents are perfectly balanced, a common mode excitation is generated. Then V_e stops compensating op-amp offset voltage and changes quickly the duty cycle value. As a consequence, output voltage V_{out} reaches V_{ref} value, *Ci2* capacitance is charged to a proper voltage value and V_e gets back to offset voltage compensation.

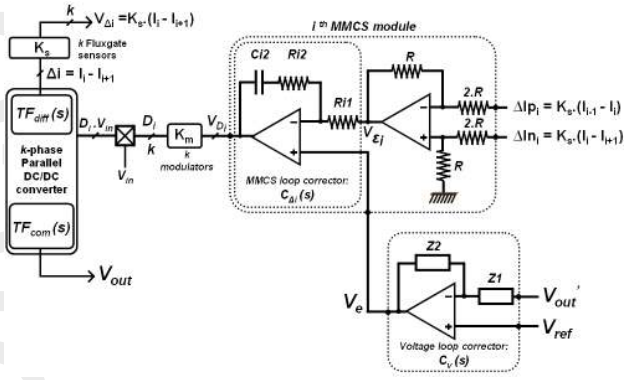

Fig. 9. *MMCS loop architecture*

B. MMCS loop stability

MMCS filter determination is impossible without system differential current transfer function $TF_{diff}(s)$ study for a converter with coupled inductors. This analysis is presented in [16] for a two-phase buck converter with coupled inductors. This transfer function is presented in (16) and adapted for a *k*-phase converter with coupled inductors in a cascade cyclic configuration.

$$TF_{diff}(s) = \frac{\Delta i(s)}{D_i(s)} = \frac{2 \cdot \frac{V_{in}}{R_{on}}}{1 + \tau_{diff} \cdot s} \quad (16)$$

and:

$$\tau_{diff} = 2 \cdot \frac{2 \cdot L_m + L_l}{R_{on}} \approx \frac{4 \cdot L_m}{R_{on}} \quad (17)$$

with L_m: transformer magnetizing inductance, L_l: transformer leakage inductance, Ron: arm equivalent resistance.

$TF_{diff}(s)$ is a first order transfer function with high gain and very low time constant τ_{diff}. Then, as R_{on} is taken as low as possible, τ_{diff} can reach very high values.

Then the open loop differential transfer function $H_{diff}(s)$ is deduced and presented in (18). It takes into account gains introduced by *PWM* modulator K_m (V^{-1}) and Fluxgate sensor K_s (V/A).

$$H_{diff}(s) = TF_{diff}(s) \cdot K_m \cdot K_s . C_{\Delta i}(s) \quad (18)$$

The proposed MMCS corrector is presented in (19). It is an integral proportional corrector. Integral correction cancels steady state error and is tuned on τ_{diff} to ensure unconditional stability. Proportional gain allows us to adjust MMCS closed-loop time constant response.

$$C_{\Delta i}(s) = \frac{V_{Di}(s)}{V\varepsilon i(s)} = -\left(\frac{Ri2}{Ri1}\right) \cdot \left(1 + \frac{1}{Ri2 \cdot Ci2 \cdot s}\right) \quad (19)$$

with *Ri1*, *Ri2*, *Ci2* : component values of the analog filter (described in Fig.9).

Bode representation of $H_{diff}(s)$ transfer function is presented in Fig.10.

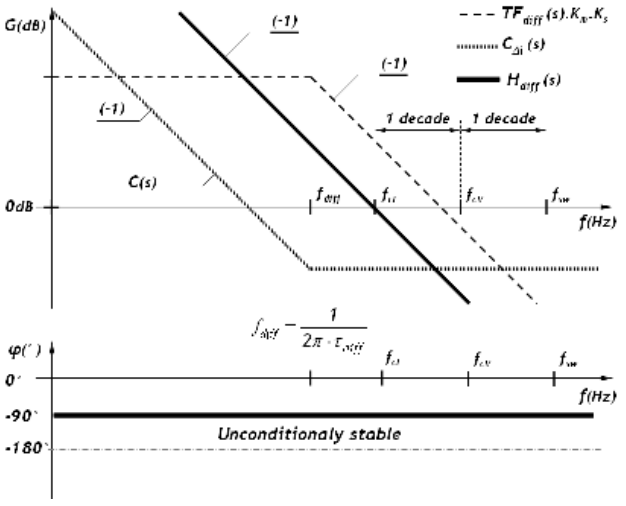

Fig. 10. $H_{diff}(s)$ Bode representation

The closed-loop system is unconditionally stable if $H_{diff}(s)$ cut-off frequency noted f_{cI} is adjusted at least one decade lower than voltage loop cut-off frequency f_{cV} which is adjusted one decade lower than switching frequency f_{sw}.

One can note that a simple proportional corrector without integral correction can be used contingents on application. Indeed, static gain is adjusted so that cut-off frequency is two decades lower than switching frequency. If $H_{diff}(s)$ static gain is high enough, then steady state error between phase's currents may be low enough so that magnetic core will not saturate.

Voltage loop stability is not the purpose of this paper: few design recommendation are given in this article. Open loop voltage transfer function $H_{com}(s)$ is described in (21). It can be noted that MMCS corrector influences voltage loop. Indeed integral correction is already provided by MMCS corrector and ensures null steady state error for voltage regulation. The system voltage transfer function expression is as follow:

$$TF_{com}(s) = \frac{1}{1 + \frac{Ll/k}{R_{load}} \cdot s + Ll/k \cdot C \cdot s^2} \quad (20)$$

then:

$$H_{com}(s) = C_v(s) \cdot (1 - C_{\Delta i}(s)) \cdot K_m \cdot TF_{com}(s) \quad (21)$$

where:

$$C_v(s) = -\frac{Z2(s)}{Z1(s)} \quad (22)$$

With R_{load}: load resistive part, C: output filter capacitor, L_l: leakage inductance of transformers.

Voltage loop corrector $C_v(s)$ must guarantee good stability and its cut off frequency f_{cV} must be at least one decade lower than switching frequency.

V. Experimental Results

A six phase DC/DC converter with coupled inductors in a cascade cyclic configuration is achieved to confirm the MMCS approach with differential current sensing. Complete system characteristics are presented in Table II.

LEM CT – 0,4P sensors are used to perform differential current sensing. Its characteristics are presented in Table I.

TABLE I.
FLUXGATE LEM CT 0,4P CHARACTERISTICS

Ipn	Primary nominal current rms	400	mA
Ipm	Primary current measurement range	± 800	mA
Vm	Output voltage (analog) @ Ipn	± 5	V
X	Accuracy (excluding offset) @ Ipn	< ± 1	% of Ipn
Voe	Electrical offset voltage	< ± 100	mV
BW	Frequency bandwidth (-3dB)	DC 40-18000	Hz

One can note that offset current measurement error which depends on electrical offset voltage *Voe* is inferior to 8 mA which is very few compared to 200 mA magnetizing current magnitude.

MMCS architecture presented in section IV is used to perform MMCS control. Its characteristics are for current sharing loop: f_{cI} = 100Hz then: *Ri1* = 270kΩ, *Ri2* = 27kΩ, *Ci2* = 1µF; and for voltage loop f_{cV} = 1,3kHz then: *Z1* = *Rv1* = 1kΩ, *Z2* = *Rv2*//*Cv2* = 10kΩ//1µF.

Fig. 11 shows the six-phase power converter test circuit and Fig. 12 shows the MMCS control card.

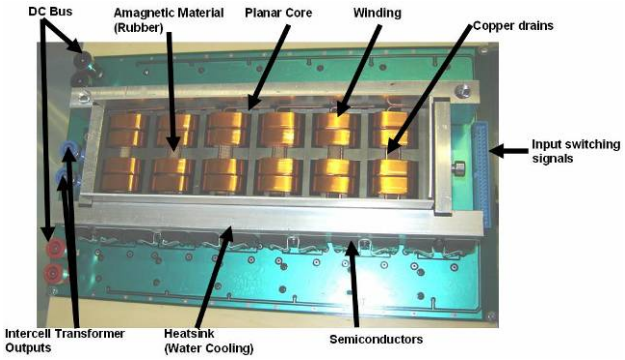

Fig. 11. *Power converter*

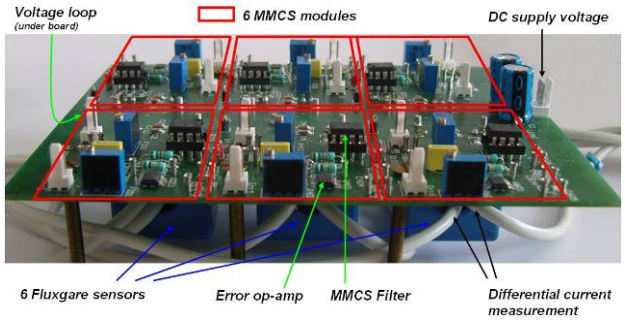

Fig. 12. *MMCS Control card*

MMCS control card is much smaller than power converter and can be easily inserted between the load and the intercell transformer.

TABLE II.
MMCS AND POWER CONVERTER CHARACTERISTICS

V_{in}	Input Voltage range	0-300	V
V_{out}	Output voltage range	0-300	V
I_{load}	Output load current range	0-100	A
L_m	Magnetizing inductance	636	µH
L_l	Leakage inductance	6	µH
R_{on}	Arm equivalent resistance	≈10	mΩ
τ_{diff}	Open-loop time constant for a differential current excitation	256	ms
F_{sw}	Switching frequency	40	kHz
F_{cV}	Voltage loop cut off frequency	1,3	kHz
F_{cI}	Differential loop cut off frequency	100	Hz
τ_{cI}	Closed-loop time constant for a differential current excitation	1,6	ms
τ_{cV}	Closed-loop voltage time constant	120	µs

Tests in steady-state are achieved in open-loop and closed-loop configuration. The fifth phase of the power converter is naturally unbalanced. Its resistive path differs from the other phases and may lead to magnetic core saturation. Fig. 12 and Fig.13 shows respectively open-loop and closed-loop steady-state tests. Output voltage and currents of the third, fourth and fifth phases are observed in both open-loop and closed-loop tests with: V_{out} = 10V, I_{load} = 40A and D_i = 25%.

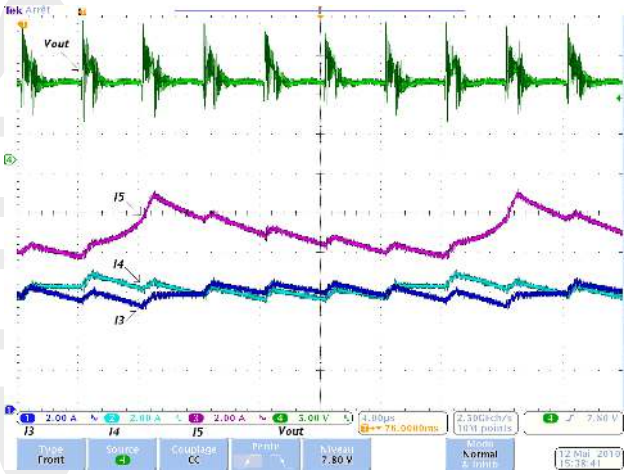

Fig. 13. *Open-loop static waveforms*

Open-loop test shows that the current of the fifth phase has a 3 amps steady state error with other phase currents. The fifth phase current is a typical saturated phase current waveform. Then restive path mismatch has leaded to a too large phase current difference and finally to magnetic core saturation.

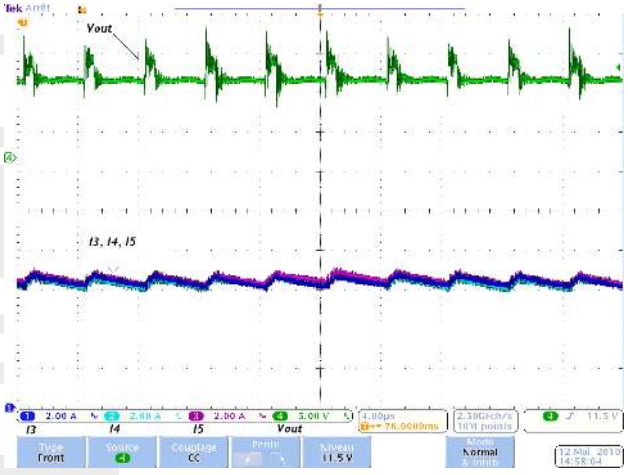

Fig. 14. *Closed-loop static waveforms*

Closed-loop test in steady-state is achieved at the same operation point as open-loop test. Average phase currents are perfectly balanced: no typical saturated phase current waveform is observed. Operation point can reach nominal load current thanks to MMCS regulation (I_{load} = 100A).

Dynamic test is achieved in closed-loop configuration. It consists in adding a step voltage perturbation to *VDi* signal in order to unbalance phase duty-cycles which leads to average phase current unbalance. Perfect differential perturbation is possible in simulation but impossible for experimentation with analog correctors. Then time constant for phase current gets back to equilibrium is not the closed-loop time constant for differential current excitation. Observed time constant depends on *Ri2.Ci2* value. One can observe that even for a strong perturbation on phase duty cycle, system reacts and compensates this default by adjusting slightly the duty cycle.

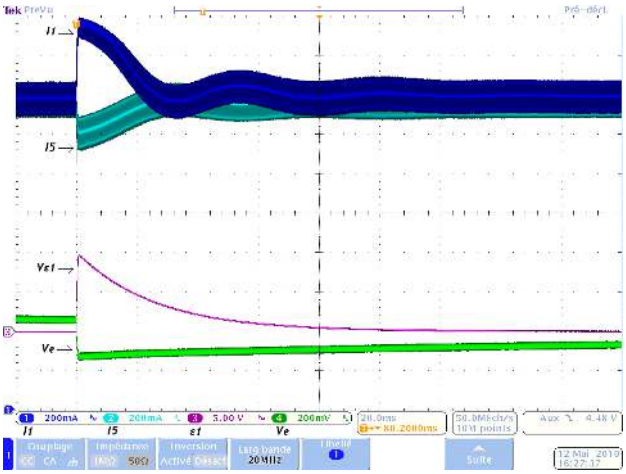

Fig. 13. *Closed-loop waveforms with dynamic perturbation*

VI. Conclusion

This article has shown a new Masterless approach to regulate phase currents of an interleaved converter. This modular architecture named “Masterless Modular Current-Sharing” (MMCS) has the following advantages:

1. Central circuit to compute global average of phase currents is not required,
2. It is a modular approach made of identical MMCS modules placed in daisy chain,
3. Scalability to a large and arbitrary number of phases.

A specific Current-sensing technique using fluxgate-sensor is proposed and has the following advantages:

4. It is suitable with parallel converter with coupled inductors topology,
5. Sensing accuracy is extremely high because it is related to the currents’ difference and not to the absolute currents’ values,
6. It is not sensitive to inductance DCR or on-state resistance variations caused by environmental conditions such as operating temperature,
7. It is not an invasive current sensing technique,
8. No manufacturing tuning is required for this sensing technique.

Power converter and its associated control boards have been achieved. Experimental results prove the validity of the proposed current-sharing method. Interest of using differential current sensor applied to this MMCS approach is demonstrated and leads to accurate current balance and intercell transformer non-saturation guaranty.

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