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Timothé Rossignol, Frédéric Richardeau, Jean-Marc Blaquière, Damien Risaletto, F. Senghor, et al.. Switching Optimization of WBG Power Devices on Inverter Leg. PCIM Europe 2013; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, May 2013, Nürnberg, Germany. hal-02964301

HAL Id: hal-02964301

<https://hal.science/hal-02964301v1>

Submitted on 23 Jul 2021

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Switching optimization of WBG power devices on inverter leg

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Abstract

In this paper the authors are interested by the switching optimisation of a SiC Power MOSFET in an inverter leg. The authors explain their efforts to build a test-bench that allows the extremely fast switching measurement of this WBG (Wide Band-Gap) component. Then trade-off curves between the dv/dt versus the switching energy are presented. The parameters are the external gate resistor and an additional gate-drain capacitor. Finally, basic dv/dt models are proposed and compared with the experimental results.

1. Context:

In power electronics the trade-off between voltage rating, current density and switching frequency leads to continually improve the silicon capabilities. However it seems that silicon power devices reach a limit especially for highly integrated converters used in embedded systems. All this encourages research in new materials and new substrates, including “wide bandgap” such as silicon carbide (SiC) in the field of middle voltage [1] and more recently gallium nitride (GaN) in the field of low voltage [2][3].

2. Problematic and Topic:

Both materials are now used to design unipolar conduction power devices (SBD, JFET and SiC MOSFET in the range of 1200V/1700V) in vertical topology and more recently HEMT GaN (in the range of 600V) in lateral topology. Those are known for extremely fast and low losses switches, with switching time between 5 and 25ns (i.e. 5 to 10 times lower than fastest IGBT of the same range of voltage). As a result very high dv/dt commutations (typically 20kV/ μ s to 50kV/ μ s, and more ...) are clearly sources of very hard perturbations and self-perturbations especially in inverter leg topology (high side/ low side coupling) and common mode current loops that induce EMI for the converter and its near environment [4]. Figs. 1 a) and b) exhibit the typical dv/dt effects previously observed by the authors on lab. set-up:

a) spike voltage across gate-source with a possible transient cross-conduction of an inverter leg (caused by the C_{gd} capacitor coupling of the power devices) that can lead to great additional switching losses,

b) pulsed common-mode current along the ground connection of a synchronous drive fed by a PWM inverter (caused by the parasitic capacitors of the windings and the magnetic elements of the actuator) and possible EMI disturbances towards the global system. For example, as shown in Fig. 1 b), a 0.8A peak current flows to the ground cable caused by a 20kV/ μ s turn-on.

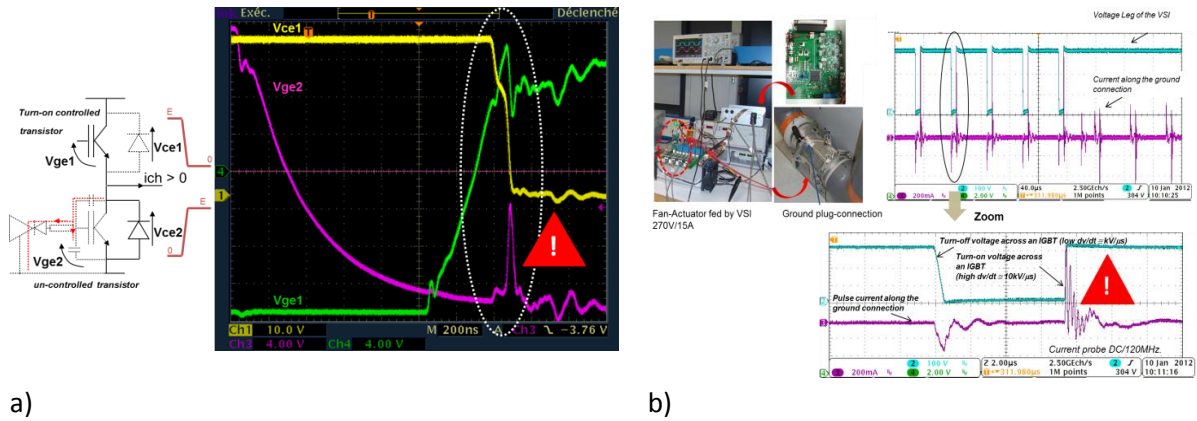


Fig. 1. Typical dv/dt effects: a) spike voltage across gate-source with a possible transient cross-conduction of an inverter leg, b) pulsed common-mode current along the ground connection of a synchronous drive fed by a PWM inverter

3. Objectives:

A simple and direct approach to limit the dv/dt is to slow down the commutation, either by optimizing the gate resistance, or more selectively by adding a feedback capacitor between the gate and the drain acting, in principle, finely only on the dv/dt value as illustrated in Figs. 2 a) and b). The drawback to this approach is the increase of the switching time, losses and a possible reduction of the gate voltage immunity [5]. Nevertheless, using a direct feedback capacitor should give a best trade-off between dv/dt limitation and over switching losses. Contrary to Fig. 2 b) authors will show that a slight $di/dt - dv/dt$ coupling exists leading to a less efficient solution.

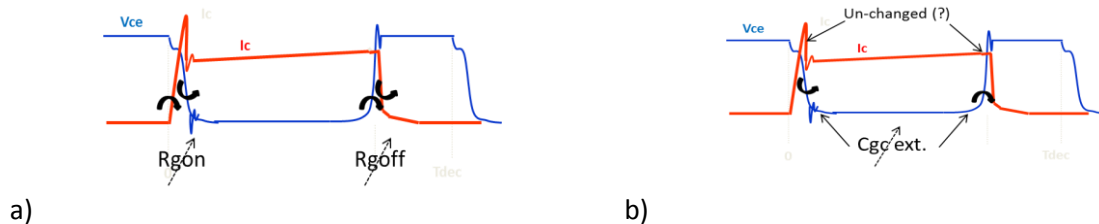


Fig. 2. a) $R_{g\text{on Ext.}}$ and $R_{g\text{off Ext.}}$ effect on voltage and current switching time (example dedicated to IGBT devices), b) $C_{g\text{c}}$ or $C_{g\text{d Ext.}}$ effect, in principle, only on voltage switching time.

In this article the authors present a synthesis result of many characterization campaigns as trade-off curves between dv/dt and switching energy based on a CREE SiC Power MOSFET, the CMF20120D. The external gate resistor (R_{gateEXT}) and the feedback capacitor (C_{gdEXT}) are the main variable parameters for a given switching current range considering a constant ambient temperature (25°C) imposed to the case. From the presented results, designers will have a preferential technique and a settable range for the driver to get a good trade-off between all the issues of the application. In addition, a simple linearized and 1st order dv/dt models are proposed by the authors and compared to the experimental results according current dependence and afterwards gate resistor dependence. Such models are able to predict, in a first approach, the spectral envelop produced by the switching voltage and then to contribute to the design of the common-mode EMI filters.

4. Methodology:

The test circuit is an inverter leg (Fig. 3 a) where the DUT is the low-side device. The load is a simple air inductor used in the well-known double short pulse method that leads to insignificant self-heating of the die (Fig. 3 b.). Very important care has been taken of the

design of the double layer PCB, of the filtering and decoupling of the switching cell and finally of using a non-inductive coaxial shunt as it is shown on Fig. 4. A track inductance estimation based on the residual linear value of 10nH/cm (outside the busbar plan) leads to an overall value of the stray inductance of 50nH. This value takes into account of the package pins of the components.

Special attention was also paid to instrumentation (oscilloscope bandwidth, high voltage passive probes and the compensation of all the imperfections that can distort the switching energy measures) as specified in Tab. 1. Fig. 5 shows an example of acceptable compensation (deskew mode) of the I_d and V_{ds} measures on the DUT. This is achieved by observation of the waveform alignment. At turn-on the switching current is aligned on the inductive voltage drop. At turn-off, it is checked that current and voltage oscillations are in quadrature (viewed from its terminals the transistor is equivalent to a C_{oss} capacitance).

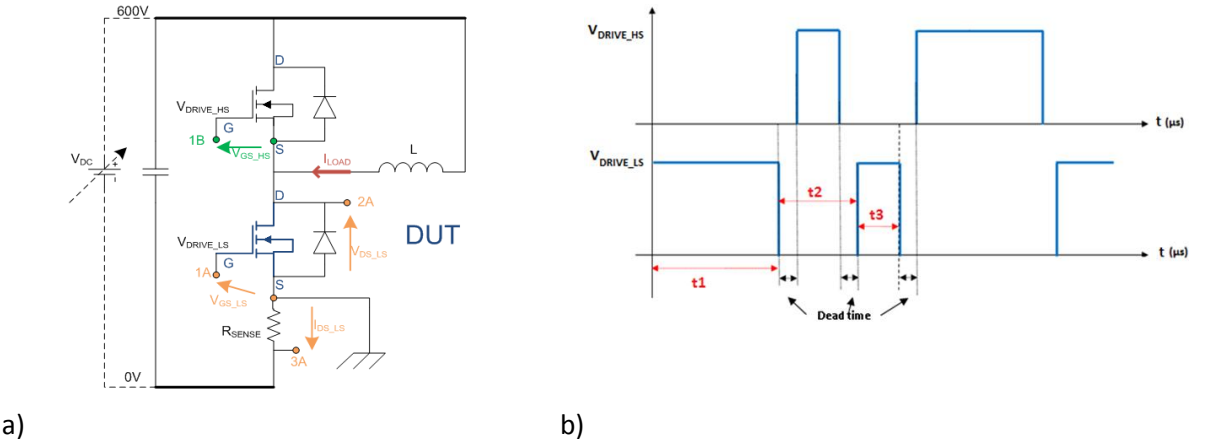


Fig. 3. a) test circuit in inverter leg topology, b) control signals of the "double-short pulse" method (t_1 is settable by step of $4\mu s$ from $2.6\mu s$ (minimum value) to $58.6\mu s$ (maximum value)). Note : in orange color are represented the two probes and the sensor connected to the oscilloscope A that is referenced to the earth. They allow to measure on the low-side transistor: 1A) the gate-source voltage, 2A) the drain-source voltage, 3A) the drain current .In green is represented a probe connected to the oscilloscope B running on battery and thus isolated from earth.

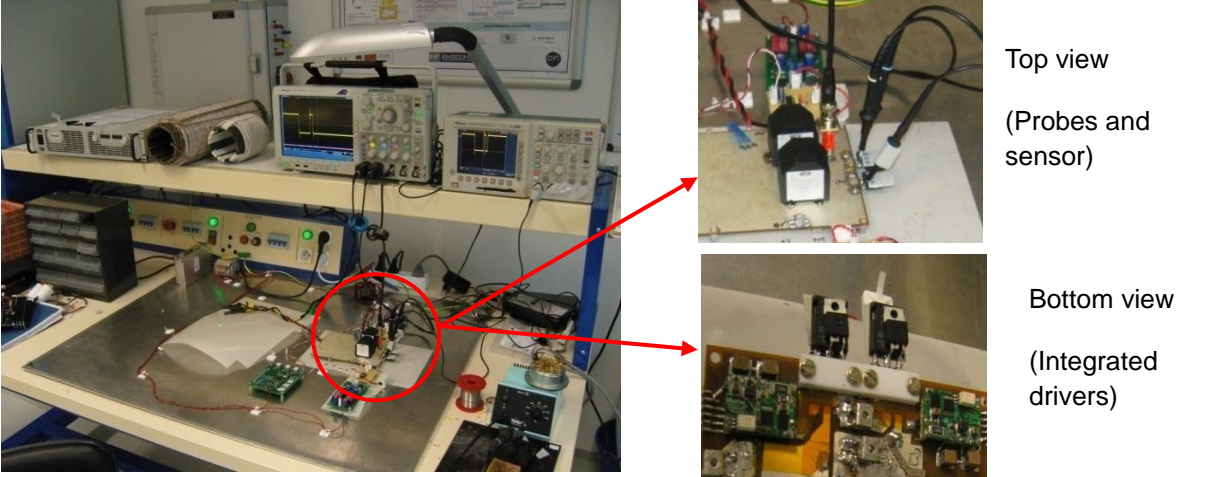


Fig. 4. Test bench for WBG devices switching characterization (overview and zooms).

Oscilloscopes, Probes and Current sensor	Features	Adaptation – Compensation/ Notes
Tek DPO414B	1GHz/5.5Gsamples/s	V_{ds} , I_d , V_{gs} DUT measures
Tek TDS3014	100MHz	V_{gs} high side measure
V_{ds} DUT probe : Tek x50 TPP0850	1kV – 1.8pF – 800MHz	Automatique capacitive compensation, Deskew : $T_p = 6.1ns$
V_{gs} DUT probe : Tek x10 TPP1000 SYNCHRO	300V – 3.9pF - 1GHz	Automatique capacitive compensation, Deskew : $T_p = 5.3ns$
V_{gs} High Side: Tek x10	300V – 200MHz	Manual compensation
I_d DUT probe : shunt T&M Research SDN 41410 using coaxial RG-58	shunt : 100m Ω - 2GHz Cable : $\tau = l\sqrt{L_l C_l}$ $L_l \cong 210nH/m$, $C_l \cong 80pF/m \rightarrow 4.1ns/m$	50 Ω adaptation, Deskew : T_p manual = 3.2ns

Tab. 1 Features of oscilloscopes, voltage probes and current sensor used for the SiC Mosfet characterisations

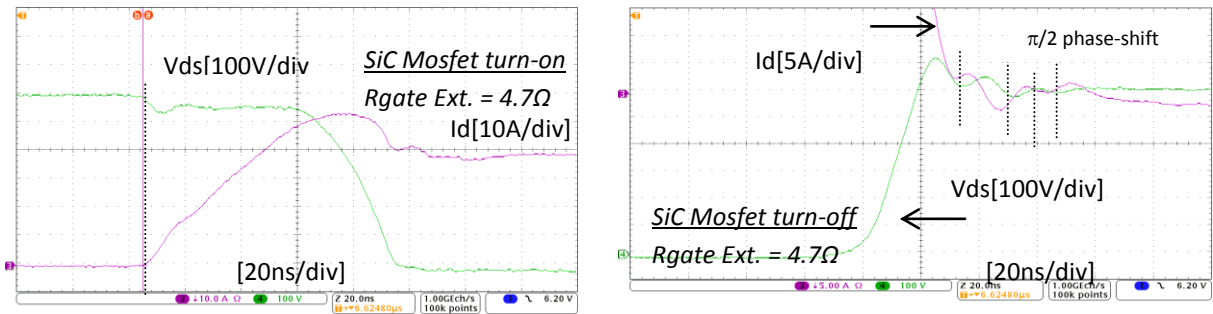


Fig. 5. Verification of the delay time compensation and alignment of curves at the output of passive probes, for turn-on and turn-off (SiC Mosfet operating point: 600V/40A @ $R_{gate\ Ext.} = 4.7\Omega$ - $T_{case}=25^\circ C$). Note : $R_{gate\ Int.} = 5\Omega$. $R_{gate\ total} = R_{gate\ Ext.} + R_{gate\ Int.}$.

5. Results

5.1. $R_{gateEXT}$ variation

Firstly in Fig. 6, we observe that as expected, an increase of $R_{gate\ EXT}$ leads to a decrease of the dv/dt and the di/dt values. Secondly, we focus on the inverter behaviour: at turn-on, for a low switched current the dv/dt is maximum and it decreases with the increase of the switched current. At turn-on, it is clear that the controlled channel current of the DUT is greatly more influent than the switched current. We notice the opposite variations for the turn-off because the switched current is more influent than the channel current: at low load current the dv/dt is minimum and it increases with the increase of the load current.

There is one particular case where the external gate resistor has no impact on dv/dt and di/dt : the turn-off at low current and so at low dv/dt . Indeed it is a case that we called “Inactive Miller Effect”, the switched current is so low that $V_{gs} < V_{gsth}$ during the switching of V_{ds} . We notice a plateau at $I_{load}/2$, it is a quasi-zero current switching at very low losses where the load current is split down the middle along the C_{oss} capacitors of the high side and low side devices.

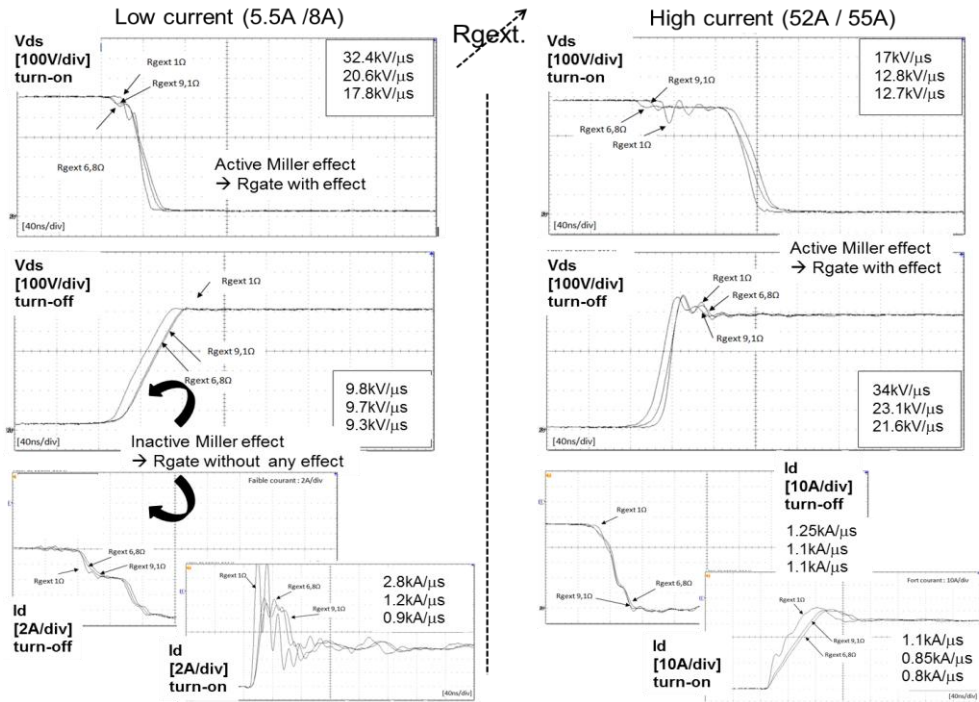


Fig. 6. Analysis and measurements of the $R_{gate\ Ext.}$ effect on dv/dt and di/dt at low current (5.5A/8A – 600V) and high current (52A/55A – 600V) including two SiC Mosfet in the leg switching-cell. Note: $R_{gate\ Int} = 5\Omega$. $R_{gate\ total} = R_{gate\ Ext.} + R_{gate\ Int.}$

5.2. C_{gdEXT} variation

In the second time of the measurement campaign we focus on the impact of C_{gdEXT} at fixed $R_{gateEXT}$. A non-inductive high-voltage ceramic capacitor is directly welded between the drain and gate pins of the package [6]. In Fig.7 the two extreme cases are compared (where the dv/dt are maximum), with an external capacitor of 100pF or without this external capacitor. In one hand, one notices that, in the both cases the impact of C_{gdEXT} is noticeable and the dv/dt is clearly decreased. But in the other hand, one can notice the presence of a slight coupling between the dv/dt and di/dt .

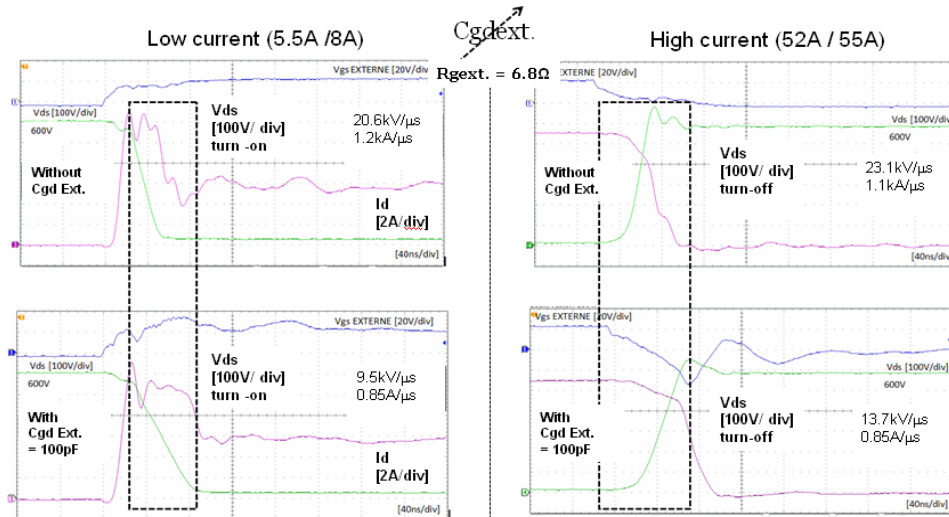


Fig. 7. Analysis and measurements of the $C_{gd\ Ext.}$ effect on dv/dt and di/dt at low current turn-on (5.5A/8A – 600V) and high current turn-off (52A/55A – 600V) including two SiC MOSFET in the switching-cell. Note: $R_{gate\ Int} = 5\Omega$. $R_{gate\ total} = R_{gate\ Ext.} + R_{gate\ Int.}$

5.3. Trade-off curves

From the exhaustive measurement campaign, trade-off curves can be drawn with dv/dt versus the switched energy in Fig. 8. By drawing on the same graph the results from the variation of R_{gate_EXT} and the results from the variation of C_{gdEXT} (at $R_{gate_EXT} = 6.8\Omega$) one can conclude that the effect of C_{gdEXT} is more selective and provides less losses at same dv/dt . In another way, for a given dv/dt fewer losses are generated with an additional C_{gdEXT} than with the increase of R_{gate_EXT} . Indeed the extrapolation of the curve corresponding to the R_{gate_EXT} variations (red dotted line) is above the curve corresponding to the C_{gdEXT} variations.

For 6.8Ω the addition of $C_{gdEXT} = 22pF$ leads to a decrease of 23% of the dv/dt . The switching energy is 18% lower compared to the possible impact of an R_{gate_EXT} which leads to the same dv/dt . Those values are lower at higher current, at turn on and at turn off.

One can notice again the particular case of low current turn-off. The variations of the parameters have no impact on the dv/dt due to the "Inactive Miller Effect" mode. The losses are extremely low because there is no channel current and measurements are absorbed in noise.

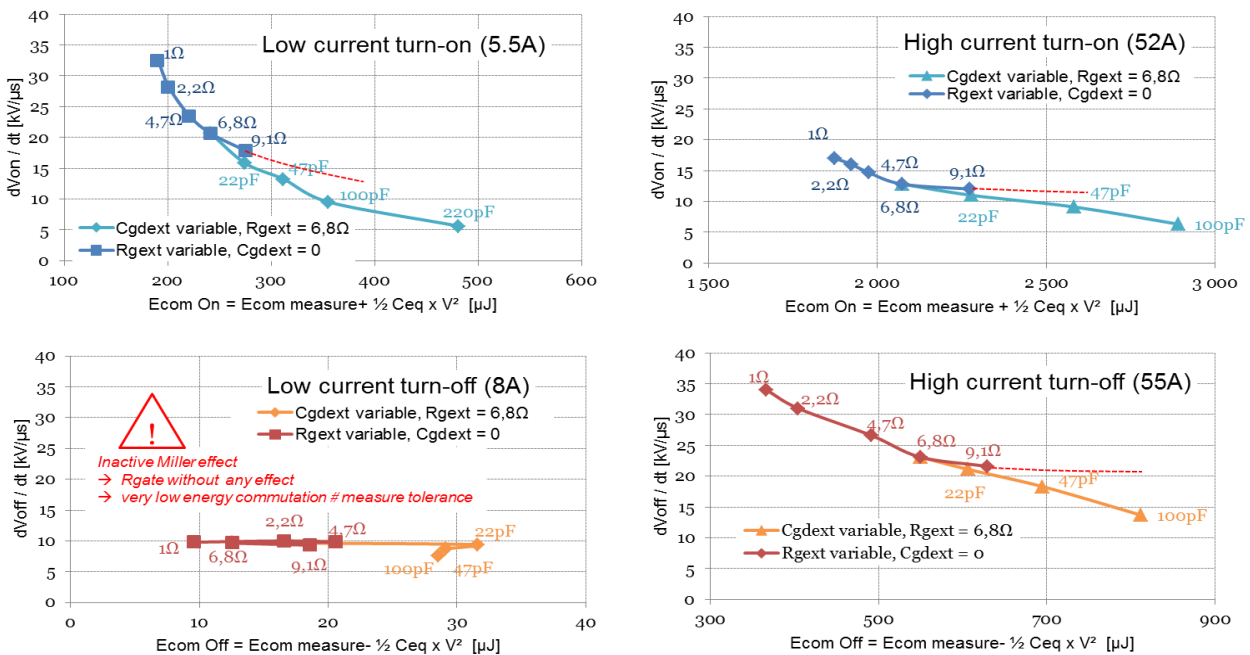


Fig. 8. dv/dt and energy commutation trade-off by using either R_{gate_Ext} . variation or C_{gd_Ext} . variation at low current turn-on (5.5A/8A – 600V) and high current turn-off (52A/55A – 600V) including two SiC Mosfet in the switching-cell. Note: $R_{gate_Int} = 5\Omega$. $R_{gate_total} = R_{gate_Ext} + R_{gate_Int}$.

5.4. dv/dt modeling and comparison with experimentation

A full range dv/dt modelling is an interesting way to predict the spectral magnitude of the switching voltage and so to pre-design the EMI filters.

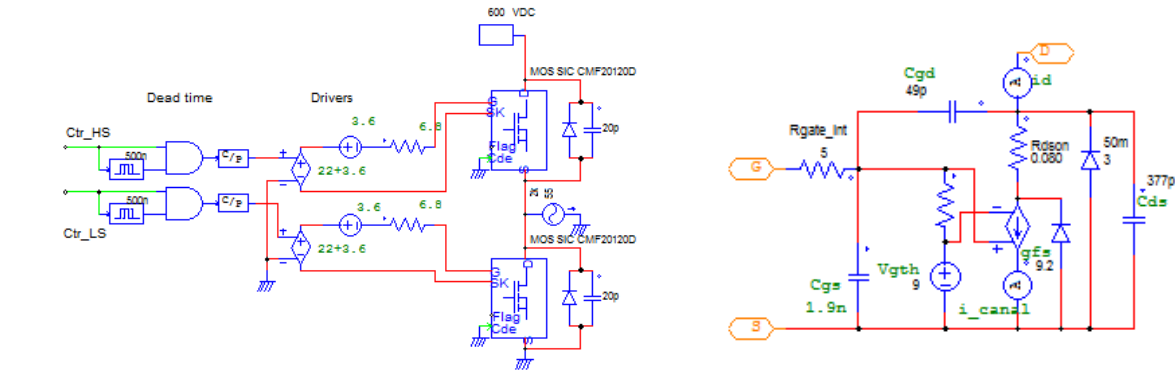


Fig.9 a) basic configuration for dv/dt analysis, b) equivalent 1st order linearized Mosfet model.

Figs. 9a) and b) remind the basic configuration of the circuit and the equivalent 1st order linearized model of the Mosfet device. Such a simplification permits to effectively establish a set of full range dv/dt models summarised in Tab.2. At turn-on the equation has no restriction domain, but at the turn-off as it is highlighted in §5.1 there are two different behaviours according to whether the Miller effect: active ($I_{load} \geq I_{load_limit}$) or inactive ($I_{load} < I_{load_limit}$). The calculation of this specific load current I_{load_limit} is given by Equ. 1.

$$I_{load_limit} = \frac{|2(C_{oss} + C_T) \cdot (V_{cde_off} - V_{gth})|}{C_{gd} \cdot R_{goff}} \quad (Equ.1)$$

	dv/dt at turn-on	dv/dt at turn-off	
	Without any restriction domain	For $I_{load} \geq I_{load_limit}$ $\rightarrow I_{channel} \geq 0$ \rightarrow Active Miller effect (AME model)	For $I_{load} \leq I_{load_limit}$ $\rightarrow I_{channel} = 0$ \rightarrow Inactive Miller effect (IME model)
DC/DC (1 Tr. - 1 Diode)	$\frac{g_{fs}(V_{cde_on} - V_{gth}) - I_{load}}{C_{oss} + C_T + C_{gd} \cdot g_{fs} \cdot R_{gon}}$	$\left \frac{g_{fs}(V_{cde_off} - V_{gth}) - I_{load}}{C_{oss} + C_T + C_{gd} \cdot g_{fs} \cdot R_{goff}} \right $	$\frac{I_{load}}{C_{oss} + C_T}$
DC/AC (2 Tr. - 2 Diodes)	$\frac{g_{fs}(V_{cde_on} - V_{gth}) - I_{load}}{2(C_{oss} + C_T) + C_{gd} \cdot g_{fs} \cdot R_{gon}}$	$\left \frac{g_{fs}(V_{cde_off} - V_{gth}) - I_{load}}{2(C_{oss} + C_T) + C_{gd} \cdot g_{fs} \cdot R_{goff}} \right $	$\frac{I_{load}}{2(C_{oss} + C_T)}$

Tab. 2 Complete and full range dv/dt modeling in DC/DC and DC/AC operation at turn-on and turn-off including active Miller effect and inactive Miller effect.

In the proposed model in Fig. 9b), all parameters have a constant value: V_{gth} , g_{fs} and C_{gd} are extracted from the data sheet in a first approach while C_{gd} and C_{ds} are specifically extracted by from the dv/dt measurements as illustrated in fig. 6. Note that a low current turn-off permits to easily yield the C_{oss} value due to the absence of active Miller effect. The extraction of C_{gd} requires the use of one of the dv/dt models presented in Tab. 2 in active Miller effect.

In Fig. 9, authors present a first comparison between the proposed dv/dt models and the dv/dt measurements according to the current switching and for different R_{gate} values. One can conclude at a good matching compared to the simple and very low cost of the modeling approach. Graphs in Fig. 10 are another way to expose the results dv/dt versus R_{gate} in the three cases: turn-on at low and high current, and finally turn-off at high current. Here again, one can conclude at a good matching of the models.

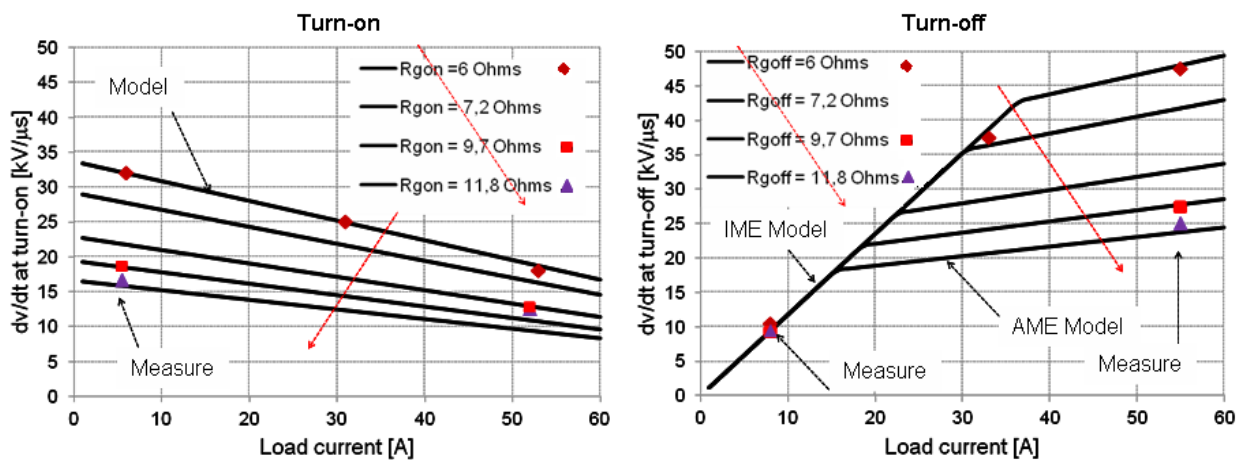


Fig. 9. dv/dt proposed models compared with experimental results over a wide range of load current. Parameter: total gate resistor ($R_{gate\ Ext.} + R_{gate\ Int.}$). Final fitting points: $V_{gth} = 9V$, $g_{fs} = 9.2A/V$, $C_{oss} = 426pF$, $C_{gd} = 49pF$.

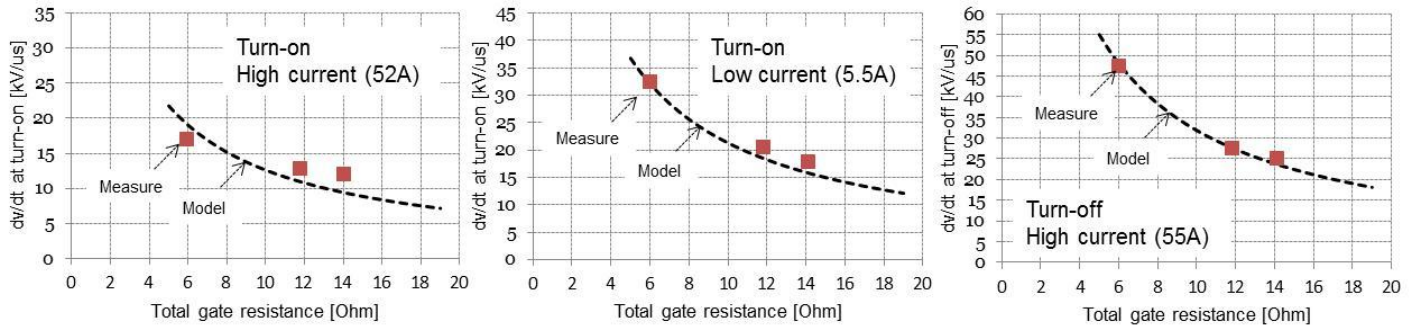


Fig. 10. dv/dt proposed models compared with experimental results over a wide range of gate resistance. Parameter: current switching. Final fitting points: $V_{gth} = 9V$, $gfs = 9.2A/V$, $C_{oss} = 426pF$, $C_{gd} = 49pF$.

6. Conclusion

A test bench for WBG power device in inverter configuration has been meticulously developed for dynamic measurement campaigns on a SiC Power Mosfet, the CREE CMF20120D. Therefore, trade-off curves (dv/dt versus switching energy) are obtained. They allow to concluding on the favourable impact of an additional C_{gd_EXT} rather than the impact of the classical increase of R_{gate_EXT} to obtain an optimum (low dv/dt, low switching energy). The authors finally propose a complete and full range dv/dt models that match with the measurement results.

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