Controlling the effective channel thickness of junctionless transistors by substrate bias

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Controlling the effective channel thickness of junctionless transistors by substrate bias

Dae-Young Jeon, Mireille Mouis, *Senior Member, IEEE*, Sylvain Barraud and Gérard Ghibaudo, *Fellow, IEEE*

***Abstract*—Substrate bias affected unique electrical characteristics of junctionless transistors (JLTs) were investigated in detail. Bulk channel thickness of JLTs (t_{si_eff}) was effectively modulated by back-gate bias (V_{gb}). The variation of threshold voltage (V_{th}) and mobility degradation were observed in the reduced t_{si_eff}, due to the negative V_{gb} induced depletion of free electrons. The V_{gb} effect was also influenced significantly by the doping concentration in JLTs. In addition, numerical simulations verified those results and analytical equations explained well the experimental results.**

***Index Terms*—Junctionless transistors (JLTs), substrate bias, effective channel thickness (t_{si_eff}), variation of threshold voltage, mobility degradation, numerical simulation, analytical equations.**

I. Introduction

Junctionless transistors (JLTs) have revealed robust performances such as less mobility degradation, reduced low-frequency noise, better reliability and enhanced immunity against short-channel effect (SCEs), due to structural simplicity without PN junctions and bulk conduction based operation [1-4]. The most important parameters such as threshold and flat-band voltage of JLTs are strongly influenced by the channel doping and the structural cross-section of devices [5-8]. In addition, the unique electrical characteristics and distribution of charge carriers of JLTs based on silicon-on-insulator (SOI) are significantly affected by back-gate bias, since there is a charge coupling effect between front and back interfaces [9-12]. JLTs have shown more sensitive to the back biasing as compared to conventional inversion-mode transistors in previous work [13] and further studies regarding the back biasing effect in JLTs are needed for tuning their electrical performance as well as better understanding operation mechanism.

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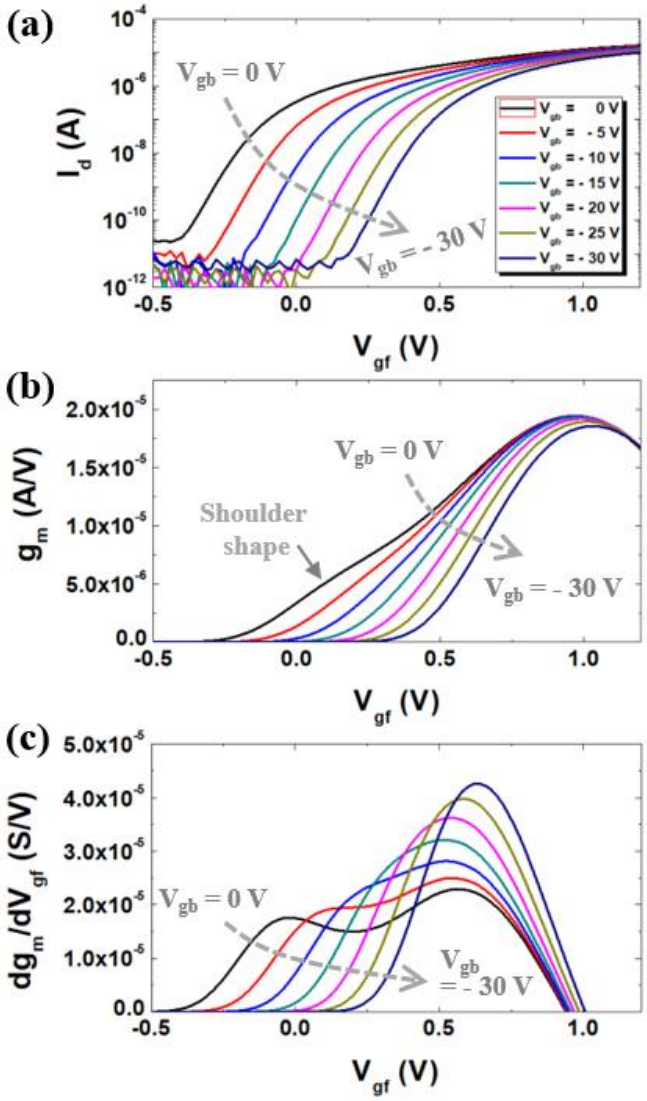

Fig. 1. (a) Transfer curves, (b) transconductance (g_m) and (c) derivative of g_m for long channel JLT (L = 10 μm) with various values of V_{gb}. The device was biased in the linear operation regime with V_d = 50 mV.

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In this paper, effective channel thickness (t_{si_eff}) of JLTs, with respect to bulk neutral conduction, was modulated by back-gate bias (V_{gb}). The reduced t_{si_eff} due to negative V_{gb} resulted in variation of threshold voltage (V_{th}) and pronounced mobility degradation of JLTs. Back biasing effect associated with the channel doping concentration in JLTs was also discussed. Moreover, numerical simulations and analytical model equations verified those results.

II. Experiments

N-type JLTs with high-k/metal gate stack were fabricated on (100) silicon on insulator (SOI) substrate at CEA-Leti, Grenoble France. Device Si thickness were thinned down to about 10 nm and the Si channel of JLTs were highly doped by implantation process with a phosphorus. The gate stack consisted in an HfSiON/TiN/Polysilicon structure with equivalent oxide thickness of ≈ 1.2 nm. Further detail material parameters of JLTs were described in previous work [11]. Gate-to-channel capacitance (C_{gc}) measurements were done by impedance analyzer HP4294a and then, effective doping concentration was extracted from sheet carrier density at flat-band voltage (V_{fb}) and Maserjian function. In addition, FlexPDE software was used for numerically simulated results and analytical modeling was carried out using MathCAD software.

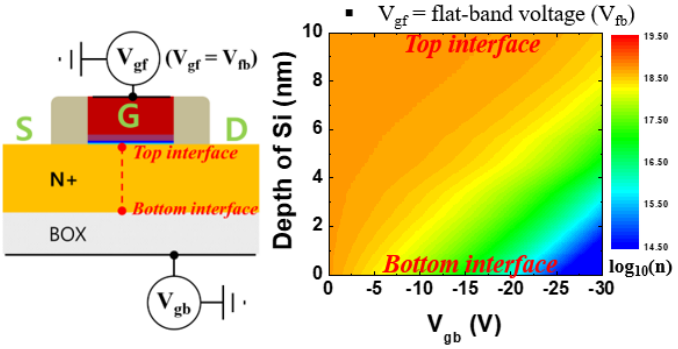

Fig. 2. Schematic of JLT structure and distribution of electron carrier concentration per unit volume (n) at $V_{gf} = V_{fb}$ with various values of V_{gb}.

III. Discussion

Transfer curves, transconductance (g_m) and derivative of g_m with varying substrate bias (V_{gb}) in the range of 0 V to – 30 V, were obtained on a long channel JLT (L = W = 10 µm) as shown in Fig. 1. A series resistance effect is neglected in the long channel device and effective doping concentration of the JLT was estimated as $N_d \approx 5 \times 10^{18}$ cm $^{-3}$. As decreasing V_{gb}, transfer curve of JLTs moved to the right as shown in Fig. 1(a). JLTs have two kinds of conduction channel such as bulk neutral (threshold voltage V_{th} < front-gate voltage V_{gf} < flat-band voltage V_{fb}) and surface accumulation channel ($V_{gf} > V_{fb}$). A shoulder shape on the g_m curve with $V_{gb} = 0$ V was observed due to the bulk neutral conduction channel in JLTs [11] and the shoulder was shrinking as decreasing V_{gb}. Derivative of g_m with $V_{gb} = 0$ V as shown in Fig. 1(c) revealed two clear peaks in black color. First peak (left-hand side) denotes the bulk conduction threshold, while second peak (right-hand side) represents the accumulation conduction threshold [14]. The first peak point moved toward the second peak as decreasing V_{gb} and finally, the dg_m/dV_{gf} with $V_{gb} = -30$ V showed only a single peak.

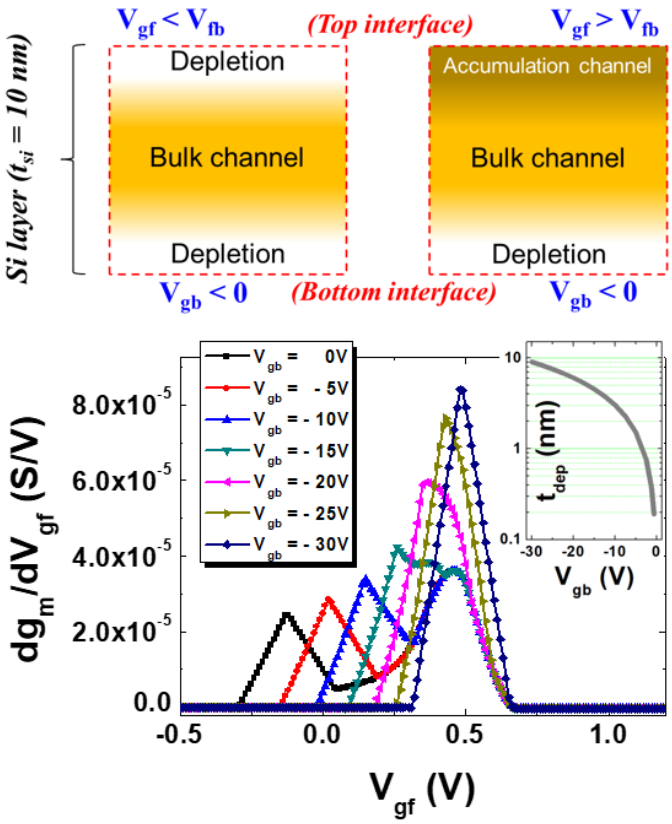

Fig. 3. Illustration showing the operating statues of JLTs with negative V_{gb}, and the V_{gb} dependent dg_m/dV_{gf} calculated from equation 1-3. The inset plot shows t_{dep} (thickness of the depletion regime) vs. V_{gb} calculated by equation 1.

It is well known that electrical properties of JLTs is strongly influenced by effective dimension and structure of devices [5-8,

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15]. As reducing a portion of bulk conduction channel in thinner device width, transfer curve and V_{th} of JLTs shifts to the right, since the bulk channel is fully depleted more easily in the thinner Si layer. Negative V_{gb} causes a depletion of electron carriers at the bottom interface and then, the bulk channel thickness of JLTs is effectively shrunk. Therefore, the results in Fig. 1 could be due to the reduction of effective bulk neutral channel thickness of JLTs with the negative V_{gb}, while the back inversion channel controlled by V_{gb} affects overall electrical behavior of conventional inversion-mode (IM) transistors with the double gate structure [9,13].

The back biasing characteristics of JLTs were visualized by numerical simulation works. Figure 2 shows distribution of electron carrier concentration per unit volume (n) at $V_{gf} = V_{fb}$ with varying V_{gb}. The entire Si channel is full of electron charge carriers with $\log_{10}(n) \approx 18.7$ [thus $\log_{10}(N_d = 5 \times 10^{18}$ cm $^{-3})$] in orange color at $V_{gb} = 0$ V. The concentration of charge carriers at the bottom interface between Si channel and buried oxide (BOX) is getting decreasing as decreasing V_{gb}. Then, a depleted layer in blue color is created at the bottom interface for further decrease of V_{gb} and effective channel thickness is noticeably thinned at $V_{gb} = -30$ V. As a result, one can expect that effective channel thickness in JLTs is well modulated by a negative back-gate bias.

The operating statuses of JLTs with negative V_{gb} are described in the illustration of Fig. 3. The negative V_{gb} results in a depletion of electron carriers at the bottom interface and the thickness of the depletion regime (t_{dep}) is calculated by:

$$t_{dep} = \frac{\varepsilon_{si}}{C_{box}} \times \left(\sqrt{1 - \frac{2 \times V_{gb} \times C_{box}^2}{q \times \varepsilon_{si} \times N_d}} - 1 \right) \quad (1)$$

where q, ε_{si} and C_{box} are the electronic charge, Si permittivity and BOX capacitance per unit area, respectively [16]. Therefore, the mobile electron charge (Q_n) in the Si channel of JLTs can be derived as [5, 17]:

when $V_{gf} < V_{fb}$,

$$Q_n(V_{gf}) = q \times N_d \times \left[t_{si} - \frac{\varepsilon_{si}}{C_{ox}} \times \left(\sqrt{1 - \frac{2 \times (V_{gf} - V_{fb}) \times C_{ox}^2}{q \times \varepsilon_{si} \times N_d}} - 1 \right) - t_{dep} \right],$$

or when $V_{gf} > V_{fb}$,

$$Q_n(V_{gf}) = C_{ox}(V_{gf} - V_{fb}) + q \times N_d \times t_{si} - q \times N_d \times t_{dep} \quad (2)$$

where C_{ox} means oxide capacitance per unit area at the top interface. Finally, drain current in the linear operation mode can be obtained by:

$$I_d(V_{gf}) = \frac{W}{L} \times \mu \times Q_n(V_{gf}) \times V_d \quad (3)$$

where μ and V_d represent the electron carrier mobility and drain bias, individually.

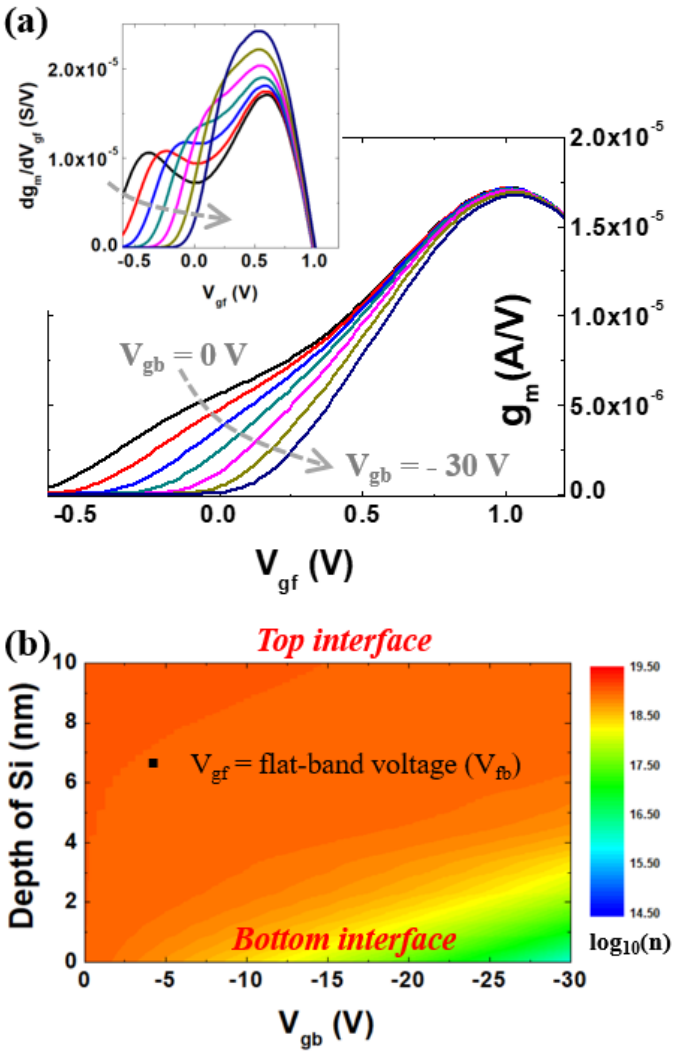

Fig. 4. (a) V_{gb} influenced transconductance and its derivative of JLT with higher doping level ($N_d \approx 10^{19}$ cm $^{-3}$). The device was biased in the linear operation regime with $V_d = 50$ mV. (b) Distribution of electron carrier concentration per unit volume (n) at $V_{gf} = V_{fb}$ with various values of V_{gb}.

The plots in Fig. 3 show V_{gb} dependent derivative of g_m (dg_m/dV_{gf}), which are calculated from equation 3. Trend of the

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calculated dg_m/dV_{gf} with varying V_{gb} was quite consistent to the experimental results in Fig. 1(c), although the equation 1 should be revised with considering a strong coupling effect between front and back gate in ultra-thin thickness [9]. Moreover, Zhang et al. reported that the thickness of bulk neutral channel in a junctionless-like transistor, based on 2-dimensional nanomaterials, was controlled by the back bias and significantly affected the threshold voltage [18].

Figure 4(a) shows V_{gb} affected behavior of transconductance in JLT with two times larger in effective doping concentration ($N_d \approx 10^{19}$ cm $^{-3}$). For V_{gb} = 0 V, the shoulder shape was more pronounced and the first peak of dg_m/dV_{gf} in the inset determined a lower threshold voltage, as compared to those in Fig. 1(b) and 1(c). The variation as decreasing V_{gb} in Fig. 4(a) showed a similar trend with that in Fig. 1. However, more noticeable bulk conduction with thicker effective channel even at $V_{gb} = -30$ V is expected in the JLT with higher doping level, since the t_{dep} is decreased with increasing N_d in the equation (1). Indeed, the depleted regime induced by negative V_{gb} in Fig. 4(b) was less clear than that in Fig. 2 with the lower doping concentration.

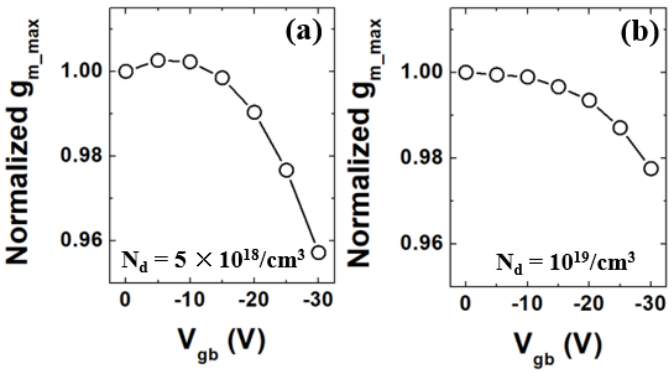

Fig. 5. Normalized g_{m_max} [$g_{m\_max}(V_{gb})$/ $g_{m\_max}(V_{gb} = 0$ V)] with different doping concentration [(a) $N_d \approx 5 \times 10^{18}$ cm $^{-3}$ and (b) $N_d \approx 10^{19}$ cm $^{-3}$].

In addition, maximum g_m (g_{m_max}) of the higher doped JLT was slightly varied as changing V_{gb} in Fig. 4(a), while a considerable variation of g_{m_max} was observed in Fig. 1(b). Those features were quantitatively plotted with the normalized g_{m_max} [$g_{m\_max}(V_{gb})$/ $g_{m\_max}(V_{gb} = 0$ V)] as shown in Fig. 5. The transconductance shape is strongly related to the behavior of carrier mobility [19-21]. Therefore, negative V_{gb} seems to give rise to a mobility degradation in JLTs and the degradation is mitigated in higher doped JLTs.

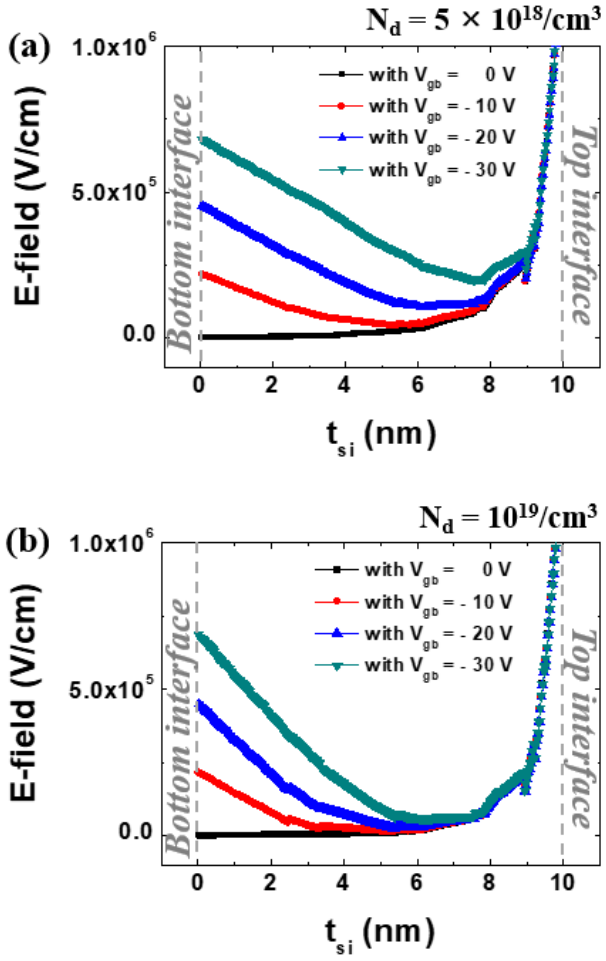

Fig. 6. E-field distribution along the Si channel from bottom to top interface of JLTs with (a) $N_d \approx 5 \times 10^{18}$ cm $^{-3}$ and (b) $N_d \approx 10^{19}$ cm $^{-3}$.

Electric-field (E-field) distribution along the Si channel from bottom to top interface was investigated to verify less mobility degradation in the JLTs with higher doping concentration. Figure 6 shows the E-field distribution in the strong accumulation mode (at V_{gf} = 1.2 V) of JLTs with applying negative V_{gb}. The E-field from the back-gate bias could influence to the bulk neutral channel of JLTs and its impact is reinforced as decreasing V_{gb} (at a large negative value). For the higher doping ($N_d = 10^{19}$ cm $^{-3}$) in Fig. 6(b), the magnitude of E-field near the bottom interface was clearly much smaller than that in the JLT with lower doping ($N_d = 5 \times 10^{18}$ cm $^{-3}$) in Fig. 6(a). The reduced E-field in the higher doped channel could

result in the less degradation of mobility caused by back-gate bias in JLTs. Jang et al. also reported that Charge carrier scattering and fluctuation could be induced at the interface between bulk neutral channel and the depleted regime in the partially depleted operation of JLTs [22].

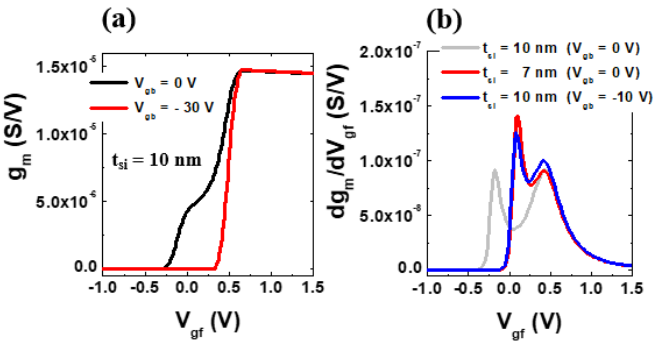

Fig. 7. (a) Back-gate bias dependent g_m behavior calculated from equation 2 and 3 (N_d = 0.5 × 10^{19}/cm^3, W = L = 10 μm and V_d = 50 mV), (b) Simulated dg_m/dV_{gf} with different values of t_{si} (the gray curve means the dg_m/dV_{gf} of a single gate JLT with t_{si} = 10 nm for a comparison).

The change of g_m in JLTs due to the back-gate bias was calculated from equation 2 and 3, as shown in Fig. 7(a). The behavior of electron charges in the channel is modulated by the V_{gb}, and then the g_m was reduced by negative V_{gb} which is consistent to experimental results in Fig. 1(b). However, maximum value of g_m in Fig. 7(a) was not changed. Therefore, the mobility degradation shown in Fig. 5 is due to an additional E-field effects at the bottom interface, as explained in Fig. 6. Furthermore, if the physical channel thickness of a single gate JLT equals to the effective channel thickness of a back gated JLT, both electrical characteristics could be very same. Indeed, the dg_m/dV_{gf} behavior of a single gate JLT with t_{si} = 7 nm was very similar to that of a back gated JLT with the effective channel thickness ≈ 7 nm (t_{dep} ≈ 3 nm at V_{gb} = − 10 V) as the plots in Fig. 7(b).

IV. Conclusions

We have shown how back-gate bias (V_{gb}) can modulate the effective channel thickness (t_{si_eff}) of SOI based JLTs. The t_{si_eff} was reduced by a negative V_{gb} and those resulted in the right-shift of threshold voltage (V_{th}) of JLTs. Numerical simulation visualized the V_{gb}-controlled t_{si_eff} with the distribution of free electron concentration in the channel of JLTs and analytical equations, with considering the depletion of free electron carriers caused by negative V_{gb}, explained well the experimental results. In addition, mobility degradation due to V_{gb} induced transverse E-field near the bottom interface was observed, and JLTs with higher doping concentration were less affected by the E-field and showed better immunity against the mobility degradation.

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