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Marc Margalef-Rovira, Abdelhalim Saadi, Sylvain Bourdel, Manuel J. Barragan, Emmanuel Pistono, et al.. mm-Wave Through-Load Switch for in-situ Vector Network Analyzer on a 55-nm BiCMOS Technology. 18th IEEE International NEWCAS Conference (NEWCAS 2020), Jun 2020, Montreal, Canada. 10.1109/NEWCAS49341.2020.9159829 . hal-02958204

HAL Id: hal-02958204

<https://hal.science/hal-02958204v1>

Submitted on 5 Oct 2020

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mm-Wave Through-Load Switch for in-situ Vector Network Analyzer on a 55-nm BiCMOS Technology

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Abstract—In this paper, an innovative millimeter-wave (mm-wave) through-load switch for in-situ reflectometers and on-wafer calibration is proposed. This two-port device can switch between two states: (i) a through connection or (ii) a 50 Ω load for both of its ports. The through-load switch is composed of a 3-dB directional coupler and two nMOS transistors controlled through a biasing voltage applied to their gate. Measurement results of a 120-GHz 3-dB directional coupler are provided up to 145 GHz together with EM simulations and circuit-level simulations up to 220 GHz of the through-load switch. A wide bandwidth is obtained, from 73 GHz to 179 GHz, with limited insertion loss of 2 dB.

Keywords—mm-wave, switch, 3-dB slow-wave coupler, in-situ reflectometer, on-wafer calibration.

I. INTRODUCTION

Current intensive use of the radiofrequency spectrum for different applications has led to overflow submillimeter-wave bands. In addition, the modern use of wireless systems for purposes such as video broadcast, Internet of Things (IoT) or high-data-rate communications demands larger bandwidths in order to achieve high speed communications (e.g. 5G or beyond-5G applications). In order to fulfill this demand, systems are moving into the mm-wave band (30-300 GHz), where the frequency allocation remains unobstructed and larger bandwidths can be achieved.

Accurate measurements are necessary for the characterization of these mm-wave circuits. Up to now, most of the time, external calibration kits on alumina substrates are used. However, above 50-100 GHz, this characterization approach suffers from high measurement uncertainties due to difference of dielectric constant between the calibration kit and the silicon wafer, and also the coupling between the probes and the silicon wafer [1,2]. To overcome these issues, some authors propose to integrate an on-wafer calibration kit together with the DUT (Device Under Test) [3]. However, the synthesis of wideband 50 Ω loads, needed for Load-Reflect-Reflect-Match (LRRM) [4] or Through-Reflect-Match (TRM) [5] calibration, is a cumbersome issue in the mm-wave band due to the sensitivity to parasitic effects and dispersion. Hence, the vast majority of on-wafer mm-wave calibration kits use a multi-line Through-Reflect-Line (TRL) calibration [6], which does not require a known load. Although on-wafer TRL is considered as

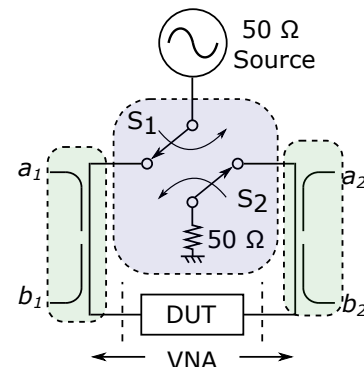


Fig. 1 a) Simplified schematic of a 2-port VNA. The switches and the load are in the blue box. The bidirectional couplers are in the green boxes.

a good candidate to improve measurement accuracy, the Line standard length constitutes a drawback, even at mm-waves, since it leads to large areas. Having accurate wideband 50- Ω loads would permit to overcome this issue.

Another issue linked to mm-wave measurements is linked to the insertion loss of the cable and coplanar probe connecting the source (the VNA) and on-wafer pads. This limits the overall directivity of the system and constitutes an issue for load-pull measurements [7]. In this scenario, together with the development of nanometric technologies, some authors proposed the integration of in-situ measurement setups, such as Vector Network Analyzers (VNAs) (i.e. reflectometers) [8-10]. In-situ measurement systems present the advantage of being physically close to the DUT and being integrated into the same environment, thus reducing the losses and transitions from the VNA to the DUT. In addition, they are more resistant to probing issues, such as probe misalignment, coupling to the substrate, imbalances in the probe contact, to name few. Moreover, complete in-situ VNAs greatly reduce the characterization equipment cost.

Fig. 1 displays a simple 2-port VNA schematic. Such a system injects a signal into one port of the DUT while sampling part of the reflected and transmitted waves using bidirectional couplers. The second port of the DUT is connected to a 50- Ω load. Then, it commutates the state of the switches and injects the signal into the second port of the DUT, while sampling the transmitted and reflected waves. This process allows to fully

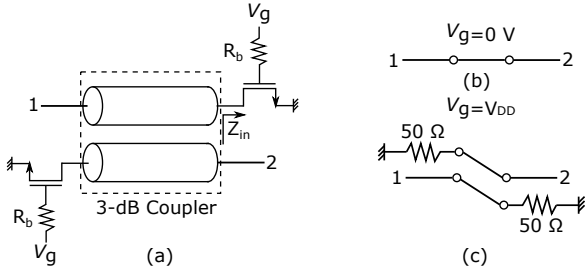


Fig. 2 a) Schematic design of the proposed through-load switch. Transistors are connected to the coupled ports of the coupler b) Function of the proposed device when $V_g = 0$. c) Function of the proposed device when $V_g = V_{DD}$.

characterize the S-parameters of the DUT. Some of the critical elements for in-situ VNAs are the switching system and the load (blue box in Fig.1). This system has to present low-loss, high isolation, while allowing to synthesize a 50- Ω load. Such a system presents two major challenges: (i) design of a switch with low $R_{on} \cdot C_{off}$ to achieve low-loss and isolation and (ii) design of a wideband 50- Ω load. This leads to a cumbersome co-design between the load and the switching system.

In this work, authors propose the use of a compact size 3-dB directional coupler together with two nMOS transistors to create a device that can either act as a through connection or as a 50- Ω load. Such a through-load device would solve both issues discussed above concerning TRM or LRRM on-wafer calibrations, when designed as a load. Additionally, this device can be used as a basic building block for in-situ VNAs. The proposed through-load device integrates two RF functions that are traditionally designed as two separate devices: a switch and a load. In addition, it drastically reduces the trade-off between R_{on} and C_{off} of a traditional switch, allowing the designer to focus only on C_{off} . Moreover, the design allows synthesizing wideband 50- Ω loads. To the best of authors' knowledge, this is the first time that such topology is proposed. For the sake of simplicity, this paper considers 50 Ω as the goal impedance, since it is the reference impedance of most commercial systems. However, the concept theoretically holds for any other normalization impedance.

This paper is organized as follows: section II presents the proposed architecture. In section III, measurement and simulation results of the device are provided. Finally, section IV presents the main conclusions of this work.

II. PROPOSED ARCHITECTURE

The proposed concept takes advantage of the large bandwidth, in terms of matching and isolation, presented by coupled-line couplers, which is intrinsically greater than its branch-line counterparts concerning its matching and the output signals phase difference. The concept behind this work is pretty straightforward, it is based on the circuit shown in Fig. 2, composed of a 3-dB coupler and two nMOS transistors in a common-source configuration in the coupler coupled ports.

A. Working principle

Let us consider an ideal 50- Ω coupled-lines 3-dB backward coupler: when the output ports of the coupler are loaded with highly reflective impedances (i.e. open-circuit or

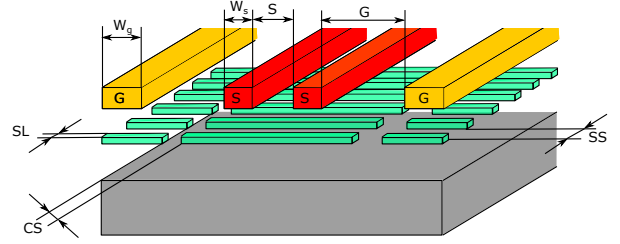


Fig. 3 Coupled-lines Slow-wave CPW architecture with a cut on the sides of the floating ribbons.

short-circuit) the input signal in port 1 is totally transmitted to port 2. On the other hand, when the coupled ports present 50- Ω loads, the signal is dissipated into the loads, port 2 being isolated. In addition, due to the nature of the coupler, the device is always matched at the center frequency of the coupler if same loads are used. Non-idealities of the load affect the isolation and the bandwidth but their effect on the device impedance is almost negligible. This is the principle behind Reflection-Type Phase Shifters [11].

B. The Load

The transistors switch between two states (OFF-state for $V_g = 0$ and ON-state for $V_g = V_{DD}$) thanks to the biasing voltage, V_g , applied to their gates through a high-value resistance, R_b . The performed RF functions in the OFF and ON-states of the transistors are depicted in Figs. 2(b) and 2(c), respectively. The transistors are sized in such a way that the real part of their input impedance, Z_{in} , is close to 50 Ω in the ON-state. In most of the integrated technologies this represents a high value resistance for the ON-state, R_{on} . This greatly relaxes the trade-off existing between R_{on} and the OFF-state capacitance, C_{off} . Hence, it allows the designer to use small transistors, which present low input capacitances and thus smaller imaginary part of their input impedance.

Finally, the 3-dB coupler is based on coupled Slow-wave CPW architecture [12]. This architecture is briefly described in the next sub-section.

C. The 3-dB Coupler

The coupler was designed using Coupled Slow-wave CPWs, which are greatly inspired from the Slow-wave CoPlanar Waveguide (S-CPW) architecture [13]. Coupled Slow-wave CPWs, shown in Fig. 3, are composed of two signal strips, two ground strips and a set of floating metal ribbons placed underneath. The CS-CPWs take advantage of the floating shield to: (i) reduce the electrical length of the coupler through the slow-wave effect, (ii) increase the electrical coupling between

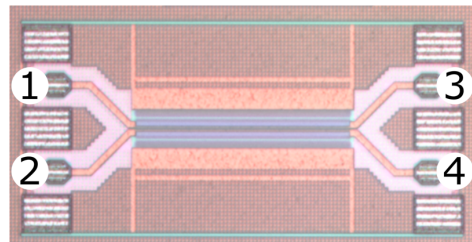


Fig. 4 Micrograph of the fabricated coupler with the de-embedded access and port numbering.

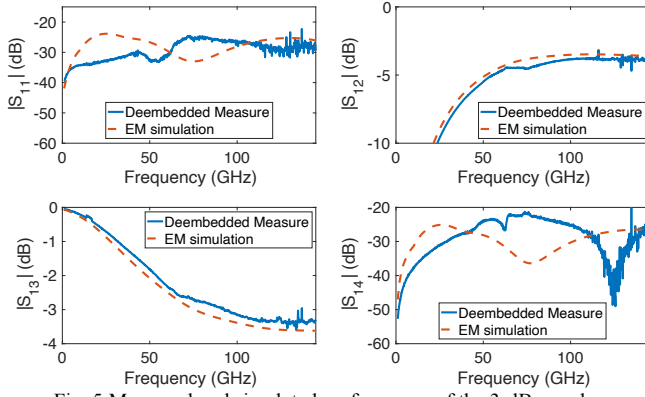


Fig. 5 Measured and simulated performance of the 3-dB coupler.

the signal strips and (iii) the directivity of the coupler. This structure was firstly introduced in [12]. In this work, authors explored the performance and versatility of the structure, introducing a cut on the fingers giving the designer an extra degree of freedom. After that, several works have reported the use of CS-CPWs for the integration of different RF functions such as: phase shifting [14], impedance matching [15], Marchand balun design [16], and for coupler design [17].

III. MEASUREMENT AND SIMULATION RESULTS

The key block in the proposed device is the integrated 3-dB coupler. As discussed above, the requirements on the transistor can be relaxed. A 3-dB CS-CPW coupler, whose micrograph is shown in Fig. 4, with a central frequency of 120 GHz was designed, fabricated and characterized in STM 55-nm BiCMOS technology. The complete device is then validated in simulation by considering the fabricated 3-dB coupler behavior and the simulation models for the transistors and resistors provided in the Process Design Kit (PDK).

The selected 55-nm technology features 8 metal layers, where the top-metal is a thick metal, ideal for TL design and power distribution, metals 6 and 7 are of an intermediate thickness and the rest are thin metals, ideal for routing digital blocks. In order to achieve the desired performance, metals 7 and 8 were stacked using vias and used to create the signal and ground strips. The floating shield was placed on metal 5, at around 2 μm below the signal and ground strips. The length of the coupler is 255 μm . The width of the signal, W_s , and ground strips, W_g , are equal to 2 μm and 15 μm , respectively. The spacing between signal strips, S , and signal to ground, G , are equal 2 μm and 20 μm , respectively. The width of the floating strips, SL , and the spacing between them, SS , are equal to 0.5 μm . Finally, the side-cut, CS , was designed using a 5 μm gap.

The coupler was measured using an Anritsu VectorStar® ME7838A4 VNA from 70 kHz up to 145 GHz. Fig. 5 plots the S-parameters of the de-embedded measurement together with the EM simulation. Simulation and measurement show very good agreement. At 120 GHz, the measured coupler exhibits -3.2 dB at the thru port (S_{13}), -3.7 dB at the coupled port, 40 dB of isolation and 28 dB of return loss.

Thanks to the good agreement between EM simulation and measurement, the rest of this paper uses EM simulation-based results of the coupler, which were carried out up to 220 GHz.

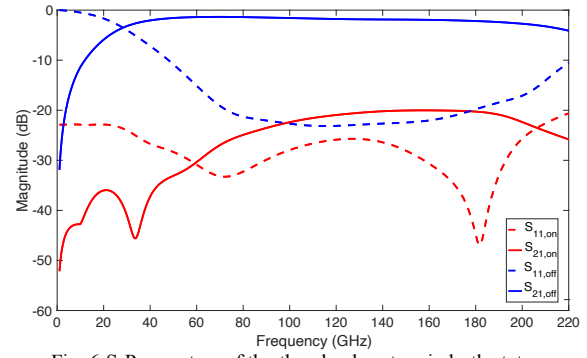


Fig. 6 S-Parameters of the thru-load system in both states.

This allows to show the capabilities of the proposed approach up to very high frequencies.

The nMOS transistors were designed with a total width of 8.1 μm , distributed in three fingers, and a length of 55 nm. The resistor was designed using the high resistivity polysilicon featured in this technology, which allows to obtain high-value resistors with low area overhead. In particular R_b has a width of 0.9 μm and a length of 9 μm , for a total resistance of 62 k Ω .

Fig. 6 presents the results of the through-load switch from 1 GHz to 220 GHz in both states. In the OFF-state, the circuit behaves as a through connection over a wideband, thanks to the low C_{off} and high OFF-state resistance, R_{off} , presented by the transistors. If a return loss greater than 20 dB is considered, the bandwidth of the device extends from 73 GHz to 179 GHz. In the middle of the band, at 120 GHz, the proposed device presents 1.8 dB of insertion loss. On the other hand, when the device is in the ON-state, it behaves as a 50- Ω matched load with an average return loss of 25 dB and an isolation between both ports greater than 19 dB throughout the whole analyzed frequency band.

In addition to the double functionality that the through-load switch presents, as stated before, the nature of the coupler ensures the proper matching. Fig. 7 shows the reflection coefficient of the through-load switch, in blue, and the reflection coefficient at the input of the nMOS transistor, in red, respectively, from 1 GHz to 220 GHz. Note that the blue curve is closer to the center of the Smith chart throughout the whole analyzed band, meaning that the system is better matched to 50 Ω .

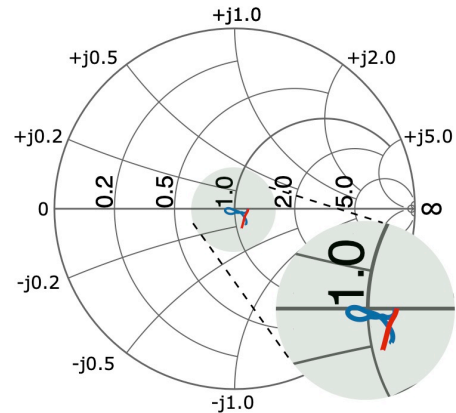


Fig. 7 Reflection coefficient from 1 GHz to 220 GHz of the thru-load in the ON-state (blue) and at the input of the nMOST in its ON-state (red).

Table I shows a comparison between state-of-the-art mm-wave switches, which could be used for in-situ VNA applications. The works in [18], [20] and [22] present Double-Shunt Single-Pole Double-Thru (DS SPDT) switches, while the works in [19] and [21] use switched coupled lines. The works in [18-21] are focused on 2-port characterization and employ an on-chip 50-Ω resistor load to terminate one of the ports of a SPDT switch. Although the through-load device is validated by simulation, it shows very good performance, which is promising for a further implementation. A complete integrated demonstrator will be sent to fabrication to validate the complete architecture.

Table 1. State-of-the-art mm-wave switches.

Ref.	Frequency (GHz)	RL (dB)	IL (dB)	Iso. (dB)	Area (mm ²)	Topology
[18]	140-220	> 10	3 -4.5	20-30	0.29	DS SPDT
[19]	220-285	> 10	4.2 -5	17-19	0.002	Switched Lines
[20]	110-160	> 10	2.6 -4	22	0.21*	DS SPDT
[21]	130-180	> 10	3.3 -4	21-23	0.004	Switched Lines
[22]	50-110	> 10	5 - 6	20-25	0.56*	DS SPDT
This work	77-179	> 20	1.4 - 2.2	20-30	0.019	3-dB Coupler

*Pads included

IV. CONCLUSIONS

In this paper, an innovative through-load switch architecture has been presented using a CS-CPW-based 3-dB directional coupler and two loads using nMOS transistors. This architecture has a double functionality, which has traditionally been integrated using switches and loads. The topology is interesting for in-situ reflectometers as well as for on-wafer calibration techniques needing a Match standard, as LRRM and TRM.

Measurements of the directional coupler from 70 kHz to 145 GHz were provided. In addition, EM simulations together with electrical simulations of the whole device were carried out to show the performance of the device up to 220 GHz.

The presented device presents a bandwidth greater than 100 GHz, with 1.8 dB of insertion loss in its OFF-state at 120 GHz. On the other hand, for the ON-state, the circuit exhibits a return loss and an isolation greater than 20 dB and 19 dB throughout the whole band, respectively.

ACKNOWLEDGMENT

This work has been funded by the European Union (ECSEL JU GA 737454: TowARds Advanced BiCMOS NanoTechnology platforms for RF applicatiOns - Taranto), and the General Directorate for Enterprises (DGE) in France.

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