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A Stored Energy Control Based Active DC Filter for the Alternate Arm Converter with an Extended Overlap Period

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Keywords

«AAC», «Active Filter», «Control», «HVDC»

Abstract

The Alternate Arm Converter (AAC) is a multilevel Voltage Source Converter (VSC) suitable for HVDC systems with DC-fault blocking capability. In its "Short-Overlap" configuration (SO-AAC) it requires a bulky passive DC filter to suppress the DC current ripple caused by the rectification of the grid currents in the DC link. With an Extended-Overlap period (EO-AAC), an active DC filtering control strategy can be implemented thanks the fact that there is always one phase in overlap mode, providing a continuous control of the DC current. Previous works have been realized considering DC inductors at each pole of the DC link. In this paper, a stored energy control assessment is proposed leading to the deduction of a stored energy model allowing a formal DC current control without DC inductors. The proposed control is supported through a static analysis and dynamic simulation in order to demonstrate its effectiveness.

Introduction

High Voltage Direct Current (HVDC) transmission system has been one of the major interest these last ten years and especially since the advent of the Modular Multilevel Converter (MMC). The MMC-HVDC is a multilevel converter that can generate high quality electrical quantities (e.g. AC and DC currents) thanks to the use of hundreds of stacked Sub-Modules (SM) in its arms [1],[2]. In its Half-bridge (HB) SMs version, the MMC has for main shortcoming to be intolerant to DC Fault as it cannot oppose the grid voltage letting the fault current flowing through the SM free-wheeling diodes. This issue can be overcome by using Full-bridge (FB) SMs, however, an increase in losses is observed making this solution less interesting in grid application. Thereby, different solutions for converter with DC fault blocking capability have been explored. The first ones lies in more advanced SMs topologies for MMC allowing voltage bi-polarity (mandatory to oppose the grid voltage) and a limited impact on the power losses [3]. The other solutions have consisted the development of new multilevel VSCs topologies with DC-Fault blocking capability. Among these new topologies, the Alternate Arm Converter (AAC), a hybrid topology between a MMC and a two-level VSC, has emerged and became a promising structure thanks to some interesting features. Indeed, in addition to its DC fault blocking capability, the AAC is compact since it is equipped with a reduced number of SM and embedded capacitive energy storage than the MMC [4],[5]. These characteristics are allowed by its specific operations which are described further.

The generic three phases representation of the AAC is illustrated on Fig. 1. An AAC arm consists in serial connection of the so called Director Switch (DS) and a stack of SMs. The classical topology of SMs is the FB-SM which provides the DC fault blocking capability. The DS is composed of several power transistors connected in series in the same way as the two-level VSC. They are controlled in a

such a way that the grid current is conducted alternately by the upper and lower arms, thereby, the upper arm synthesises the positive part of the AC voltage whereas the lower arm is in charge of the negative part. This alternate mode of operation of the arms provides the aforementioned features that makes the AAC an interesting topology for HVDC application (i.e. reduced number of SM and energy storage). However, this basic operating mode, also called in this paper Non-overlap mode, prevent from having a full control of the AAC dynamics that may leads to a uncontrolled deviation of its internal stored energy. Therefore, to ensure the energy equilibrium at both sides of the converter an Overlap mode has been introduced.

During a given time called overlap period (duration of the overlap mode), the upper and lower DS are both closed allowing a temporary MMC leg behaviour improving the converter controllability. Thus, as for the MMC, a current can flows through the DC link and phase leg. This current, also called overlap current in this paper, can be used to control the stored energy inside the converter in order to maintain the overall power balance as in [6],[7],[8].

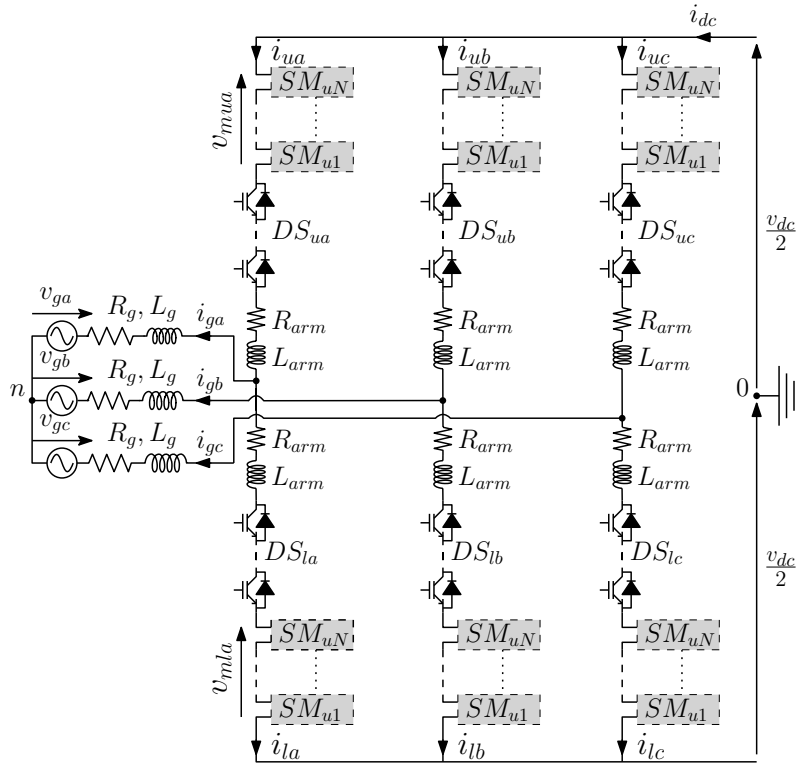


Fig. 1: Alternate Arm Converter scheme

As most of the topologies, the AAC has also some shortcomings. The AAC, as it was originally proposed by [4], now called Short-Overlap AAC (SO-AAC) [9], is known for having a restricted range of operation close to an energy "sweet-spot" which ensures no deviation of its internal stored energy [4] over the time. Operation far from this operating point leads to high energy balancing current imposing very high dynamics to the overlap current control. The second drawback of the SO-AAC, is the passive DC filter needed to filter the harmonics rejected by the Non-overlap mode in the DC current. To overcome this latter, the Extended-Overlap AAC (EO-AAC) has been proposed. The EO-AAC is an AAC that operates with an overlap angle of 60 degrees (overlap period measured in degrees) ensuring one phase leg in overlap mode at each moment. The purpose of the extended overlap period, is to modify the classical AAC control in order to output a constant DC current allowing to remove the passive DC filter needed by the SO-AAC. So far, solutions based on the use of DC inductors have been proposed by [10] and [11]. This present paper, describes how, by the mean the AAC internal stored energy an active DC current filtering control strategy can be deduced in a formal way and without considering DC inductors.

To do so, the first section is dedicated to the presentation of the AAC operating principles and basics of the energy equilibrium. Then, a presentation of the AAC conventional stored energy controller is pro-

posed to highlight its inability to provide the expected active DC filter as the DC current is not explicitly controlled. Thus, the last section introduces another stored energy model which provides at the same time a control of the stored energy and the active DC filtering feature.

Operating Principles of the AAC

As previously mentioned, the AAC operations are composed of two operating modes (Non-overlap and Overlap) which modify the electrical circuit and the converter control capabilities.

Non-overlap Mode

In Non-overlap mode, only one arm conducts the grid the current. Based on Fig. 1 and assuming the upper arm of the 'j' phase conducting gives:

$$v_{gj} + (R_g + R_{arm}) i_{gj} + (L_g + L_{arm}) \frac{di_{gj}}{dt} = \frac{v_{dc}}{2} - v_{muj} \quad (1)$$

Defining v_{vj} such as:

$$v_{vj} = v_{gj} + (R_g + R_{arm}) i_{gj} + (L_g + L_{arm}) \frac{di_{gj}}{dt} \quad (2)$$

According to (2), in Non-overlap mode only the grid current i_g can be controlled thanks to v_v . However, the converter has to control the power flow and its internal stored energy, in this operating mode only one of this two tasks can be achieved since only the grid currents are controllable. To perform the second control, the Overlap mode is introduced to give access to a second current.

Overlap mode

In Overlap mode, both arms of a phase leg participate to the AC voltage synthetization. This operating mode is therefore considered as a MMC-like mode. Thereby, the MMC decoupled model can be temporary used to control the AC and DC powers separately. First, the decoupling variables are introduced:

$$v_{\Sigma j} = \frac{v_{muj} + v_{mlj}}{2}; \quad v_{vj} = \frac{-v_{muj} + v_{mlj}}{2}; \quad i_{\Sigma j} = \frac{i_{uj} + i_{lj}}{2} \quad (3)$$

Where, $v_{\Sigma j}$ represent the converter inner DC voltage, v_{vj} the AC voltage synthesized by the converter, and $i_{\Sigma j}$, the equivalent MMC differential current. Thus, the current models can be derived and given in the equations (4).

$$\begin{cases} v_{gj} + \left(R_g + \frac{R_{arm}}{2}\right) i_{gj} + \left(L_g + \frac{L_{arm}}{2}\right) \frac{di_{gj}}{dt} = v_{vj} \\ R_{arm} i_{\Sigma j} + L_{arm} \frac{di_{\Sigma j}}{dt} = \frac{v_{dc}}{2} - v_{\Sigma j} \end{cases} \quad (4)$$

Using the models above provide a decoupled control of the AC and DC powers. The AC power is still controlled with i_{gj} thanks to v_{vj} while the DC power is regulated with $i_{\Sigma j}$ through $v_{\Sigma j}$. In this paper, the AC side is in charge of the power flow (based on the grid requirement) and the DC side is used to the regulation of the AAC internal stored energy.

Energy Equilibrium in the AAC

Unlike the MMC, open loop control as the well known Circulating Current Suppressing Control (CCSC) to maintain the converter stored energy around its nominal value is impossible. The AAC arms instantaneous power is not zero in average value, besides at the aforementioned energy "sweet-spot". If the converter has no overlap period implemented, the "sweet-spot" gives an optimal converter modulation ratio (m) which provides a natural energy balance:

$$\hat{V}_g = \frac{4}{\pi} \frac{v_{dc}}{2} \rightarrow m = \frac{4}{\pi} \quad (5)$$

However, as the AC (and DC) voltage may deviates, operation at the "sweet-spot" cannot be guaranteed, therefore the implementation of an energy controller is mandatory. As the purpose of this study is to determine an active DC filter based on the regulation of the AAC internal energy, different solutions are explored.

Per-phase Stored Energy Control

The most common way to control converters stored energy is to consider each converter phases as three (in case of three phase systems) independent energy tanks. Thus, each phase is regulated independently corresponding to the control of the classical $W_{\Sigma j}$ variables [12],[13].

Per-phase Stored Energy Model

As mentioned above, the stored energy control is based on the power imbalance cancellation between the two converter sides. Thus, after few derivations, which are actually the same as the MMC, a generic stored energy model in average value (over the grid period T) is obtained:

$$\frac{1}{2}C_{tot} \left\langle \frac{d(v_{C_{tot}uj}^2 + v_{C_{tot}lj}^2)}{dt} \right\rangle_T = \left\langle \frac{dW_{\Sigma j}}{dt} \right\rangle_T = V_{dc} \langle i_{\Sigma j} \rangle_T - P_{acj} \quad (6)$$

with, P_{acj} the average value of the AC power flowing through the 'j' phase, C_{tot} the equivalent arm capacitor and $v_{C_{tot}(u,l)}$ the equivalent arm capacitor voltage.

In (6) the power balance appears as being dependent of the average value of i_{Σ} . However, due to changes in operating mode over the time, it can be shown that this current is actually composed of one component related to the Non-overlap mode (i_{Σ}^{ovl}), and uncontrollable, and another component, the overlap current (i_{Σ}^{ovl}), allowed by the Overlap mode existence. This latter, can be used to regulate the converter stored energy. As (6) considers the overall average value of i_{Σ} without distinction between controllable and uncontrollable part, it can be modified to highlight the system disturbances and output as in (7).

$$\left\langle \frac{dW_{\Sigma j}}{dt} \right\rangle_T = \underbrace{V_{dc} \langle i_{\Sigma j}^{ovl} \rangle_T}_{\text{Controller output}} + \underbrace{V_{dc} \langle i_{\Sigma j}^{ovl} \rangle_T - P_{acj}}_{\text{System disturbances}} \quad (7)$$

In Non-overlap mode, there is one non zero arm current which is equal to the grid current. Therefore, in this operating mode, the current i_{Σ} follows the rectified grid current. Thus is obtained:

$$\langle i_{\Sigma j}^{ovl} \rangle_T = \frac{\hat{I}_g}{\pi} \cos(\phi) \cos\left(\frac{\theta_{ovl}}{2}\right) \quad (8)$$

By expressing the DC voltage of the system disturbance in (7) according the AC voltage peak value ($V_{dc} = k_{acdc} \hat{V}_g$), the overall system disturbance can be expressed according to the AC power using (8). So:

$$\left\langle \frac{dW_{\Sigma j}}{dt} \right\rangle_T = V_{dc} \langle i_{\Sigma j}^{ovl} \rangle_T - P_{acj} \left(1 - \frac{2k_{acdc}}{\pi} \cos\left(\frac{\theta_{ovl}}{2}\right) \right) \quad (9)$$

The model given in (9), outputs the average value of i_{Σ}^{ovl} over the grid period, however, as the overlap period is shorter than the grid one, the magnitude of this current should be increased to obtain the right average value. This control is supposed to have slow dynamics compared to current dynamics and the measure of the energy well filtered, hence it can be considered that the overlap current is rather constant during the overlap period. Thus, it is assumed that:

$$\langle i_{\Sigma j}^{ovl} \rangle_T = \langle i_{\Sigma j}^{ovl} \rangle_{T_{ovl}} \left(\frac{\theta_{ovl}}{\pi} \right) \quad (10)$$

Therefore, the AAC per phase stored energy model is obtained:

$$\left\langle \frac{dW_{\Sigma j}}{dt} \right\rangle_T = V_{dc} \langle i_{\Sigma j}^{ovl} \rangle_{T_{ovl}} \left(\frac{\theta_{ovl}}{\pi} \right) - P_{acj} \left(1 - \frac{2k_{acdc}}{\pi} \cos \left(\frac{\theta_{ovl}}{2} \right) \right) \quad (11)$$

Control Design and Simulation Results

To determine the control structure associated to the AAC stored energy model, the principle of the model inversion is used. It is illustrated as follows:

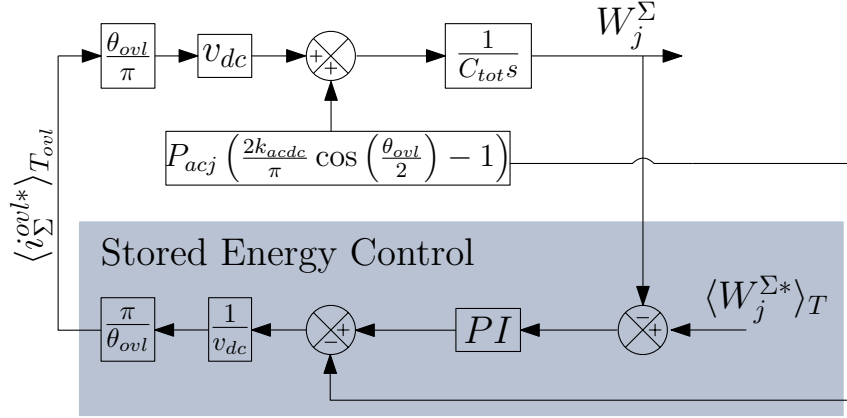


Fig. 2: AAC per phase stored energy model and control structure

For the sake of clarity, the filter on the energy measurement is not represented on Fig. 2, however, it is required to remove the AC components from the energy. Different types of filter can be used, but here sliding mean value filter is used for its ability to suppress almost totally the AC components. This controller has been implemented on the EO-AAC (i.e. overlap angle of $\pi/3$) which has the following characteristics:

Table I: Characteristics of the simulated EO-AAC

Parameter		Value
Rated power	S_n	1.04 GVA
DC voltage	V_{dc}	640 kV
AC voltage	U_g	500 kVLL-RMS
Grid frequency	F	50 Hz
SM per arm	N	330
SM capacitance	C_{SM}	6.15 mF

The number of SM depends on the overlap period length. A longer overlap period means a longer conduction period of each arm and therefore more positive voltage to generate. The SM capacitance is based on the stored energy requirement estimation, this study has shown that the EO-AAC needs approximately 15 kJ/MVA of embedded capacitive energy storage [10]. In the following dynamic simulation results are proposed to illustrate : the good performances of this control and its limitation regarding the DC current control. To do so, active power events are considered :

- at $t = 0.1$ s, a power ramp of 1 pu in 100 ms is applied
- at $t = 0.5$ s, a power reversal in 50 ms is imposed

As depicted on Fig. 3, the stored energy controller exhibits good dynamic performances even during a fast power reversal. However, as highlighted on Fig. 4, the DC current is not filtered even if the converter is in Extended Overlap configuration. In this case, the DC current ripple is around 0.159 pu (around 250 A for a 1 GW converter). This issue comes from the fact that with this control the DC current is not controlled.

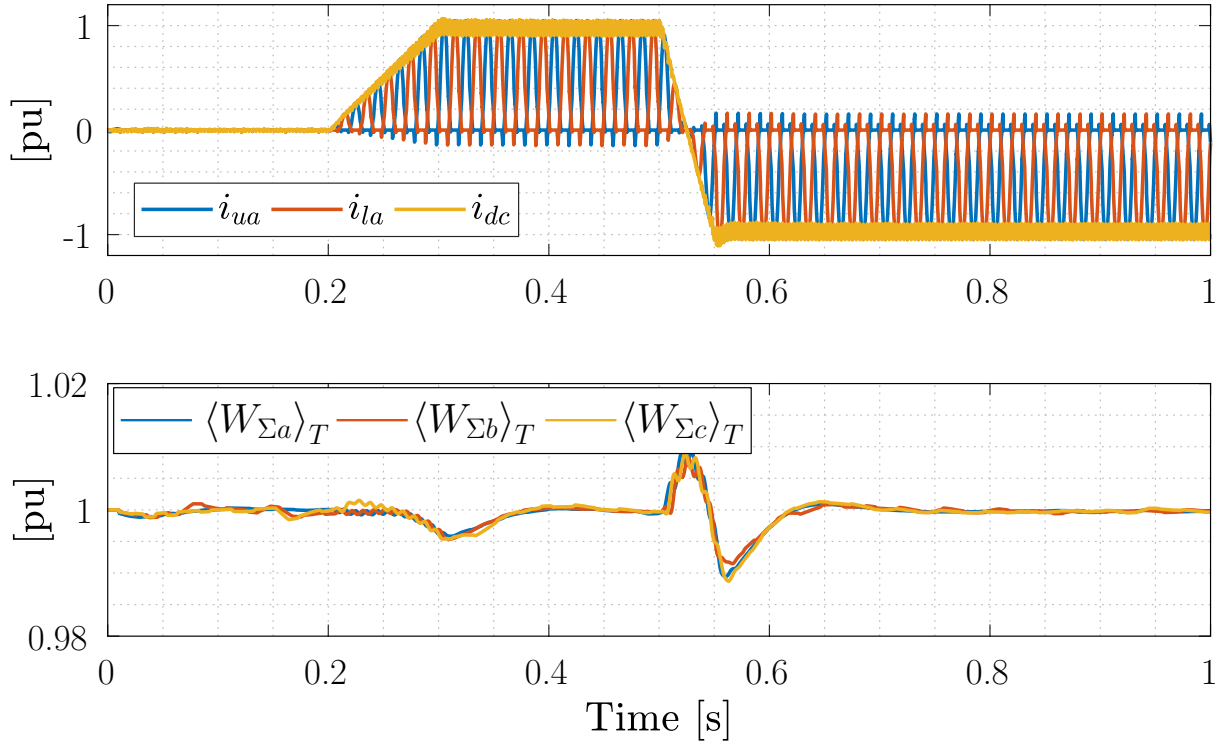


Fig. 3: Simulation results of the EO-AAC with per-phase stored energy control

The output of this control is the overlap current which influences the DC current waveform. The DC current is then a consequence of the overlap current control. However, to get the active DC filtering effect, the overlap current reference should be generated according to DC current waveform which is not possible here, if the control is formally deduced from the model. Therefore, the control proposed in [11] cannot be formally used without closed loop control on the DC current as DC inductors are used and because the per phase control does not provide the control of the DC current. Another stored energy control must be considered.

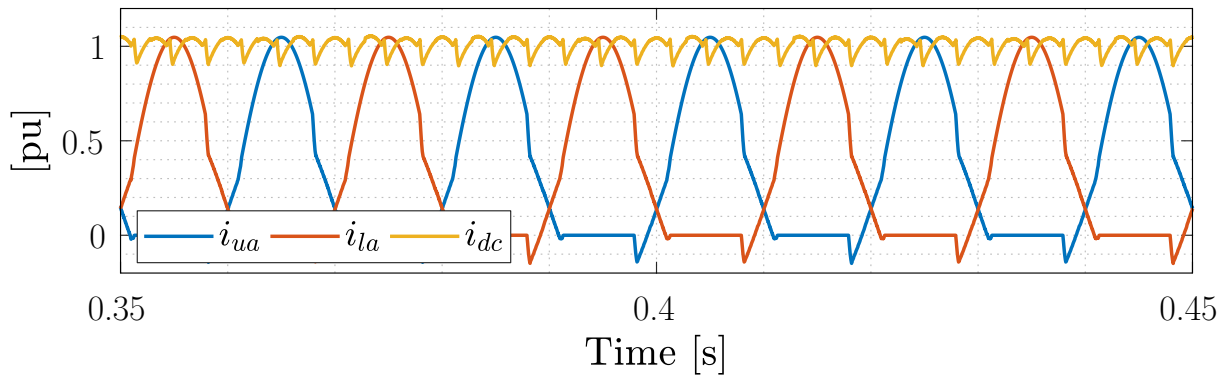


Fig. 4: Zoom on the arm and DC current waveforms in steady state

DC Current Ripple Removal with the Total Stored Energy Control

The previous control had as its output the overlap current which was rather constant during the overlap period. The control detailed in this section must output non-constant overlap current to oppose the DC current ripple while keeping the converter internal around its nominal value. These features can be achieved by using the total stored energy control.

Total Stored Energy Model

Achieving the control of the stored energy phase by phase led to the regulation of the average values of each i_{Σ} . However, by circuit analysis, it can be shown that:

$$i_{dc} = i_{\Sigma a} + i_{\Sigma b} + i_{\Sigma c} \quad (12)$$

Thus, considering the whole converter stored energy (W_{tot}) defined by:

$$W_{tot} = W_{\Sigma a} + W_{\Sigma b} + W_{\Sigma c} \quad (13)$$

leads to a model where the overall DC (or AC) power can be regulated thanks to the total stored energy control. Until now, the per-phase stored energy control regulated the average value of i_{Σ} , with W_{tot} it is now possible to regulate explicitly the DC current. The model is given as follows:

$$\frac{dW_{tot}}{dt} = v_{dc}i_{dc} - p_{ac} \quad (14)$$

Stored energy controllers are essentially achieved in average value to suppress every AC components in the measurement, mostly for simplification of the control. Using the total stored energy control gives the advantage of not having to use filter on the energy measurement. Indeed, as W_{tot} is defined as the sum of the three W_{Σ} , in normal condition, all the AC components in W_{Σ} constitute a three phase energy system which sums to zero. Therefore, this control can be achieved in instantaneous value giving access to the instantaneous value of i_{dc} and by extension its waveform. However, since there is only one phase in overlap mode (so only one overlap current controllable) the equation (12) should be used to obtain an overlap current reference:

$$i_{\Sigma j}^{ovl*} = i_{dc}^* - i_{\Sigma j_x} - i_{\Sigma j_y} \quad (15)$$

with, the variables noted x^* corresponding to references and the sigma currents $i_{\Sigma j(x,y)}$ of the two other phases in Non-overlap mode. Thus, using (15) allows to compensate the harmonics rejected by the two phases in Non-overlap mode into the DC link.

Theoretical Analysis of the Proposal

The previous subsection has detailed the total stored energy model and the way to generate overlap current references with active DC filtering purpose. This subsection, by the mean of a static analysis, aims to validate the ability of this control to:

1. remove the DC current ripple and,
2. maintain the stored energy stable

Fig. 5 gives the comparison between the per-phase stored energy control and the total stored energy with active DC filtering control strategy on the DC current waveform. Thanks to the use of the total stored energy controller and (15) the DC current is well filtered without using DC inductors.

Regarding the stored energy, a calculation of the overlap current average values over the overlap period can be achieved to verify that they are the same with the per-phase and total stored energy controls. To do so, a static analysis is required. Considering the derivative term of (11) equals to zero, the average value of $i_{\Sigma a}^{ovl}$ over the overlap period can be obtained:

$$\langle i_{\Sigma a}^{ovl} \rangle_{T_{ovl}} = \frac{P_{acj}}{V_{dc}} \left(1 - \frac{2k_{acdc}}{\pi} \cos \left(\frac{\theta_{ovl}}{2} \right) \right) \left(\frac{\pi}{\theta_{ovl}} \right) \quad (16)$$

Then, in the case of the total stored energy, by using (15) and considering the DC current constant and the average values over the overlap period of the sigma currents gives:

$$\langle i_{\Sigma a_j}^{ovl} \rangle_{T_{ovl}} = i_{dc} - \frac{1}{T_{ovl}} \int_{T-T_{ovl}/2}^{T+T_{ovl}/2} i_{\Sigma j_x}(t) + i_{\Sigma j_y}(t) dt = i_{dc} - \hat{I}_g \sin \left(\frac{\pi}{3} \right) 2 \sin \left(\frac{\theta_{ovl}}{2} \right) \quad (17)$$

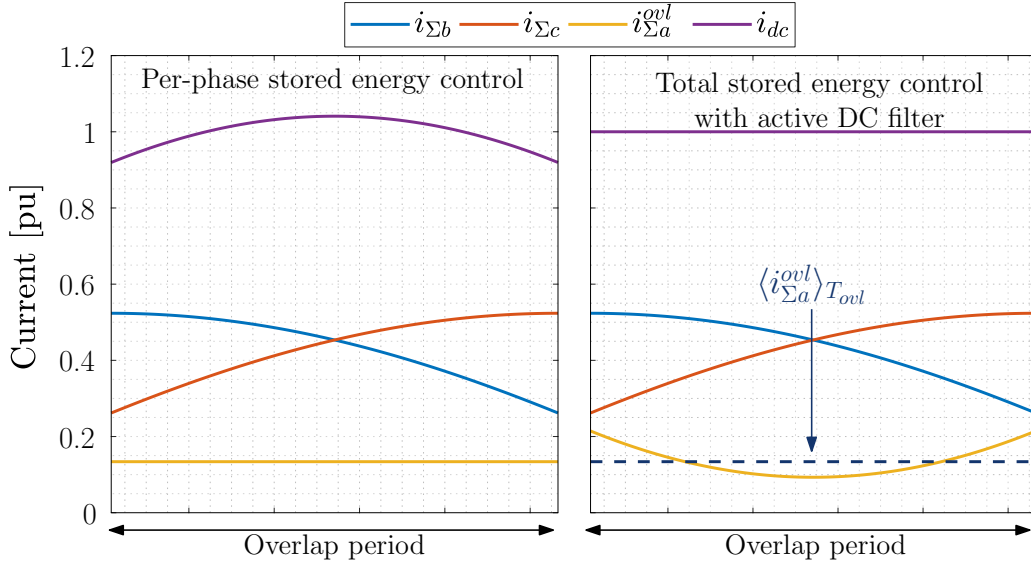


Fig. 5: Theoretical waveforms of i_{dc} and $i_{\Sigma a}^{ovl}$ with both stored energy controllers

Assuming the active power equals to 1 pu, the overlap current magnitude with the per-phase stored energy controller is equal to 0.133 pu. In the case of the total stored energy control, the average value of the overlap current over the overlap period is also equals to 0.133 pu as it is depicted on Fig. 5. Thus, by the mean of an analytical study, it has been shown that the proposal allows at the same the active filtering of the DC current and maintaining the energy balance of each phase.

Control Design and Simulation Results

In the same way as the per phase stored energy controller, the control design is based on a strict inversion of the total stored energy model.

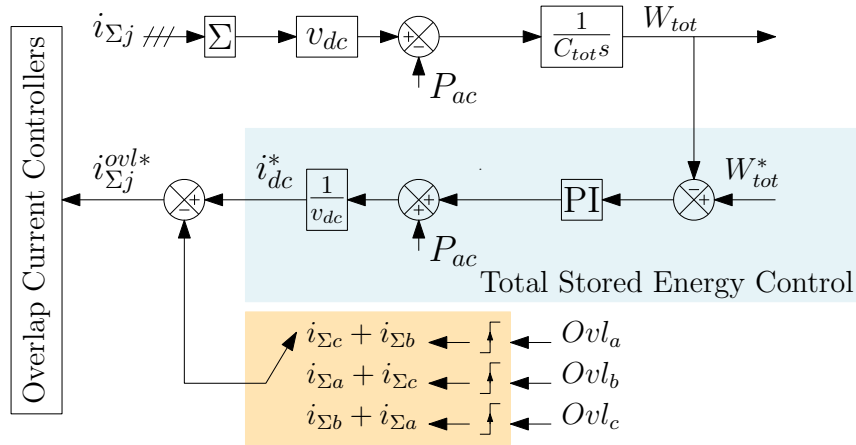


Fig. 6: EO-AAC total stored energy model and control structure

The upper part of Fig. 6 shows the total stored energy model and its control structure. The most important part of this figure is the yellow frame where the equation (15) is illustrated. Indeed, the right reference have to be sent to the active overlap current controller (i.e. the one with its phase leg in overlap mode). Thus, a boolean variable is used to detect when a phase is in Overlap mode (Ovl_j) and therefore to know which $i_{\Sigma j}$ must be subtracted to i_{dc}^* .

To validate the dynamic performances of the control, the same power events as the previous control are considered:

- at $t = 0.1$ s, a power ramp of 1 pu in 100 ms is applied
- at $t = 0.5$ s, a power reversal in 50 ms is imposed

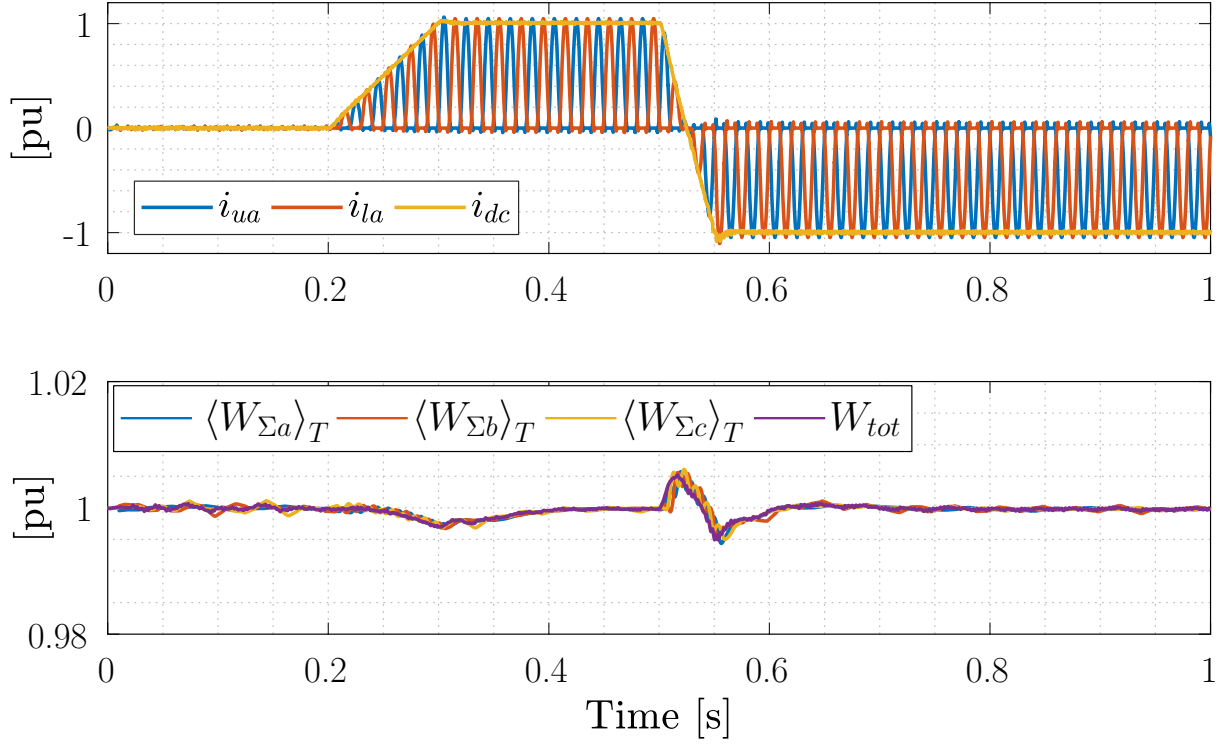


Fig. 7: Simulation results of the EO-AAC with total stored energy control

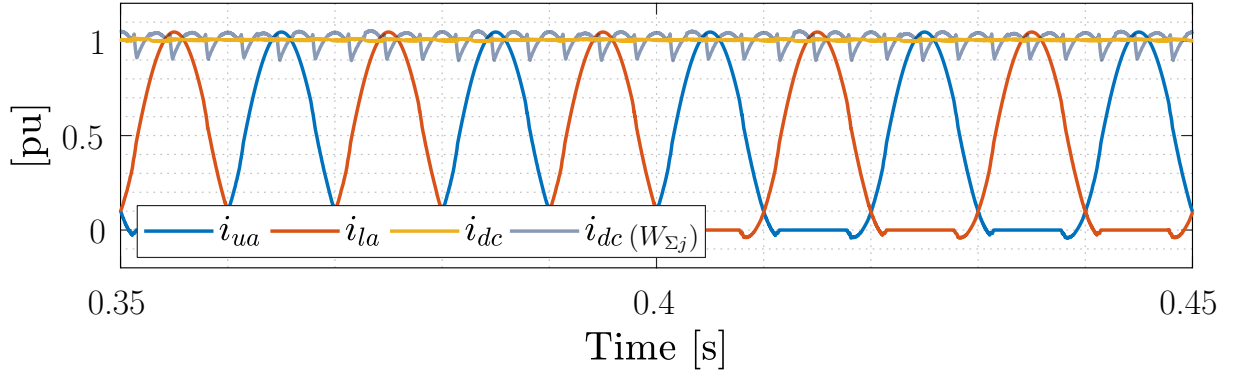


Fig. 8: Zoom on the arm and DC current in steady state

Simulation results are presented on Fig. 7. The dynamic performances of the converter with active DC filtering are comparable to that of the AAC with per-phase stored energy control. In this case, the dynamics are a little better since the control is made in instantaneous value, therefore there is no phase delay caused by the measurement filters. The overall stored energy in the converter (W_{tot}) is well controlled around its nominal value and evenly shared between the three phases. This simulation confirms the static analysis detailed in the previous subsection.

In addition to the acceptable dynamic performances, it can be seen that the DC current is no more highly rippled as it was with the previous control. A comparison between the DC currents with both controls is provided by Fig. 8. Thus, it can be seen that the arm current waveforms have been modified during the overlap period in order to obtain a smooth DC current. By using this control, the DC current ripple drops to 0.023 pu in steady-state. The grey line represents the DC current obtained with per-phase energy control.

Conclusion

This paper has presented an active DC filtering control strategy for the EO-AAC based on its internal stored energy control. Two stored energy control strategies have been compared showing the limitation of the classical option (per-phase control) which does not explicitly control the DC current. Thereby, another stored energy control where the DC current clearly appears as an output has been detailed : the total stored energy control. Using this control allows to modify the arm current waveform of the phase leg in overlap mode to obtain smooth DC current. Finally, based on a static analysis and a dynamic simulation, this control has shown its ability to, at the same time, keep the converter energy stable and provide the active DC filtering effect.

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