A Bidirectional Three-port Current-fed LC Parallel Resonant Converter

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***Abstract*-This paper presents a Three-port current-source bidirectional resonant converter. The converter achieves zero-voltage switching (ZVS) due to the presence of a parallel resonant tank circuit, a combination between parallel inductors and capacitors. Moreover, it has reduced output current ripple and reduced power losses in the transistors if compared with a voltage source topology. The conversion occurs with self-oscillating switching technique or with forced switching in a pre-determined frequency range without losing the ZVS conditions. Due to the high frequency transformer that allows a high voltage ratio between the ports, the converter applications includes different energy storage systems that require bidirectional power flow capability, such as hybrid vehicles. A design procedure to select the converter parameters and simulation results are presented to validate the converter operation principle.**

I. INTRODUCTION

Nowadays, the demand for high performance isolated DC/DC converters in multiple-port applications has been increased due to the existence of different energy sources and loads present in hybrid systems.

In parallel, in order to increase converter's power density, resonant converters have become an interesting solution. Due to its soft switching strategies as zero-voltage switching (ZVS) and zero-current switching (ZCS), the frequency can be increased without generating higher power losses in the transistors. Also, due to the sinusoidal current or sinusoidal voltage characteristics, the transformer can benefit from lower power losses if compared to other converters.

Three-port resonant converters using a series LC or a series LLC circuit tanks have been presented in [1], [2]. A current-fed resonant converter without bidirectional capability is presented in [3]. Parallel resonance is usually applied to push-pull converter stages, as in [4], where a push-pull LC parallel converter is operated under soft-switching condition and does not require bulk capacitors.

In [5], a bidirectional three-port LC parallel converter is discussed for fuel-cell hybrid system applications. The converter structure is similar to the converter presented in this text; however ZVS was not achieved because of the control methodology implemented. In [6], a push-pull converter uses a series-parallel resonance to operate under zero-current switching condition.

The converter presented in this paper has reduced current ripple, reduced conduction power loss and does not need bulk capacitors. In addition, to reduce the total number of magnetic components and the current ripple on the DC sides, different coupling factors between the three input inductors are investigated in the converter design.

The Three-port bidirectional current-source parallel resonant converter is shown in Fig. 1. The converter is a current-fed topology and in this application, instead of large capacitances, as required in common voltage-source converters, the inductor in series with the voltage source is large enough to smooth the current. The converter study is divided into 4 sections:

The section II presents the converter analysis and operation modes. In sections III and IV, the converter design is presented by taking in consideration different coupling factors between the three input series connected inductors. The converter behavior and characteristics are verified with simulations and the results are presented in section V and VI.

II. THE CONVERTER OPERATION ANALYSIS

In the circuit presented in Fig.1, three-voltage sources are connected in series with individual inductors to reduce the current ripple. Due to the presence of these inductors, the input current ripple is low and the current can be considered like almost constant with a small variation around its average value. The LC circuits connected in parallel to the transformer terminals are used in the resonance and a RC load is connected at the second DC side.

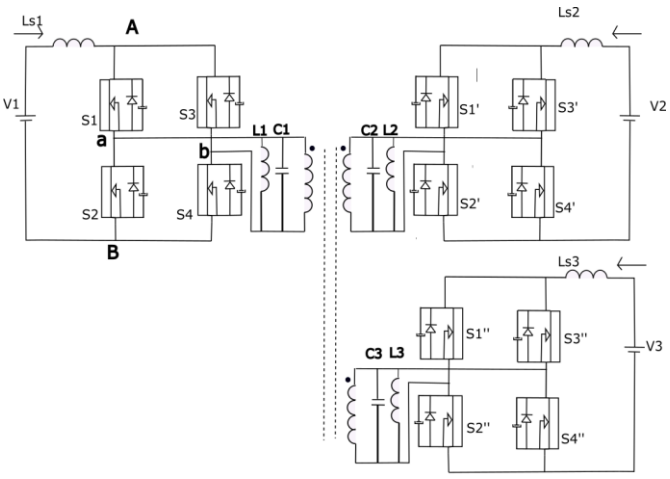

Fig. 1. The Three-port parallel resonant current-fed converter.

Full-bridges are required to keep the current continuity during the switching transitions and to allow the reverse power flow operation required in the bidirectional functionality.

The transistors are switched by pairs alternatively in the diagonal direction and an overlap is used to keep uninterrupted the current flow. When the three full-bridges are simultaneously switched at a same frequency, a square current waveform is injected by each port to the three windings of the high-frequency transformer connected in parallel with the LC tank circuits.

A simplified circuit is represented in Fig. 2. In this figure the full-bridges are replaced by current sources and the transformer is considered with ideal characteristics, such as, infinite magnetizing inductance and very small leakage inductances. The passive elements are all transferred to the primary side of the transformer and an equivalent parallel inductance and capacitance are represented.

A second representation is interested in order to consider the input inductance values in the analysis. The schematic from Fig. 3 considers the voltage sources connected in series with the input inductances and the DC voltage redressed between the points "a" and "b", Vab, in Fig. 1. An equivalent AC-load from the second port is also represented and it could be connected to any of the ports. In this schematic, the MOSFET's on-resistance are considered small without generating significant voltage drop. The total current flowing to the point A, also represented in Fig. 1 is:

$$i_{ab} = i_1 + i_3 + i_2 = i_C + i_L + i_{Lm} \quad (1)$$

$$i_{Lm} = i_{T1} + i_{T3} + i_{T2} \approx 0, L_m \to \infty \quad (2)$$

The sum of the currents flowing into the transformer windings is considered as zero, as can be seen in (1). The voltage drop on the series inductances is calculated as a function of the three current sources on the DC sides.

$$V_1 = L_{s1}\frac{di_1}{dt} + u;\ V_3 = L_{s3}\frac{di_3}{dt} + u;\ V_2 = -L_{s2}\frac{di_2}{dt} + u \quad (3)$$

Combining (1) and (3), the resonant voltage is obtained from:

$$C\frac{du^2}{dt^2} + \frac{u}{L} + u\left(\frac{1}{Ls_1} + \frac{1}{Ls_2} + \frac{1}{Ls_3}\right) - \left(\frac{V_1}{Ls_1} + \frac{V_2}{Ls_2} + \frac{V_3}{Ls_3}\right) = 0 \quad (4)$$

The solution of the differential equation depends on the initial conditions: The transistors are switched during the zero-voltage crossing, while the current still keeps its same signal just before the transition, so the current in the parallel inductor achieves the maximum value when the voltage u (t) passes by zero and the capacitor is completely discharged. The equations for the voltage and current in the parallel resonant cell are presented in (5) and (6).

$$u(t) = I_{Lpeak} L W_r \sin(Wt) + K[1 - \cos(Wt)] \quad (5)$$

$$i_L(t) = -\frac{K}{L W_r}\sin(W_r t) - I_{Lpeak}\cos(W_r t) + \frac{Kt}{L} \quad (6)$$

$$W_r = \sqrt{\frac{L+L_s}{L_s L C}};\quad K = \left(\frac{V_1}{L_{s1}} + \frac{V_2}{L_{s2}} + \frac{V_3}{L_{s3}}\right)\frac{L L_s}{(L+L_s)} \quad (7)$$

$$\frac{1}{L_s} = \left(\frac{1}{L_{s1}} + \frac{1}{L_{s2}} + \frac{1}{L_{s3}}\right) \quad (8)$$

The resultant resonant frequency of the three-port converter depends on the combination between the parallel elements, but also on the series connected inductors. In the case that the value of the combined DC side series inductors in (8) is large if compared with the inductance resultant from the parallel arrangement, the resonant frequency is mainly influenced by the parallel LC tank circuit, as can be seen in (9):

$$F_r = \frac{1}{2\pi}\sqrt{\frac{L+L_s}{L_s L C}} \cong \frac{1}{2\pi}\sqrt{\frac{1}{L C}} \quad (9)$$

At steady state, the gain between the voltage sources and the load is unitary. In reality will be less than one due to the voltage drop on the MOSFET on-resistances and parasitic elements.

From the equivalent circuit in Fig. 3, the voltage-time balance in the DC side inductor can be used to determine the resonant peak voltage, in the transformer primary side. The same calculation can be made for Ls2 or Ls3. The voltage peak can be determined using the equivalence between the voltage-time balance principle over Ls1 in half of the period and the DC voltage source V1:

$$V_1 - \frac{1}{\pi}\int_0^{\pi} u(t)\, d\omega t = 0 \ \Rightarrow\ V_1 = \frac{1}{\pi}\int_0^{\pi} u(t)\, d\omega t \quad (10)$$

$$\frac{1}{\pi}\int_0^{\pi} u(t)\, d\omega t = \frac{1}{\pi}\left[2V_{peak} + K\pi\right] = V_1 \quad V_{peak} = \frac{\pi(V_1+K)}{2} \quad (11)$$

If the DC side input inductances, Ls1, Ls2 and Ls3 are very large when compared to the parallel inductance L, the voltage peak is minimized and is determined in (12):

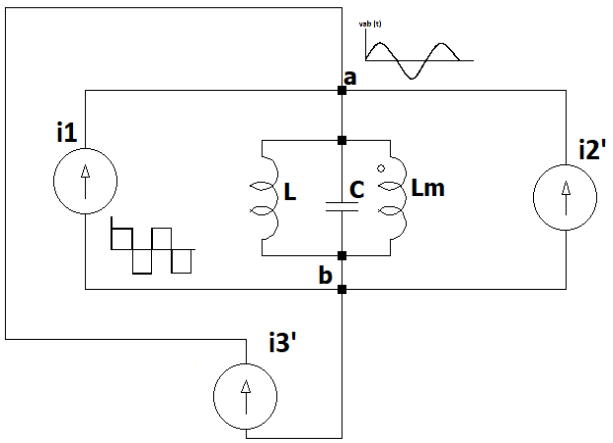

Fig. 2. The equivalent circuit with large input inductances. 1/L = (1/L1 + 1/L2 + 1/L3); C = C1 + C2 + C3.

$$V_{peak} = \frac{\pi}{2}\left[V_1 + \left(\frac{V_1}{L_{s1}} + \frac{V_2}{L_{s2}} + \frac{V_3}{L_{s3}}\right)L\right] \cong \frac{V_1\,\pi}{2} \qquad (12)$$

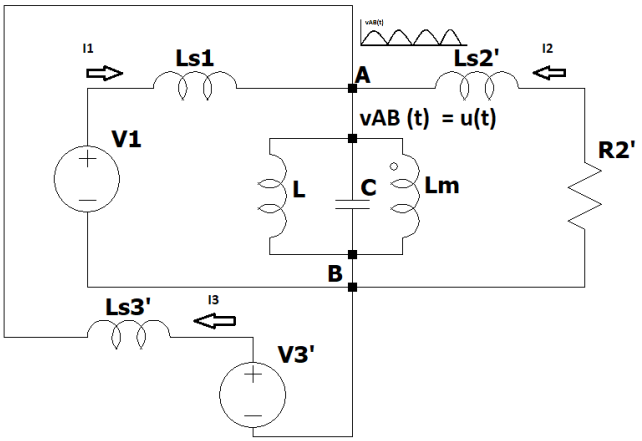

Fig. 3. The equivalent circuit for analysis considering the input inductances values. 1/L = (1/L1 + 1/L2 + 1/L3); C = C1 + C2 + C3.

1. *The ZVS mode*

The Three-port parallel resonant converter can be operated under ZVS conditions when the switching frequency is equal or smaller than the resonant frequency. At the resonant frequency, the parallel equivalent impedance is increased and the time interval during the switching transition is minimized. At this condition the circulating energy is reduced because the minimum power loss is produced in the parallel resonant elements to obtain the soft switching mode.

At frequencies smaller than the resonant frequency, the ZVS is still obtained, but the power loss is increased due to the circulating current during the switching transition times. In addition, as can be verified in (10), smaller the switching frequency, higher will be the voltage peak applied in the transistors.

The converter operation of a single full-bridge is illustrated in Fig. 4. The parasitic capacitors of the MOSFET are also indicated because they also have an impact in the resonance, being in parallel with the capacitance C1 in case that parasitic inductances are minimized.

During the first half-cycle, the switches S1 and S4 conduct. The current and the voltage are positive; when the voltage cross zero, the opposite switches (S2 and S3) can be turned-on at zero-voltage switching. Only after an overlap time, the transistors S1 and S4 are turned-off to prevent an open circuit. The reactive energy oscillates in the resonating cell and then is returned to the voltage sources, all during a half-cycle allowing the switching when the capacitors are fully discharged.

The current and the voltage waveforms are illustrated in Fig. 5 for a single full-bridge. During the time interval t1, the transistors S1 and S4 conduct while S2 and S3 are OFF. The input current i1 and the voltage Vab are positive, while the currents in the capacitors Cs2 and Cs3 are decreasing due to the resonant circulating energy. During t2, while S1 and S4 are still ON, the transistors S2 and S3 can be turned-on under ZVS condition, because Cs2 and Cs3 are fully discharged and their currents become zero again.

At interval t3, S1 and S4 are turned-off only after S2 and S3 had been turned-on to prevent an open-circuit. The voltage Vab and the current i1 are negatives. The capacitors Cs1 and Cs4 are being charged and discharged during this interval. When they are fully discharged, during t4, the switches S2 and S3 are turned-off after the switches S1 and S4 had been turned-on. The capacitances are discharged and the parallel inductor conducts the maximum current while the voltage is zero.

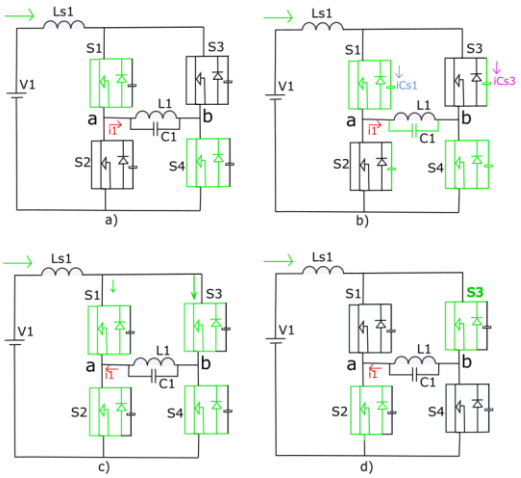

Fig. 4. The converter operation modes for a single full-bridge. a) S1 and S4 are ON and Vab =0. b) The capacitors Cs2, Cs3 and C1 are charged and discharged. The remaining energy goes back to V1. c) While Vab =0, S2 and S3 are turned-on under ZVS. The remaining energy is stored in L1, while the current is distributed between both arms. d) S1 and S4 are turned-OFF under ZVS. Cs1 and Cs4 are progressively charged while Vab increases. The circulating energy is now absorbed from V1.

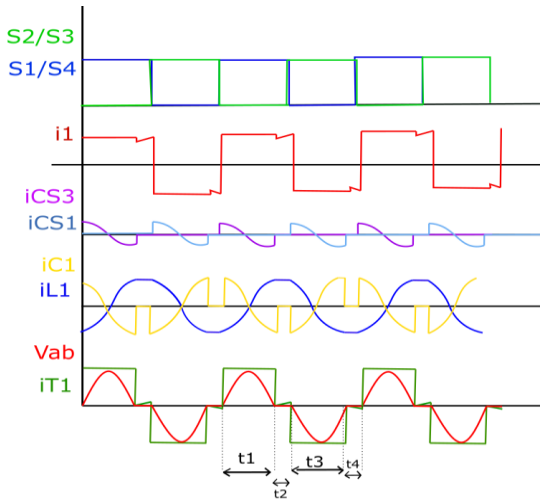

Fig. 5. The converter operation modes for a single full-bridge.

This behavior is verified in the other full-bridge sides since the same voltage u (t) is imposed by the parallel circuit tank in theirs terminals due to the transformer characteristics, which must have minimized leakage inductances and a high magnetizing inductance.

III. THE DC SIDE INDUCTORS

One of the characteristics in the three-port current-fed resonant converter is the possibility of implementing different arrangements with the DC side inductors. Their values are mainly determined by the average current in each of the ports and we can see from (11) that it plays an important role in the resonant voltage peak.

In order to obtain a good converter's performance, MOSFETs with low on-resistance should be used; and since their resistances are directly associated with their nominal voltages, an effort should be done to keep a minimized voltage peak during the converter operation.

Increase the DC side inductances it is one of the solutions to achieve this objective, but will have an impact on the converter volume. A second option will consist in the use of a single magnetic core. Using a coupling factor between the three DC side inductors will bring some advantages to the configuration, especially in the case that the DC side inductances are smaller than the parallel ones.

The first advantage is the reduction of the total number of magnetic elements; and in addition, the reduction of the peak voltage, allowing the use of a MOSFET with smaller conduction on-resistance without needing to actually increasing the DC inductor values.

The common coupling factor kc between the three series connected inductances allow to write the following equations:

$$V_1\text{-}u = L_{s1}\frac{di_1}{dt} - k_c L_{s2}\frac{di_2}{dt} - k_c L_{s3}\frac{di_3}{dt} \quad (12)$$

$$V_2\text{-}u = L_{s2}\frac{di_2}{dt} - k_c L_{s1}\frac{di_1}{dt} - k_c L_{s3}\frac{di_3}{dt} \quad (13)$$

$$V_3 - u = L_{s3}\frac{di_3}{dt} - k_c L_{s1}\frac{di_1}{dt} - k_c L_{s2}\frac{di_2}{dt} \quad (14)$$

In order to simplify, the DC sides inductances remained to the primary side in Fig. 3 are considering with the same value, Ls1, and the solution of the resonant voltage is then obtained from (15). The equivalent voltage and the resonant frequency are presented in (16) and (17).

$$C\frac{du^2}{dt^2} + \frac{u}{L} + \frac{3u}{L_{s1}(1\text{-}2k_c)} - \frac{V_1+V_2+V_3}{L_{s1}(1\text{-}2k_c)} = 0 \quad (15)$$

$$u(t) = I_{Lpeak} L W_{r_2} \sin(Wt) + K_2[1 - \cos(Wt)] \quad (16)$$

$$W_{r_2} = \sqrt{\frac{3L+L_{s1}(1\text{-}2k_c)}{(1\text{-}2k_c)L_{s1}LC}}; \quad K_2 = \left(\frac{V_1}{L_{s1}} + \frac{V_2}{L_{s2}} + \frac{V_3}{L_{s3}}\right)\frac{L L_{s1}(1\text{-}2k_c)}{[L+L_{s1}(1\text{-}2k_c)]} \quad (17)$$

The voltage-time principle balance when applied over Ls1 during half of the period corresponds to the DC side voltage V1. The peak voltage is now calculated as:

$$V_{peak} = \frac{\pi V_1}{2} + \left(\frac{V_1}{L_{s1}} + \frac{V_2}{L_{s2}} + \frac{V_3}{L_{s3}}\right)\frac{L L_{s1}(1\text{-}2k_c)}{2[L+L_{s1}(1\text{-}2k_c)]} \quad (18)$$

The coupling factor kc represents a symmetrical contribution from two inductances to the third one, and is not higher than one. When this factor is small, the voltage peak in (18) becomes the result presented in (11). Fig. 6 presents an example to show the impact in the MOSFET's peak voltage for different ratios between the parallel and the series DC side inductances. We see that, even when the series inductance is smaller than the parallel inductance, is still possible to find a compromise and keep a security margin for the equivalent voltage applied in the MOSFET during its turned-off stage.

IV. THE CONVERTER DESIGN

The converter design should start at first with the selection of the desirable switching frequency and the nominal operating voltage. Second, after selecting the resonant frequency, for different quality factors between the parallel inductance and the load, the parallel inductance can be pre-determined. For the parallel resonant converter is interesting to obtain the parallel impedance higher than the load in order to obtain a good quality factor to the circuit.

Then, using different ratios between the parallel and the DC series side inductance the last one is evaluated. A compromise should be done in order to obtain a security margin for the mosfet nominal voltage and a reduced volume. A minimum value must be ensured in order to keep low the current ripple.

Because of the sinusoidal voltage applied on the transistors, the power transistor selection will have an important influence on the converter performance, since the MOSFETs for high voltage applications have an increased conduction resistance. This resistance should be as low as possible, not only to reduce the conduction power losses, but also to maintain the voltage gain close to one.

The following table shows the converter design for a typical application example.

TABLE I
CONVERTER SPECIFICATION FOR AN APPLICATION EXAMPLE:

Appearance			
	Port 1	Port 2	Port 3
Nom.Volt (V)	480	480	20
N	24	24	1
Power (W)	3.5 kW	3.5 kW	3.5 kW
Res.Freq (kHz)	200	200	200

2. The converter control

The converter control can be implemented in two different ways. The first one consists in the self-oscillating switching technique presented in [4] for a current-fed push-pull converter. The technique consists in to measure the voltage on

the transformer terminals and detect the zero-crossing to ensure that the converter will be switched at ZVS by tracking its natural resonant frequency. This technique has the advantage that the power losses are reduced because the converter is switched with the minimum required overlap transition time. In addition, because of the self-tracking, the variation on the capacitor and inductor values are naturally considered. However, the control is not robust and load variations can provoke some instability.

The second technique is to force the converter operation in a frequency smaller than the resonant frequency; in this frequency range the current will be delayed from the voltage because the equivalent impedance from the parallel inductance is smaller than the parallel capacitance, allowing the complete discharge of the capacitors before the switching transition. However, smaller the switching frequency, higher will be the voltage peak and the overlap transition time, increasing also the circulating energy and the power losses.

In order to validate the converter operation, the control proposed here is a combination of both techniques and is similar to the control technique presented in [4] for the push-pull converter. It consists in to measure the voltage at the transformer terminals to detect its zero-crossing, while keeping a forced switching signal at a pre-determined frequency, as can be verified in Fig. 7.

V. SIMULATION RESULTS

Using the design requirements from Table I and the design steps from section IV, the converter presented in this section considers the characteristics from Table II. Parasitic capacitances in the MOSFETs and also a small leakage inductance in the transformer primary side were introduced. The input DC side inductances are reduced if compared to the parallel elements and the designed resonant frequency is 200 kHz, however, due to the parasitic elements, this frequency was modified, but still kept closed of the desirable value.

As represented in Fig. 1 and according to Table 1, 480V is connected in the voltage source V1 and 20V in the voltage source V3. A MOSFET with a nominal voltage of 1200V is used in this simulation and a margin security of 350V is obtained with the design presented in Table 2. A coupling factor it is considered between the DC side inductances.

TABLE II
CONVERTER DESIGN SPECIFICATION:

Appearance			
	Port 1	Port 2	Port 3
Nom.Volt (V)	480	480	20
N	24	24	1
Lsx	42 uH	42 uH	73 nH
Cx	4nF	4nF	2.3 uF
Lx	165 uH	165 uH	290 nH

In Fig. 8, the AC current in each winding of the converter is presented. The voltage source V1 connected to the first port provides 7 kW to the loads connected at the second and the third ports. In Fig. 9, the currents in the transformer terminals after the resonant cells are shown. Note that the transistors are switched when the sinusoidal voltage in the transformer winding pass by zero. The current waveforms are very similar to the expected square current waveforms. The current ripple obtained at steady-state in the DC side can be seen in Fig. 10.

VI. CONCLUSION

In this paper a modified Three-port Bidirectional Current-fed resonant converter is presented. The converter has reduced current ripple and operates with zero-voltage switching due to the presence of a parallel tank circuit connected with the transformer windings. The coupling factor between the three DC series inductances is also studied in order to reduce the number of magnetic components and the converter conduction power losses by making possible the use of transistors with a smaller on-resistance.

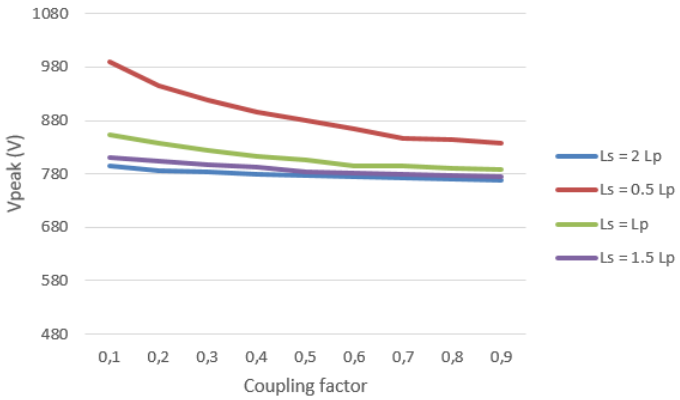

Fig. 6. Peak voltage under the power transistors for different DC sides inductances values and coupling factor.

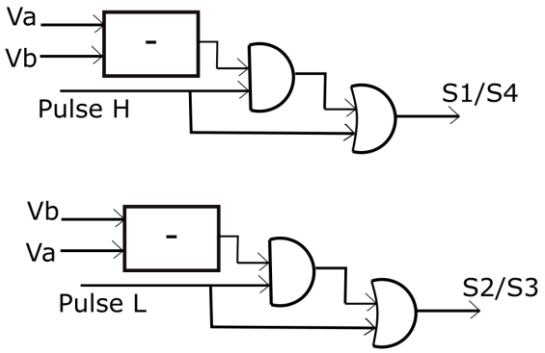

Fig.7. Command generation for the three-port resonant converter.

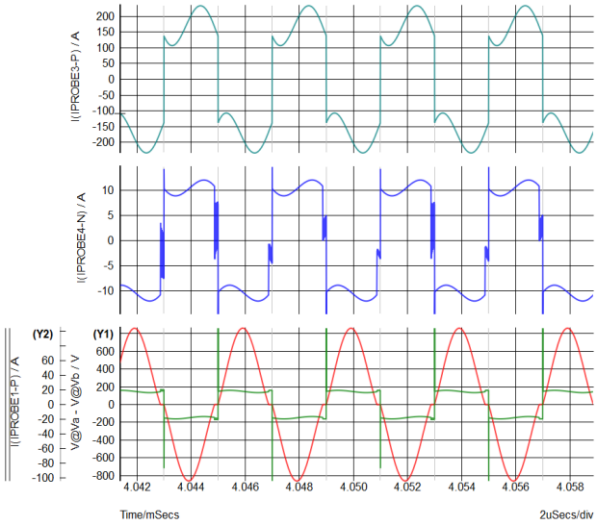

Fig.8. Converter operation while Port 1 supplies 7 kW for ports 2 and 3. a)Current in the primary side, i1 b) Current in the secondary side, i2 c)Current in the third side, i3 and voltage Vab.

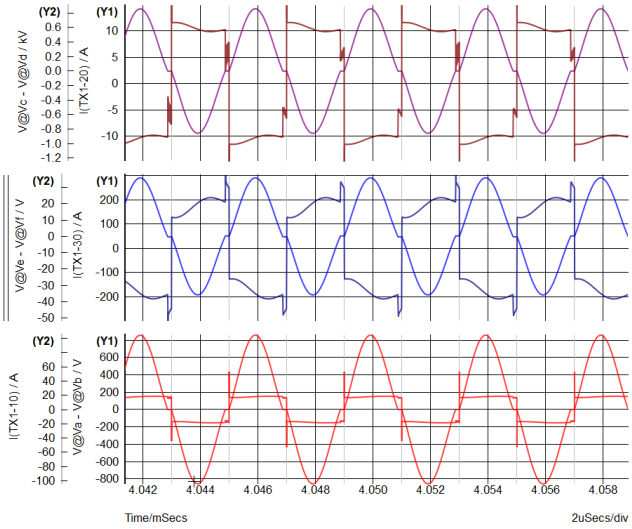

Fig.9. Converter operation while Port 1 supplies 7 kW for ports 2 and 3. a)Current in the transformer secondary side, iT2 and Vcd. b) current in the transformer third side, iT3 and Vef. c) Current in the primary side, iT1 and Vab.

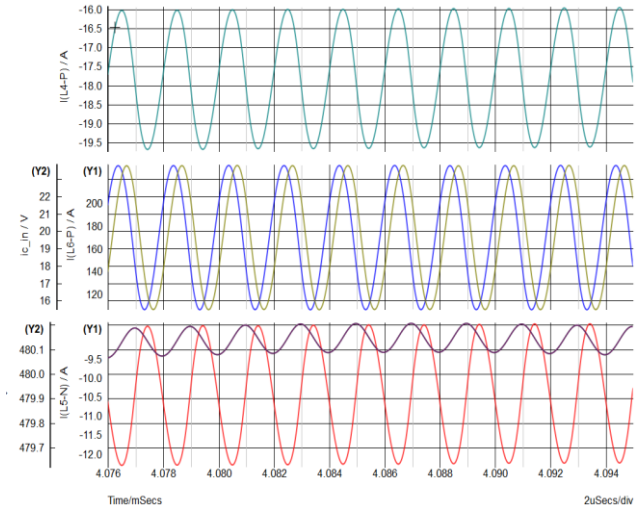

Fig.10. Converter operation while Port 1 supplies 7 kW for ports 2 and 3. a) DC current I1. b) DC current I3 and output voltage V3. c) DC current I2 and output voltage V2.

REFERENCES

[1] Y. Kim, D. Dujié, and P. Barrade, "Multiport Resonant DC-DC Converter," *IECON2015-Yokohama*, IEEE, pp. 3839-3844, November 2015.

[2] H. Krishnaswami, and N. Mohan. "Constant Switching Frequency Series Resonant Three-port Bi-directional DC-DC Converter ," IEEE, pp. 1640-1645, November 2008.

[3] R. Nareshkumar, M. RAmteke, "Closed-loop control of current-fed full-cbridge parallel resonant soft-switched dc-dc boost converter for PV applications ," in *IEEE*, 2016 pp. 2462-2467.

[4] A. Namadmalan, "Bidirectional Current-fed resonant inverter for contactless energy transfer systems," in *IEEE Transactions on Industrial Electronics, vol.62, N°1, January 2015.* pp. 238-248.

[5] H. Krishnaswami, and N. Mohan. "A Current-fed Three-port bi-directional DC-DC Converter ," IEEE, pp. 523-526, November 2007.

[6] R. S. K. Moorthy, and A. K. Rathore. "Zero Current Switching Current-fed parallel resonant push-pull (CFPRPP) Converter ,"in International Power Electronics Conference IEEE, pp. 3616-3623, 2014.

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