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## P-type SiC layers formed by VLS induced selective epitaxial growth

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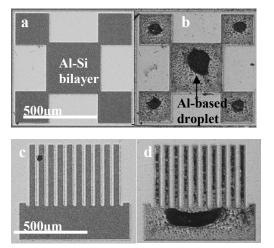
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Unipolar SiC devices like Schottky diodes, MESFET and JFET are already or will be soon commercialized. Different universities or industrial research teams have published a non-negligible number of bipolar device demonstrators in SiC. Nevertheless large efforts were mainly targeted in increasing the breakdown voltage. Results on 19.5kV bipolar diodes were published [1]. In spite of that, the development of SiC bipolar devices is slowed down due to the low currents which are obtained in forward polarization. This is due firstly to the material quality which limits the device area and secondly to the high resistances of the SiC p-type layers and the ohmic contacts on these layers. Diminishing the SiC p-type layers resistance is difficult by classical process due to the solubility limit of dopants during the CVD epitaxy [2] or the material degradation by ion implantation at high doses. Partial material recovery and dopant activation are obtained after high temperature post-implantation annealing  $(1700 - 1800^{\circ}C)$ . In this paper we present SiC p-type material selectively grown at relatively low temperature process by Vapour-Liquid-Solid (VLS).

The unique configuration of the VLS process, where only carbon is brought by the gas phase, allows to grow SiC only where the seed is covered by the Al-Si melt. Using the same procedure as in reference [3], a n-type 8° off-axis 4H-SiC substrate is covered by controlled thickness Al-Si bilayer stacking, 1 $\mu$ m of Si by CVD at 1000°C under silane followed by 2 $\mu$ m of Al deposited by sputtering. Photoresist was deposited on the sample and Al patterns are defined by photolitography and subsequent Al wet etching. Using the formed Al mask, RIE (SF<sub>6</sub>-O<sub>2</sub> 250W – 60mTorr) was performed to locally remove the Si and SiC up to 4 $\mu$ m in the substrate

The sample as prepared is heated up to  $1000^{\circ}$ C in a RF reactor on a graphite susceptor under 5 slm Ar. Propane is then flowed in the reactor and reacts with the Al-Si melt formed by the Al/Si patterns. Al-doped SiC layers are thus grown selectively at the place where the liquid is present. Results of selective growth by VLS are presented in the figure 1. It is clear that this method enables to grow SiC layers with different size (up to 800 µm) and shape of patterns. For larger patterns, it is important to increase the Al/Si bilayer thickness in order to avoid dewetting upon melting. Note that the initial Al/Si thickness ratio corresponds to a molar ratio of 70/30.

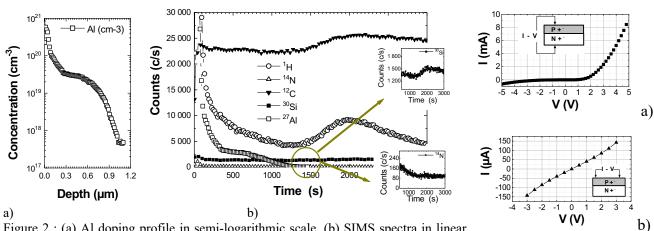
The Al doping concentration was determined by SIMS measurements with CAMECA IMS4F using an  $O^{2+}$  ion beam. The Al profile (figure 2a) presents a very high concentration in surface (4 to  $5.10^{20}$  cm<sup>-3</sup>) in the first 40 nm to decrease after to a plateau of  $3.10^{19}$  cm<sup>-3</sup> and finally to fall at the interface between the VLS layer and the substrate. This could be related to the Si content impoverishment during VLS growth as the initial amount of Si is limited. The interface is clearly showed by the evolution of  $^{12}C$ ,  $^{30}Si$ ,  $^{14}N$  or  $^{1}H$  profiles: the first two increase simultaneously before to reach a constant plateau revealing a stoichiometric difference between the epitaxial VLS layer and substrate; the  $^{14}N$  decreases indicating a higher N concentration in the epitaxial VLS layer; the hydrogen profile shape follows the one of Al in the VLS layer with an overshoot at the interface. Electrical I-V measurements were performed on these layers, in vertical configuration (figure 3a) to chuck the insulation of the epitaxial layer from the substrate, and in horizontal configuration (figure 3b) to estimate the sheet resistance of these layers. In vertical mode a rectifier behavior is found with a threshold voltage of 2V in forward bias. The p-n junction is confirmed and thus the



<u>Figure 1 :</u> illustration of the selective growth using VLS process. Figure a and c) before the growth. Figure b and d) after the growth. Note the remaining Al-based droplets on the patterns. The white scale corresponds to  $500 \ \mu m$ .

p-type layer may be electrically analyzed. In lateral mode the almost linear current versus voltage variation shows ohmic contact behavior between the pads (tungsten carbide) and the p-type SiC. We remark the low level of the current, which is typical for semiconductor behaviour of the p-type SiC layers. To estimate the sheet resistance of the formed p-type SiC layers, four - points I-V measurements were performed on Van-der-Paw structures. The sheet resistance found was  $5.5k\Omega$  which represent a promising result compared to those obtained on ion implantation layers [4]. The square resistance is still high due to the Al concentration decrease from the surface to the interface (the calculated sheet resistance with this profile is about 3.5 k $\Omega$ ). On the other hand, no difficulty was encountered to take the contact thanks to the higher Al level at the surface.

In the final paper the discussion will de developed on the electrical properties of the p-type SiC layers and its physical properties.



<u>Figure 2</u>: (a) Al doping profile in semi-logarithmic scale, (b) SIMS spectra in linear scale with the evolution of  ${}^{12}C$ ,  ${}^{30}Si$ ,  ${}^{14}N$ ,  ${}^{1}H$  and  ${}^{27}Al$  profiles at the interface

<u>Figure 3 :</u> I – V measurements in vertical (a) and lateral configuration (b)

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