



HAL
open science

A 3.5 kV thyristor in 4H-SiC with a JTE periphery

Pierre Brosselard, Thierry Bouchet, Dominique Planson, Sigo Scharnholz,
Gontran Pâques, Mihai Lazar, Christophe Raynaud, Jean-Pierre Chante, Emil
Spahn

► **To cite this version:**

Pierre Brosselard, Thierry Bouchet, Dominique Planson, Sigo Scharnholz, Gontran Pâques, et al.. A 3.5 kV thyristor in 4H-SiC with a JTE periphery. European Conference on Silicon Carbide and Related Materials (ECSCRM 2004), Sep 2004, Bologne, Italy. hal-02953080

HAL Id: hal-02953080

<https://hal.science/hal-02953080>

Submitted on 5 Oct 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

A 3.5 kV thyristor in 4H-SiC with a JTE periphery

Pierre Brosselard^{a, b}, Thierry Bouchet^c, Dominique Planson^b, Sigo Scharnholz^a, Gontran Pâques^a, Mihai Lazar^b, Christophe Raynaud^b, Jean-Pierre Chante^b, and Emil Spahn^a

^{a)} French-German Research Institute of Saint Louis (ISL), B.P. 34, F-68301 Saint Louis cédex, France

^{b)} Centre de Génie Electrique de Lyon (CEGELY) INSA-Lyon, UMR 5005 CNRS, Bât. Léonard de Vinci, 20 av. Albert Einstein, F-69621 Villeurbanne, France

^{c)} IBS Z.I. Peynier-Rousset Rue Gaston Imbert Prolongée 13790 Peynier France
corresponding author: pierre.brosselard@insa-lyon.fr

Today, at ISL, there are pulsed power applications under investigation which handle electric energies up to 10 MJ using switching elements as sparc gaps or high power semiconductors based on silicon [1]. Since silicon based technology is reaching its physical limits concerning blocking and power handling capability, GTO thyristors based on SiC are under investigated for compact future pulsed power systems we are investigating [2]. Reaching breakdown voltage of 19 kV [3], the potential of SiC based devices appears very interesting.

According to preparatory device simulations using the finite element code MEDICITM, the developed GTO-thyristors should be able to block voltages up to 6 kV. The models and parameters used by the simulator are described by Brosselard and al. in [4].

Simulations with different fixed charge densities at the oxide/SiC interface have been realised with a 1.5 μm oxide thickness. The results are shown in figure 2. A negative charge induces a positive charge in SiC which limits the extension of the space charge so that the breakover voltage decreases.

The n-type 4H-SiC wafer material was purchased from Cree ResearchTM, including a P⁺PNP⁺ (from the wafer up to the top) epitaxial layer structure (figure 1). The process sequence has been divided in five photolithographic levels. The realization has begun with two different dry etchings, the first allowing to take the gate contact, the second one necessary for the mesa protection. A nitrogen implantation followed by 1700°C/30mn annealing were needed to realise the JTE. After an oxide deposition to passivate the thyristor structure, a nickel metallisation has been realized.

The static characterisations used to evaluate the breakover voltage were performed using a 12.5 kV high voltage source. The maximum breakover voltage equals to 3.5 kV, as illustrated in figure 2. The previous simulations show that the fixed charge density is negative and included between 2 and 3 $\times 10^{12}$ cm⁻². Other samples must be produced and characterised to extract the charge density from C(V) measurements.

All devices on the sample have been electrically characterised with a 1100 V Keithley K2410. Figure 3 shows the location of the breakover voltage on the wafer surface. The dark ones hold a voltage up to 1kV. This figure clearly shows that the repartition of the better ones, is not uniform. We can see that most of them are placed in the upper left side of the sample, whereas nearly no thyristor, able to hold a higher voltage, are placed in the left border region. That illustrates the non uniform distribution of wafer defects []. We can also see through figure 4 that the device area has a large impact on the breakover voltage. Indeed only the smallest devices (0,2 mm²) were able to hold voltages above 3000 V.

We conclude, that the results are encouraging for the use of the thyristors in power applications. The turn-on characterisations are in progress and will be described in the final paper.

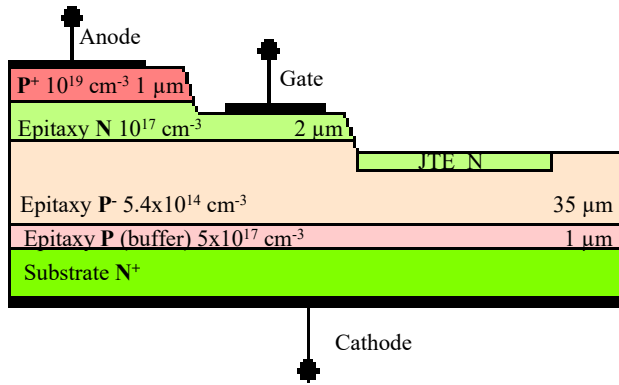


figure 1 : Thyristor description with JTE protection

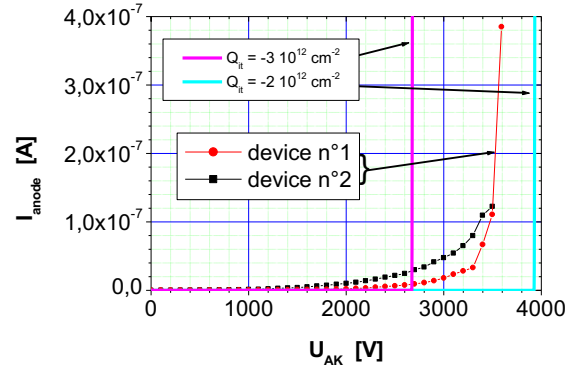


figure 2 : Experimental and simulated electrical characteristics

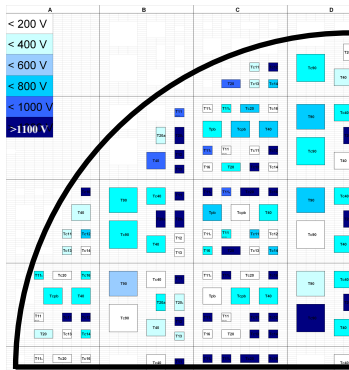


figure 3 : Repartition of the breakover voltage of thyristors as a function of the device place on the quarter wafer surface

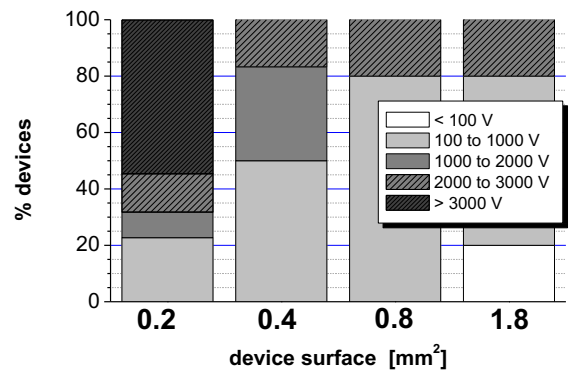


figure 4 :Statistic of the breakover voltage as a function of the device surface (in percents)

[1] : E. Spahn, G. Buderer, V. Wegner, F. Jamet 9th IEEE Pulsed Power Conference Albuquerque/NM, USA, 18-24 June 1993

[2] : S. Scharnholz, V. Zorngiebel, P. Brosselard, and E. Spahn; in IEE Proc. of the 1st European Pulsed Power Symposium (EPPS) , 22-24 October 2002, Saint Louis, France; 2002; pp. 14/1-14/6.

[3] : Y. Sugawara, D. Takayama, K. Asano, R. Singh, J. Palmour, T. Hayashi : Proceedings of 2001 International Symposium on Power Semiconductor Devices & Ics, Osaka, pp. 27-30

[4] : P. Brosselard, D. Planson, S. Scharnholz, V. Zorngiebel, M. Lazar, C. Raynaud, J.P. Chante and E. Spahn. Proc of Int. Semiconductor Conference (CAS), Sinaia, Roumania, 2003; pp. 219-221