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Abstract : For CMOS processing compatibility, hybrid bonding of III-V materials on Silicon should be operated below 300°C, requiring an interfacial layer as thin as possible in order not to hamper the electrical transport through the interface. Both SiO_2 and ZnO interfacial layers have been investigated in the case of n-InP/n-Si hybrid heterostructures. Efficient electrical transport through oxide-mediated bonded InP/Si heterostructures is demonstrated, related to tunneling through the oxide-interfacial layer. These electrically-operated oxide-interfacial-layer heterostructures provide both efficient bonding processing and open the field for full 3D design and operation of optoelectronic devices.

Introduction

In the domain of Silicon photonics, the ability to electrically operate the hybrid III-V on Si (or SOI) interface will open the full 3D field bringing new design opportunities and immense gains for thermal-budget, chip power consumption, footprint and integration of driving electronics. Electrical transport has been demonstrated in the case of GaAs/Si [1-2] ; it has also been demonstrated in the pioneer work of D.Pasquariello [3] in the case of both hydrophobic and hydrophilic InP/Si bonding , and recently for air-bonded InP/Si [4].

Hybrid heterostructures obtained by bonding have the advantage versus heteroepitaxial growth to offer a high crystalline quality, even though the lattice mismatch is important, being ~8% in the case of InP/Si. We have here considered bonding processes being CMOS processing compatible. Bonding has then to be operated at a temperature below or at 300°C maximum in order to preserve the already processed contacts. Thus an intermediate layer is mandatory, otherwise wafer fusion without intermediate layer is reported to be operated in the 600°C temperature range, in the case of InP/GaAs [5] or hydrophobic bonding is reported to be operated at 400°C in the case of InP/Si [3].

The intermediate layer commonly introduced is a SiO_2 layer, due to its large compatibility with Silicon. It can be an intentionally deposited SiO_2 layer with a thickness in the [5-50] nm range; this approach has been widely implemented for hybrid devices [6-9] but such a large thickness prevents electrical transport through the interface. When bonding is operated without any intentionally deposited layer but under ambient air, this processing leads to a non-controlled thickness of the oxide layer at the interface, which is in the [2-5] nm-thick range in the case of [1], or which thickness is not given in the case of [4]. For such a thin layer, electrical transport has been measured thanks to tunneling through the oxide layer. In order to generate an ultra-thin SiO_2 interfacial layer, we have developed a process operating under vacuum with de-oxidized surfaces activated by ozone, reaching a 1.2nm-thick oxide interface layer [10].

Hybrid interface

We consider here bonding operated at 300°C, thus including an interfacial layer. We have investigated two interfacial layers: (i) the SiO_2 interfacial layer generated by ozone-activated bonded surfaces and (ii) an intentionally deposited thin ZnO interfacial layer, taking advantage of the conductivity of this metallic oxide [11-12].

In order to clearly evidence the degradation of the electronic transport that could be brought by the intermediate oxide layer, we have considered a hybrid heterojunction with doping polarity and concentration leading to an ohmic behaviour without any oxide. The n-Si 10^{19} cm^{-3}/n-InP 10^{19} cm^{-3} doping polarity and concentration heterostructure has already experimentally demonstrated an ohmic behavior [13]; this choice is also supported by the band diagram calculated with the CHARGE solver

of the Lumerical commercial tool. Figure 1 indicates that an ohmic behavior can be expected due to the reduced potential barrier at the conduction band edge. The energy reference Fermi level is taken at 0 eV.

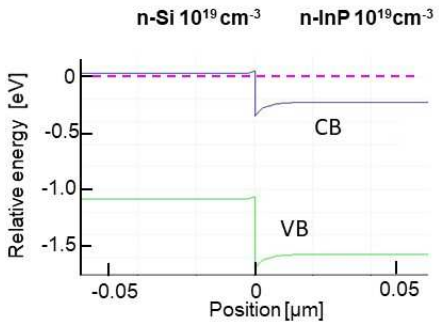

Figure 1: Band diagram (Conduction Band and Valence Band) calculated by Lumerical CHARGE solver . Doping are n-Si/ n-InP both $10^{19}cm^{-3}$

Additionally, the high doping of both materials ensure a negligible contribution of both material sections to the measured resistance.

Oxide-mediated bonding

Both 1cm square InP and Si samples are de-oxidized, terminated by HF last. Both surfaces are then activated by ozone –O_3- and annealed under vacuum at 300°C during 1 h 30 min, with a slight pressure. Such a process has produced a 1.2nm-thick SiO_2 interfacial layer [10]. Figure 2-left shows the STEM image of the interface, evidencing no structural defect in both lattices. Figure 2-right shows in-situ EDX profiles for all the elements, Oxygen is present at the interface, without any diffusion in either lattice. The residual roughness of both surfaces being in the [0.3-0.4] nm range, such a thin layer could be very close to the thinnest possible layer for oxide-mediated bonding. Annealing experiments operated up to 500°C have evidenced the layer stability, without any migration or reordering.

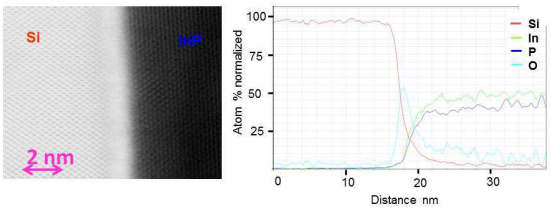

Figure 2 : O_3 activation bonded interface

left: STEM image of the interface

right : in-Situ EDX all elements distribution [9]

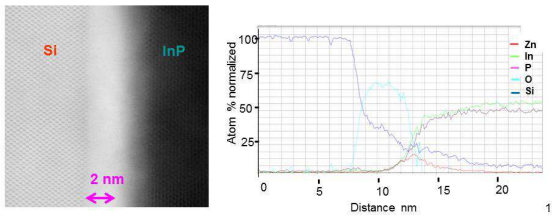

Figure 3: ZnO-mediated bonded interface

left: STEM image of the interface

right: in-Situ EDX all elements distribution

We have also considered a conductive oxide intermediate layer, since even if its thickness will be several nanometers, its conductivity would not hamper the electrical transport. ZnO is well known to present a conductivity related to oxygen vacancies [11-12]. Both InP and Si surfaces are prepared oxide-free as described in [10], a ZnO layer 1.6 nm-thick has been deposited by sputtering at room temperature on the InP surface only. Both surfaces are then immediately brought into contact and annealed at 300°C under vacuum during 1 h 30 min, the same bonding procedure used for ozone-activated surfaces [10]. Figure 3-left shows the STEM image of the interface, evidencing no structural defect in both lattices. Figure 3-right shows in-situ EDX profiles for all the elements. The Zn element distribution has a 15% maximum, showing a large inter diffusion both in Si and in InP. This inter diffusion is enabled since the sputtering deposition at room temperature produces an amorphous layer of low density which easily diffuses during the 1 h 30 min duration annealing at 300°C for bonding. The oxygen element is present on a distance of ~ 4nm, larger than the 1.6nm-thick ZnO deposited layer, and on the Silicon element side mainly, indicating that silicon has been oxidized, generating the stable oxide SiO_2. The 4nm-thick oxide interface layer is then a sum of SiO_2+ $Zn(Si)O_x$ +ZnO.

Electrical processing and measurements

For electrical transport measurement, a n-doped (S) $1x10^{19}$ cm^{-3} 500nm-thick InP membrane has been bonded on a n-doped (P) $1x10^{19}$ cm^{-3} Si substrate. Both oxide bonding, ozone-activated surfaces and ZnO intermediate layer, as well as an oxide-free bonding, have been processed and measured, the oxide-free interface being a benchmark since it has already evidenced efficient electrical

transport [13-14]. After substrate removal, the InP membrane evidences so surface defect. 150µm-diameter mesa were etched by Cl_2-based Inductive Coupled Plasma etching through the InP membrane down to the Si substrate. Electrical contacts were performed, a Ti-Au contact on top of the InP mesa, and a Ni/Au/Ge contact on the Si substrate. These two contacts have been qualified to be ohmic. The Si contact geometry has a circular pattern 100µm wide and 110µm far from the InP mesa as sketched in Figure 4 left. Electrical measurements were conducted using a four-probe set-up allowing the exclusion of probe resistance, the current being forced from the mesa contact to the outer contact. V(I) transport characteristics of the heterojunctions (figure 4 right) show ohmic behavior in the case of the oxide-free bonded interface, as already reported, and also for the oxide-mediated bonded interfaces.

In the case of the SiO_2 1.2nm-thick interface layer obtained with the ozone activation of de-oxidized surfaces, this ohmic behavior confirms the tunneling transport already proposed as the transport mechanism in the GaAs/Si interface [1], and corroborates the measurement performed on InP/Si air-bonded interfaces [4] since, even if no TEM picture is provided to clearly show what exists at this interface, an oxide layer is most probably present due to the bonding being operated in ambient air. Related to this tunneling mechanism, the thinnest oxide layer is sought since the current transport is a decaying exponential function of the oxide layer thickness.

The ZnO bonded interface also shows an ohmic behavior comparable to the O3-activation bonded interface leading to the SiO_2 intermediate layer. Even being thicker (~4nm-thick), the multi composition of this oxide layer (SiO_2+ $Zn(Si)O_x$ +ZnO) evidenced by the in-situ EDX profiles of the elements, allows tunneling through its SiO2 part, and conduction through its Zn-based part which is Si and In-doped due the inter diffusion. As a consequence, the ZnO bonded interface has an electrical behavior very similar to the one including the SiO_2 interfacial layer obtained by O_3-activated surfaces.

The major contribution to the resistance being the interfacial resistance, when compared to the oxide-free bonded interface, both oxide-bonded heterostructures show no significant increase of the resistance related to the presence of the oxide layer at the interface.

The resistivity calculation is beyond the scope of this paper, since its correct calculation would require a current flow simulation to quantify the electric field lines according to the structure and contacts

geometry and a quantitative measurement of any possible surface currents along the etched mesa walls.

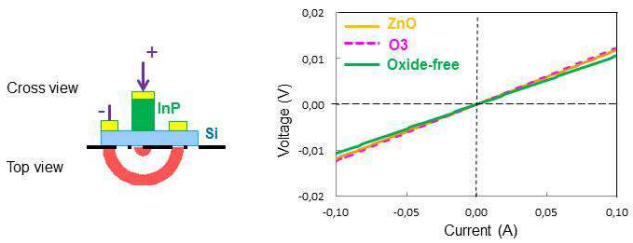

Figure 4 *Left*: Schematic of the electrical contacts (not at scale)

Right: V(I) Transport characteristic of the hybrid interfaces

Discussion

Even though these experimental measurements demonstrate that a very thin oxide intermediate layer does not increase the interfacial resistance when compared to an oxide-free interface, thus allowing efficient electric transport, the proposed involved mechanisms remain macroscopic. Commercial simulation tools implementing energy gaps and electronic affinities for the band structure and transport calculation does not allow a detailed description of the interface. They also do not take into account that Si and InP do not have the same crystallographic system and the same polarity. A quantum transport approach simulation should be undertaken in order to correctly describe the complex mechanisms occurring at the interfaces (e.g. bond breaking and charge transfers) and include a detailed description of the oxide interfacial layer, especially when the composition of the oxide layer becomes complex due to diffusion during bonding and its related annealing. Advanced simulation implementing full-band quantum simulation with empirical pseudopotential and Non Equilibrium Green Function formalism [15] is under development to support an optimized design of the interfacial layer for efficient electrical transport.

Conclusion

In this study, we have demonstrated that an oxide layer, being thin enough, does not hamper the electrical transport through a n-InP/n-Si hybrid heterostructure. Bonded hybrid interfaces obtained

under vacuum operation at 300°C including or a SiO_2 1.2nm-thick interfacial layer or a 4nm-thick complex SiO_2+ $Zn(Si)O_x$ +ZnO interfacial layer have been measured, evidencing an ohmic behavior and no significant increase of the interfacial resistance when compared to an oxide-free bonded interface. Oxide-mediated bonding has thus two advantages, a technological one related to the efficient and easily implementing bonding processing, and a functional one allowing electrical transport through the interface, provided the right choice is made for the thin oxide interfacial layer.

In-depth electrical characterization, involving low-T measurement, is under progress, and a quantum transport approach simulation is currently undertaken in order to correctly explain the conduction mechanisms involved.

References

[1] K.Tanabe, K. Watanabe, Y. Arakawa, *Scient. Rep*. **2012,** *2*, 349

[2] R.Alcotte R. Alcotte, M. Martin, J. Moeyaert, R. Cipro, S. David, F. Bassani, F. Ducroquet, Y. Bogumilowicz, E. Sanchez, Z. Ye, X. Y. Bao, J. B. Pin, T. Baron,. *App. Phys. Lett. Materials* **2016**, *4*, 046101

[3] D. Pasquariello, M. Camacho, K. Hjort, L. Dózsa, and B. Szentpáli, Materials Science and Engineering: B 80, 134 (2001)

[4] R.Inoue, K.Tanabe, *Appl. Phys. Lett*., **2019**, *114*,191101

[5] J. Bentell, F.Wennekes, F. Salomonsson, M. Hammar, K. Streubel, *Physica Scripta* **1999,** *T79*, 206.

[6] A.W.Fang, H.Park, Y.Kuo, R.Jones, O.Cohen, D.Liang, O.Raday, M.N.Sysak, M.J.Paniccia, J.E.Bowers *Materialstoday*, **2007**, *10*, 28

[7] G.H. Duan, S. Olivier, C. Jany, S. Malhouitre, A. Le Liepvre, A. Shen, X. Pommarede, G. Levaufre, N. Girard, D. Make, G. Glastre, J. Decobert, F. Lelarge, R. Brenot, B. Charbonnier , *IEEE. J. Selected Topics on Quantum Electronics*, **2016**, *99*, 379

[8] C-W. Lee, D.K-T Ng, A.L.Tan, Q.Wang *Opt. Lett*., **2016**, *41,* 3149

[9] S.Keyvaninia, G.Roelkens, D.Van Thourhout, C.Jany, M.Lamponi, A. LeLiepvre, F.Lelarge, D.Make, G.H.Duan, D.Bordel, J.M.Fedeli, *Opt. Expr*, **2013**, *21*,3784

[10] A. Talneau, G. Beaudoin, D. Alamarguy, G. Patriarche, *Microelec. Engin*., **2018**, *192*, 25

[11] L. Liu, Z. Mei, A. Tang, A. Azarov, A. Kuznetsov, Q. Xue, X. Du , *Phys. Rev. B* **, 2016,** *93*, 235305

[12] X. Yu , H. Zheng, X.Fang , H. Jin, M.Cao *Chin. Phys. Lett*. **2014**, *31*, 117301

[13] K. Pantzas, A. Itawi, L. Couraud, J.C. Esnault, E. Le Bourhis, G. Patriarche, G. Beaudoin, I. Sagnes, J. Streque, A. Talneau, , *IPRM* , **2014**, Tu D2-3

[14] A.Talneau, C. Roblin, A. Itawi, O. Mauguin, L. Largeau, G.Beaudoin, I. Sagnes, G. Patriarche, C. Pang, H. Benisty, *Appl . Phys. Lett.*, **2013**, *102*, 212101

[15] M. Pala, D. Esseni, *Phys. Rev. B*, **2018**, *97*, 125310