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Electrical scanning probe microscopy approaches to investigate solar cell junctions and devices

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ABSTRACT

C-AFM and KPFM techniques have been applied to investigate advanced junctions that are currently involved in highly efficient silicon solar cells. Our first study focuses on silicon heterojunctions and notably hydrogenated amorphous silicon (a-Si:H)/crystalline silicon (c-Si) P/n or N/p heterostructures which band bending at the interface forms a 2D channel. This conductive channel was indeed evidenced for the first time by cross-sectional investigations by C-AFM confirming the analysis of macroscopic planar conductance measurements.

A second example of nanoscale characterization concerns the passivating selective contacts consisting in a thin silicon oxide (SiO_x) layer between the c-Si and a highly doped polysilicon (poly-Si) layer. The electrical carrier transport is here not limited by the oxide layer and it is assumed that tunnelling through the oxide and/or the presence of pinholes are the main competitive mechanisms. For this specific heterostructure KPFM reveals local surface potential drops of 15-30 mV, which do not exist on samples without SiO_x. These potential drops suggest the presence of pinholes that are formed during the poly-Si annealing process performed in the range of 700-900 °C.

Finally, in a third study, we concentrate on p-i-n radial junction (RJ) silicon nanowire (SiNW) devices that are investigated under illumination by KPFM, in the so-called surface photovoltage (SPV) technique. This work focuses on the possibility of extracting the open-circuit voltage (V_{OC}) on single isolated SiNW RJ by local SPV measurements using different AFM tip shapes and illumination directions in order to minimize shadowing effects.

Keywords: C-AFM, KPFM, SPV, silicon heterojunctions, polysilicon, passivated contact, silicon nanowires (SiNW)

1. INTRODUCTION

Conductive and Kelvin probe atomic force microscopy (C-AFM and KPFM) techniques are powerful tools that are commonly used in microelectronics for carrier/dopant and junction profiling analysis.^{1,2,3} In a natural way the capabilities of these techniques have also gained the interest of the photovoltaic (PV) community in particular to analyze material, interfaces, and junction properties.^{4,5,6}

In this respect, we introduce in the following subsections three examples of AFM analyses applied to the study of interfaces, junctions and nanodevices, , some of which are involved in high-efficiency silicon solar cells. The main results and achievements for each example will be then presented and discussed separately in the next section.

1.1 Amorphous silicon/crystalline silicon interface

Among the most interesting heterojunctions in the field of photovoltaics (PV) the combination of crystalline silicon (c-Si) with hydrogenated amorphous silicon (a-Si:H) has opened up new fields of study, especially after demonstrating the highest solar efficiency to date for single-junction c-Si technology.⁷ This technology known as silicon heterojunction (Si-HET) takes advantage from its hetero-interface where recombination has been greatly improved notably by inserting an intrinsic a-Si:H buffer layer, between the doped c-Si absorber and the doped a-Si:H layer.⁸

The physics of this interface is not particularly simple mainly because the interface properties are generally difficult to access, and the quality of the device is generally assessed through the open-circuit voltage of the cell or the effective lifetime in the c-Si wafer, measured from various techniques like photoluminescence, photoconductivity decay or from other techniques.^{9,10,11,12} More specifically, the device physics of the Si-HET cannot be analysed with the conventional theory junction where a depletion approximation in the space charge region is commonly adopted. In this respect, it has been predicted and afterward demonstrated the existence of a strongly inverted layer at the c-Si surface layer that requires to be taken into account.¹³ Concerning this last point, electrical measurements and more particularly those involving atomic force microscopy (AFM) have played an important role in highlighting this inversion layer.¹³⁻¹⁵

In next section, we will address and review some of our main results concerning cross-sectional investigations of (n) a-Si:H/(p) c-Si interfaces specifically through the C-AFM technique.

1.2 Passivating selective contacts: Poly-Si/SiO_x/c-Si

As an ongoing effort to improve the efficiency of single junction c-Si solar cells, the polysilicon (poly-Si) passivating contact architecture was developed to minimize the recombination losses at the level of contacts.¹⁶ This architecture uses a very thin SiO_x layer (1~2 nm) between a heavily doped poly-Si films and a c-Si absorber.^{17,18} It should be noted that this structure is inspired by the works carried out in the 1980s by Yablonovitch et al.¹⁹ on solar heterostructures involving microcrystalline silicon and silicon dioxide layers, and Van Halen et al.²⁰ on bipolar transistors based on poly-Si tunnel junction contacts.

The conduction mechanisms taking place across this structure are not straightforward. Initially the tunneling current through the SiO_x was considered as the main mechanism, however recent investigations on selective wet etching of poly-Si have revealed the presence of pinholes in the SiO_x layer indicating new paths for the electrical transport of charges.²¹⁻²³

In the next section of this paper, we will explore highly doped poly-Si/SiO_x and intrinsic poly-Si/SiO_x contact structures by C-AFM and KPFM approaches, in order to explore the electrical transport mechanisms and notably the capability to detect the presence of pinholes.²⁴

1.3 Silicon nanowires

Nanowire (NW) arrays offer another promising route for improving performances in photovoltaic (PV) devices. Concretely, NWs based on radial junctions (RJ) combine optical light trapping and carrier collection strategies that are assumed to enhance solar efficiency compared to conventional planar structures.²⁵⁻²⁷ Note that the NW technology also reduces the amount of material used.

For the particular technology of silicon nanowires (SiNWs) efficiencies up to 9.6 % have been reported for RJs based on Si thin-film technology.²⁸ The improvement of these devices requires in particular a fine characterization which ideally can be carried out at different scales. Indeed, the possibility to characterize the photoelectric performances of individual nanowire devices would open new perspectives in the optimization of the final device.

In this context, KPFM technique was used with the idea to evaluate the local open-circuit voltage (V_{OC}) of RJ SiNW devices through surface photovoltage (SPV) measurements. To this end, we have explored two approaches. The first approach was focused on the analysis of *completed* devices where the SiNW solar cells are finalized with ITO as front electrode. The *completed* devices were sequentially characterized by current-voltage (I-V) and KPFM measurements with the final goal to extract and compare V_{OC} and SPV. The second approach, which is based mainly on SPV measurements, was to look at single, isolated RJs where the SiNW device has no front ITO contact. The review and the results achieved for these two experimental approaches are presented in the next section.

2. RESULTS AND DISCUSSION

2.1 C-AFM investigation of a-Si:H/c-Si interface

C-AFM measurements were carried out using a Multimode Nanoscope IIIa AFM with the homemade electrical extension named Resiscope.²⁹ This extension based on a logarithmic amplifier is used in contact mode and applying a stable DC bias voltage to the sample. The measurements were performed with a conductive diamond coated AFM tip (CDT-FMR) with a cantilever spring constant of 2.8 N/m and applying forces in the range 100-500 nN.

Figure 1 schematizes the studied sample cross-section with the C-AFM setup. The sample has a symmetric configuration where the same a-Si:H layer was deposited on both sides of the c-Si absorber followed by ITO, the sample was thereafter cleaved before cross-sectional measurements. The thickness of the a-Si:H was deliberately chosen thick (300 nm) to facilitate the localization of the interface between the (p-type) a-Si:H layer and the (n-type) c-Si wafer. The optimized measurement conditions were found after a deoxidation of the cross-section surface by a HF 1% dip and performing the C-AFM scans under nitrogen atmosphere.^{14,15}

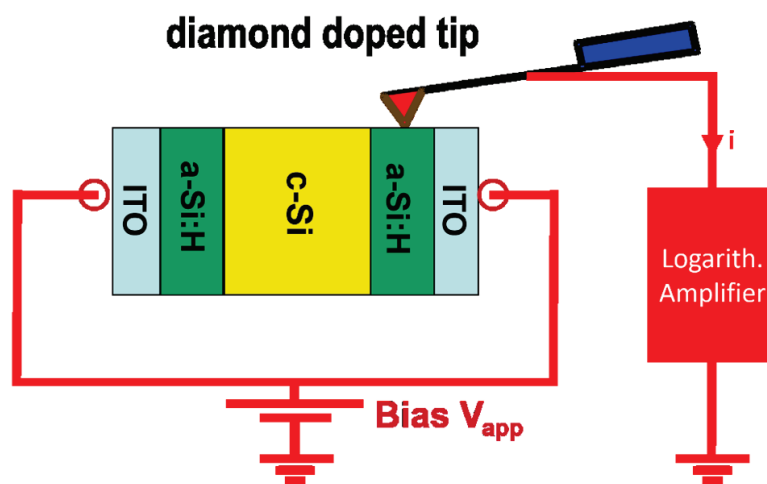


Figure 1. Scheme illustrating the a-Si:H/c-Si sample in a cross-sectional configuration during the C-AFM measurement.

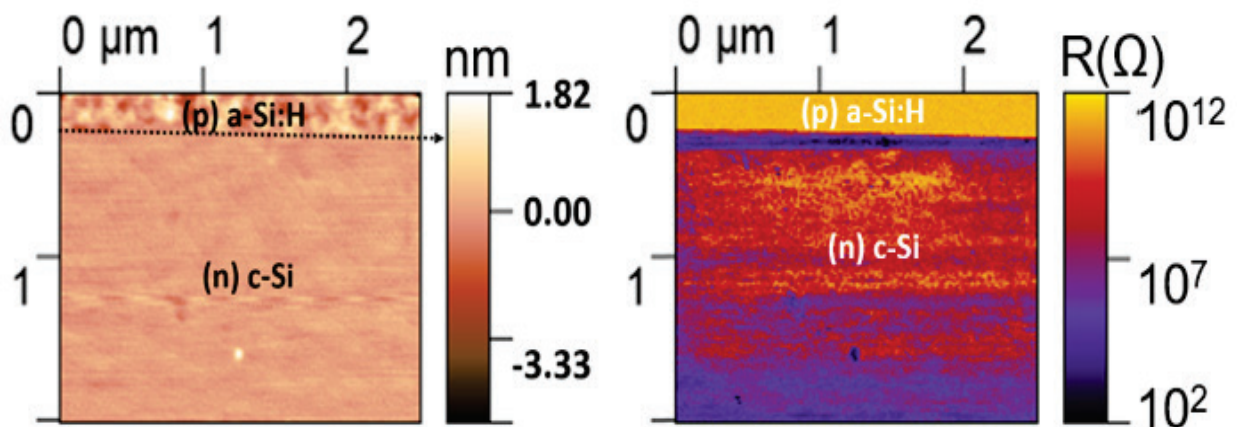


Figure 2. C-AFM image illustrating a cleaved section of an (p) a-Si:H/(n) c-Si heterointerface. Left : topography; right : local resistance mapping (logarithmic scale). Data from Ref.[30].

Figure 2 illustrates the topography and the local resistance mapping on the cross-section after a HF dip and for an applied voltage of 1 Volt. The scanned area shows, from top to bottom, the n-type a-Si:H layer (≈ 300 nm) and the p-type c-Si substrate. The ITO contact is here not observable since it has been partially removed from the top edge with the HF treatment. The electrical image points out in particular a much lower resistance at the interface between the a-Si:H and the c-Si substrate. More precisely, this lower resistive channel is located within the c-Si substrate.

Cross-sectional profiles are illustrated in Figure 3.a, height and local resistance profiles were extracted from the preceding mappings, notably the averaged AFM profile was performed over a width of $0.5 \mu\text{m}$. The profiles along the heterointerface show a flat cleavage surface (topographical variations lower than 5 nm) and a high electrical contrast between the conductive channel and both the a-Si:H layer and the c-Si substrate. In addition to the conductive channel in the c-Si side it is also possible to identify a region with a decreasing conductivity of about 1 micron in width. This is the order of magnitude of the width for a depleted space charge region in c-Si. Due to the low surface roughness of the cross-section it remains important to note that the observed conductive layer cannot result from an experimental artefact. The resistivity profile across the (n) a-Si:H/p c-Si hetero-junction was also calculated with the AFORS-HET simulator and illustrated in Figure 3.b.³¹ The shape of the calculated profile is very similar to the one measured by C-AFM. Note that the same C-AFM observations were also evidenced on other samples with different thicknesses of a-Si:H.

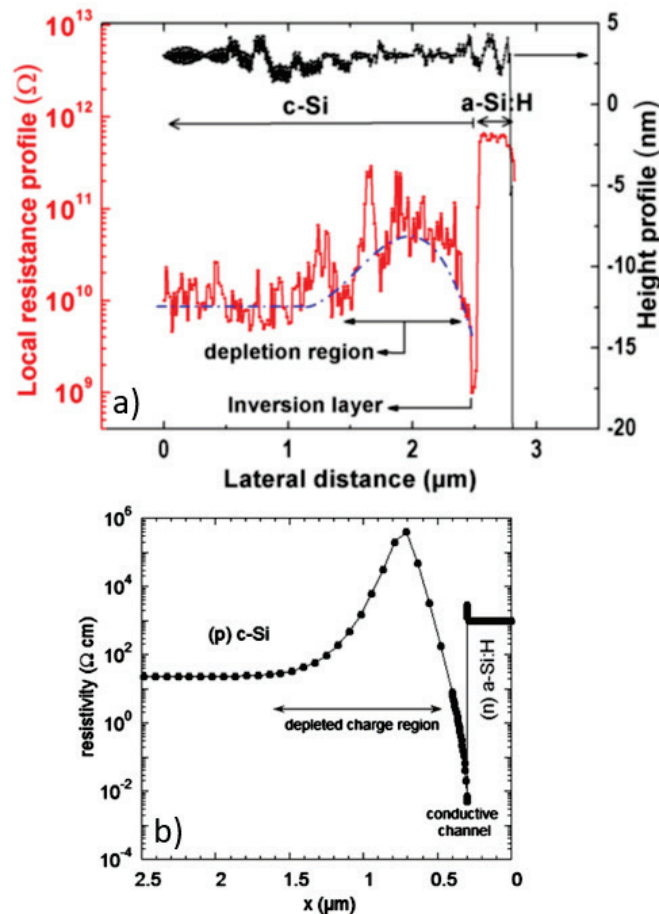


Figure 3. a) Local resistance (left ordinates) and height (right ordinates) profiles extracted by C-AFM across the (n) a-Si:H/(p) c-Si interface; b) resistivity profile calculated across the same interface using AFORS-HET simulator. Data from Ref. [14].

The C-AFM analysis clearly reveals a more conductive layer between the c-Si substrate and the a-Si:H film, which corresponds to the predicted strong inversion layer in (n or p) a-Si:H/ (p or n) c-Si heterojunctions.³² From a purely quantitative point of view the profile results of this inversion layer extracted by C-AFM measurements have to be considered carefully. Indeed, the reliability of the latter is affected by a multitude of factors amongst which the contact quality (sample surface roughness, AFM tip radius, shape, pressure...) and the surface band-bending due to surface states can greatly impact the conductance values. Many of these limiting factors have been here mitigated, thanks in particular to the HF treatment applied after cleaving which enabled to remove the native oxide on the c-Si and at the same time to temporarily passivate it.³³ The very low roughness of the surface cross-section and the nitrogen atmosphere while measuring were very beneficial in providing experimental evidence of the strong inversion layer in crystalline silicon heterojunctions.

2.2 C-AFM and KPFM applied on poly-Si/SiO_x/c-Si structures

For this study, C-AFM and KPFM measurements were carried out using a scanning probe microscopy system from HORIBA/AIST-NT (TRIOS platform). C-AFM was carried out with the electrical extension Resiscope associated to conductive platinum silicide AFM tips (PtSi-FM) with a cantilever spring constant of 2.8 N/m. KPFM measurements were performed using two pass mode using either AM (amplitude modulation) or FM (frequency modulation) conditions with conductive platinum/iridium coated AFM tips (ARROW-EFM).

Regarding the sample fabrication, n-type CZ (Czochralski) c-Si wafers (resistivity of 2–3 Ω cm) were used. A thin SiO_x layer (~1.3 nm) was grown on the wafers surface by integrating a 10 min-long ozonized DI-H₂O rinsing during the wet chemical cleaning process. A hydrogen-rich a-Si layer (a-Si:H) was single-side deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition) on top of the SiO_x layer, using a 13.56 MHz PECVD reactor. Precursor gases consisted of silane (SiH₄), hydrogen (H₂), and H₂-diluted diborane (B₂H₆) for the p-type doping. The a-Si:H (boron doped or intrinsic) layer thickness was targeted in the range 20–30 nm. The samples were annealed in the range 700–900°C in a tube furnace under argon atmosphere in order to activate dopants and crystallize the a-Si:H layer. The full detail of the fabrication can be found elsewhere.³⁴

C-AFM technique was first applied on structures with highly doped poly-Si layers obtained after an annealing at 800°C, and specifically the measurements were realized after poly-Si surface deoxidation using a diluted HF treatment. Measurements were first carried out on a sample with a buffer passivating oxide layer (Figure 4.a) and then on a sample structure without passivating oxide (Figure 4.b) between the poly-Si layer and the c-Si wafer. The current maps of both samples reveal current spots (CSs) of a few nanoamperes (nA) with densities over 100 per μm². Lancaster et al.³⁵ have observed such high density of CSs and correlated them to the spatial degradation of the ultra-thin oxide layer that involves the creation of pinholes. However in our case the CS pattern is observed for both sample configurations (with and without passivating oxide), which suggests that C-AFM maps are not mirroring the spatial distribution of pinholes. Indeed, several properties of the poly-Si (surface morphology, doping, lateral conduction properties ...) can be convoluted in the C-AFM image. In addition, when comparing the density of CSs (250-750 per μm²) with the density of pinholes revealed by selective wet etching (in the range of 10⁻² to 1 per μm²), the CS density is several orders of magnitude higher.²¹ C-AFM measurements performed on highly conductive poly-Si layers thus appear to overestimate the pinholes density in the oxide. Similar conclusions were later presented by Richter et al.³⁶ where no correlation was found between the processed C-AFM measurements and the pinhole density revealed by the selective wet etching.

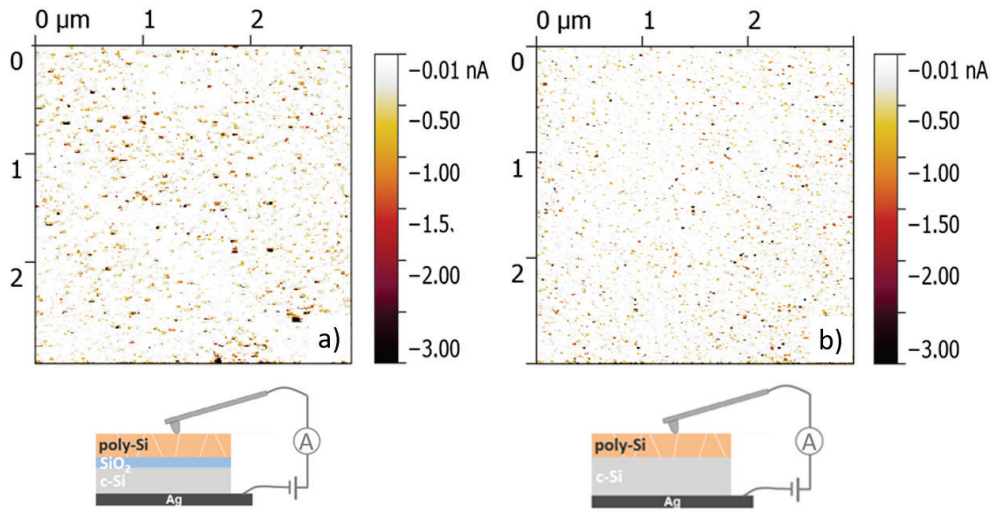


Figure 4. C-AFM scans on: a) poly-Si/SiO_x/c-Si structure with interfacial oxide and b) poly-Si/c-Si structure without interfacial oxide. Data from Ref. [24,34].

KPFM measurements were conducted on the same samples initially analyzed by C-AFM. Both samples have highly doped poly-Si layers resulting from an annealing at 800°C, but one them has no passivating oxide at the poly-Si/c-Si interface. Figure 5.a, measured on the sample with interfacial passivating oxide, reveals local drops of the surface potential with surface density values that vary in the range of 10^{-1} to 1 per μm^2 . Conversely, the KPFM image obtained on the sample without SiO_x (Figure 5.b) shows a homogeneous view with no perceptible changes in the surface potential. The comparison of these two KPFM maps highlights the link existing between the presence of the passivating oxide (underneath the poly-Si layer) and the observed potential drop which density is in line with the wet etching work previously cited.²¹ Regarding the origin of those potential drops we agree with the conclusions of Kale et al.^{22,23} that pointed out a more favorable dopant diffusion process at the pinhole locations which would cause local variations in doping. Note that Kale et al.^{22,23} performed KPFM measurements on passivation contact structures where the poly-Si and the underneath SiO_x layer were sequentially removed. In our experimental approach, we performed the KPFM measurements directly on the poly-Si layer without removing any layer. However, as for the C-AFM measurements, an HF treatment was required to deoxidize the poly-Si surface.

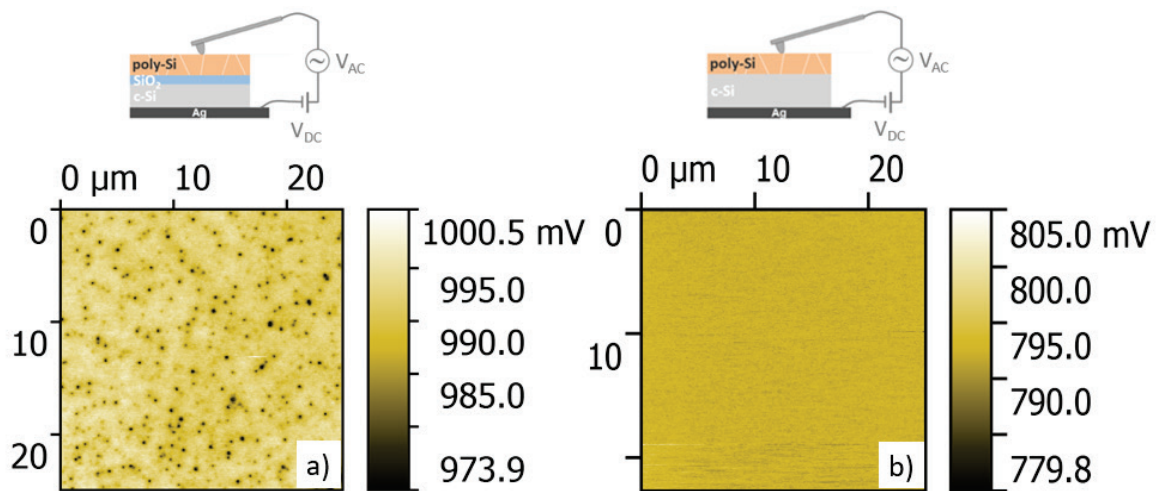


Figure 5. KPFM scans on: a) poly-Si/SiO_x/c-Si structure with interfacial oxide and b) poly-Si/c-Si structure without interfacial oxide.

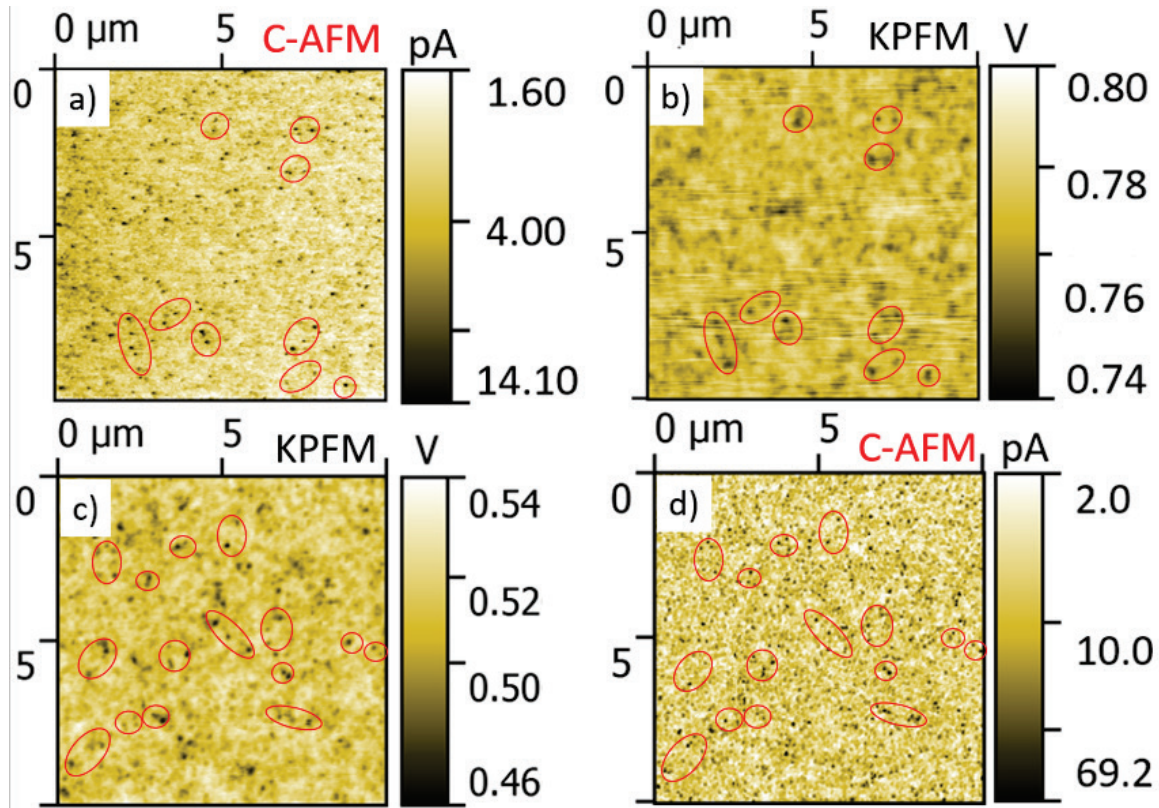


Figure 6. a) C-AFM and b) KPFM correlative measurements of a (i) poly-Si/SiO_x/c-Si sample at the same location; c) KPFM and d) C-AFM correlative measurements on the same sample taken elsewhere.

In a second phase of this study poly-Si/SiO_x/c-Si structures with intrinsic poly-Si, instead of the conventional highly doped poly-Si, were investigated by C-AFM and KPFM with this time the idea to perform correlative measurements at the same scan locations. Figures 6.a and 6.b display an example where the C-AFM was performed first and the KPFM secondly. Correlative analysis of both scans show similar features: local drops of the surface potential in KPFM can be localized as current peaks with the C-AFM. A few red circles have been added on the images to illustrate these common features. Since the C-AFM measurement in contact mode was first performed, the KPFM image appears slightly distorted. In order to solve this problem a new scan was performed using the KPFM technique first and then the C-AFM. These two scans are illustrated in Figure 6.c and 6.d, respectively. With this new pair of mappings we come to the same conclusion, i.e. that some conductive spots correlate well with potential drops, however these similarities concern only a small part of the numerous current spots that are observed by C-AFM. As mentioned earlier, C-AFM mapping can reflect several local properties of the material, namely the electrical conductivity inhomogeneities due to the surface morphology, the thickness variation of the passivating oxide, the highly doping level in the poly-Si layer, etc. In this respect, the implementation of an intrinsic poly-Si layer has favorably minimized the lateral conduction and enabled us to observe for the first time spatial correlations between C-AFM and KPFM mappings.

2.3 SPV and V_{oc} measurements on p-i-n radial junctions (RJ) SiNW

The studied p-i-n radial junctions (RJ) SiNWs were developed on a substrate of ZnO:Al coated Corning glass (Cg). The SiNW growth was performed at temperatures in range 400-500°C by PECVD, and it was mediated using Sn nanoparticles as catalysts. The p-i-n RJ was obtained by depositing thin conformal layers of intrinsic (80 nm) and then n-type (10 nm) hydrogenated amorphous Si (a-Si:H) by PECVD at 175°C on the highly p-doped SiNW core. The devices were then finalized with a conformal deposition of ITO forming circular top contacts of diameter 4 mm defined by a mask during sputter-deposition. The full details of the fabrication are explained elsewhere.^{27,37,38}

As for the previous subsection, KPFM measurements were done using a scanning probe microscopy system from HORIBA/AIST-NT (TRIOS platform). This platform includes three microscope objectives allowing the illumination of the sample from different directions (top, side and bottom). SPV measurements at the micro/nano scale are obtained by subtracting the CPD (Contact Potential Difference) measured by KPFM in the dark to the CPD under illumination. As regards the evaluation of the V_{OC} , it was extracted by I-V measurements under the same illumination conditions by integrating into the platform assembly a micropositioner with a tungsten needle that enabled to contact the device by the front contact.

Figure 7 displays an example of photovoltaic measurement in a *completed* SiNW RJ device. Macroscopic I-V measurements under 488 nm laser illumination and for different power illuminations (70, 150, 270 and 560 μW) are illustrated in Figure 7.a. This latter reveals typical PV cell operating behavior where the short-circuit current, I_{SC} , and the open-circuit voltage, V_{OC} , increase with the incident light power. Figure 7.b shows an illustration (from left to right) of the topography, the CPD under dark and the CPD under 488 nm illumination resulting from successive KPFM measurements performed at the same location. The topography scan reveals a density of NWs per unit area of around 10^9 cm^{-2} with heights varying in the range 500-1000 nm. The CPD scans show mostly local variations of the potential at the NW edges which can be considered as artifacts due to the rapid changes in height between two adjacent NWs. The places which are exempt from such artifact are the top of the NWs where the topography height change remains negligible. All CPD values presented in the following were extracted at the top of the NWs.

Figure 8 therefore compares the V_{OC} and SPV values extracted from the macroscopic I-V and the KPFM measurements as function of the incident illumination power. The results are illustrated in a semi-log scale for two different completed devices. The maximum deviation between the V_{OC} and SPV curves is less than 5% for the lowest illumination power ($\sim 70 \mu\text{W}$) and becomes less than 2% for higher illumination power. For both graphs the SPV and V_{OC} values follow a logarithmic behavior with values in the range 500-600 mV. The slopes of V_{OC} and SPV give an ideality factor (n) of 1.5 ± 0.1 for device 1 and 1.75 ± 0.25 for device 2, respectively. These values are in good agreement with values reported in the literature for a-Si:H p-i-n junctions which are in the range 1.5-2.³⁹⁻⁴¹

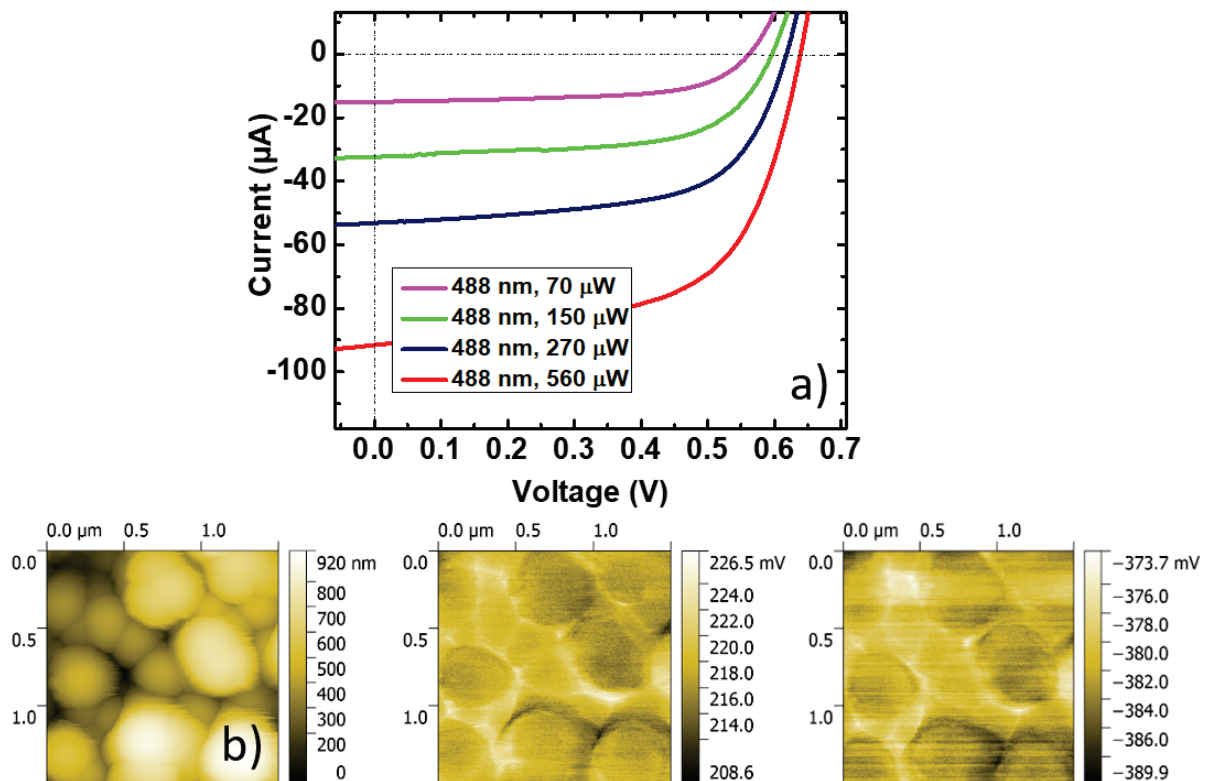


Figure 7. a) Macroscopic I-V curves measured under different power illuminations (70, 150, 270 and 560 μW at 488 nm); b) from left to right: topography, CPD under dark conditions and CPD under illumination (270 μW at 488 nm), respectively. Data from Ref.

[42].

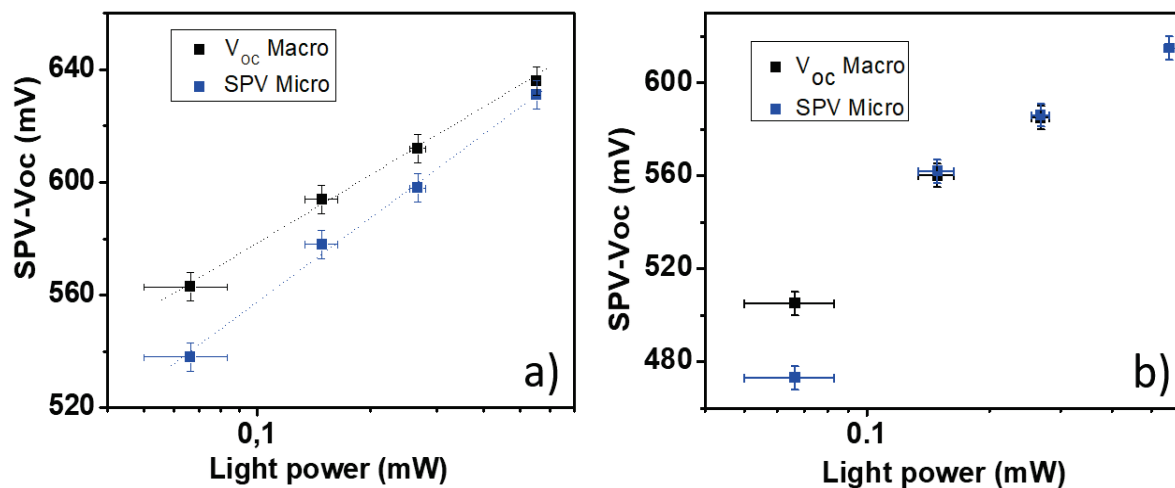


Figure 8. V_{oc} and SPV versus light power for two different devices: a) device 1 and b) device 2. Data from Ref. [42].

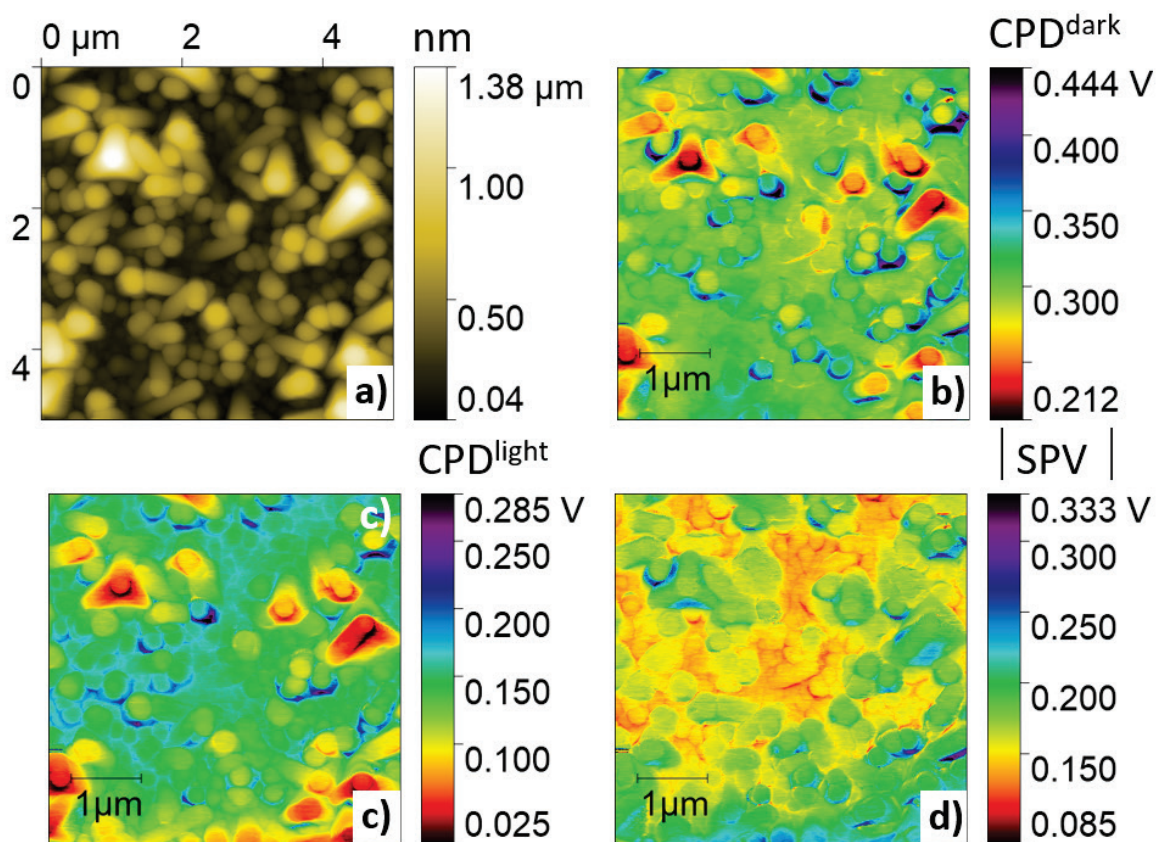


Figure 9. KPFM measurement performed at the same location on isolated NWs illustrating a) the topography, b) the CPD under dark conditions, c) the CPD under white LED illumination and d) the absolute value of SPV.

So far SPV measurements were carried-out on *completed* SiNW RJ devices. In Figure 9 we illustrate an example of SPV analysis obtained on isolated SiNWs. The term isolated here refers to the fact that nanowire RJs are not covered and not electrically connected to each other with an ITO top contact. The SPV mapping d) results from the subtraction of the CPD under dark conditions b) to the CPD under white LED illumination c). This mapping highlights photovoltage variations of up to 50 mV, with notably the lowest values observed in the regions where the NWs appear the smallest with the presence of voids. In accordance with this scanning procedure, the SPV was then analyzed as a function of light power using as previously the 488 nm illumination. Figure 10 displays the SPV results evaluated on isolated SiNW RJ devices. As a reference guide, the SPV curve obtained for the completed RJ device in Figure 8.a) was also added. The reported SPV values correspond to an average value resulting from several tens of NWs. Figure 10.a) (red empty squares) displays the first SPV curve obtained experimentally and corresponds to measurements made with an arrow shape AFM tip (ARROW-EFM) and an illumination coming from the top as in Figure 8 and Figure 9. The very low SPV values for this curve as well as its slope below 1 (~ 0.4) suggests a shadowing effect due to the AFM tip. Indeed keeping the same top illumination and changing the AFM tip by a tilted probe (ATEC-EFM) allowed us to observe an increase of 40 % of the SPV values for the same range of power illumination (Figure 10.b, black filled triangles). Similar results were obtained when changing the illumination from the top to the side and replacing the AFM tip ATEC by the initial AFM tip ARROW (Figure 10.c, blue filled squares). Although the SPV values have significantly increased, they remain below the reference one while keeping similar slopes ($\sim 1.3-1.4$).

The previous results indicate that the local SPV analysis by KPFM on isolated SiNW RJs cannot quantitatively reflect the optimal value of V_{OC} due in particular to the absence of ITO. The extracted local V_{OC} is here restricted by the surface band bending as a consequence of the full depletion of the n-type a-Si:H layer and its oxidation surface state. The measured SPV not only includes the V_{OC} but also the photo induced band-bending change near the surface of the n-type a-Si:H layer.⁴³ Also note that fixed dipole layers at the surface can further add a supplemental potential step.⁴⁴

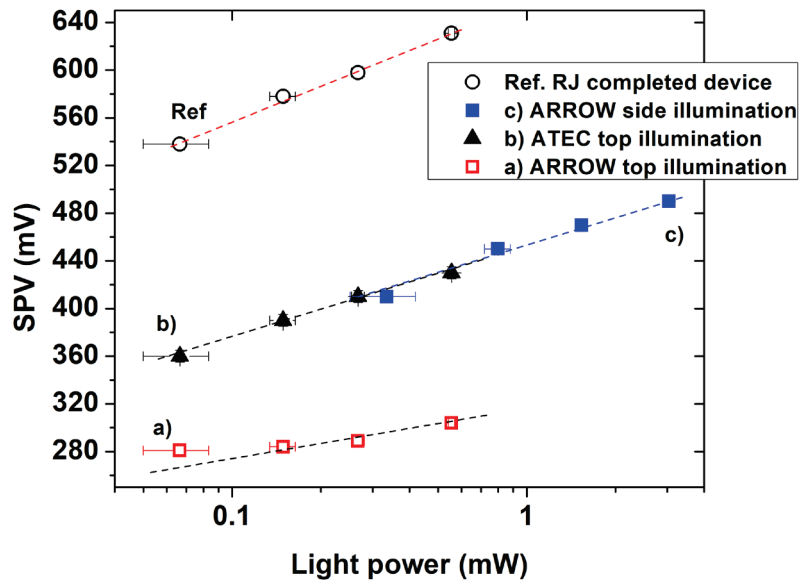


Figure 10. SPV versus light power obtained on isolated RJs. The measurements were performed with different AFM tip shapes (ARROW-EFM and ATEC-EFM) and different directions of illumination (top and side). The reference RJ device designates the device 1 illustrated in Figure 8.a). Data from Ref.[42].

3. CONCLUSIONS

In this work, we illustrate the capabilities of the C-AFM and KPFM techniques to investigate a-Si:H/c-Si heterojunctions, and polysilicon passivating contact structures, both being involved in highly efficient silicon solar device schemes, and radial-junction silicon nanowire solar cells.

For the particular case of silicon heterojunctions analyzed by C-AFM, a conductive channel between the a-Si:H layer and the c-Si substrate was evidenced in (n) a-Si:H/ (p) c-Si heterostructures, related to the existence of a strong inversion layer that was also suggested by planar conductance measurements and reproduced through numerical calculations of the carrier concentration profiles.

Passivated contact structures based on heavily-doped poly-Si and a thin SiO_x layer were investigated in a first attempt by C-AFM. The high density of current spots found is here in contradiction with the density of pinholes revealed by selective etching. This first observation leads us to believe that C-AFM maps can reflect several material features of the poly-Si layer (surface morphology, doping, lateral conduction...) as well as those of the SiO_x layer, especially its inhomogeneities in thickness. The KPFM applied to the same samples evidenced local potential drops without the need to etch the passivated junction. These local drops are expected to be an indirect observation of the dopant diffusion taking place more favorably during the annealing process through the existing pinholes.

Correlative C-AFM and KPFM measurements applied to the intrinsic structures of poly-Si/SiO_x/c-Si enabled for the first time to match certain conductive spots with local potential drops. However, only a small portion of the conductive spots correlate well with KPFM observations. This brings us to the same conclusion that surface morphology, local conduction properties of the poly-Si and thickness inhomogeneities of the SiO_x may contribute to overestimating the density of pinholes.

Finally, in the last sub-section of this article, completed devices based on p-i-n RJ SiNWs were jointly analyzed under illumination by I-V and KPFM measurements. This first comparison carried out for different illumination powers show that the local SPV values extracted from KPFM are very close to the V_{OC} values obtained from I-V analysis. Local SPV measurements on isolated SiNW RJs show, on the contrary, a significant difference from the previous V_{OC} values. A shadowing effect of the AFM tip has been evidenced and minimized changing the tip shape and/or the illumination orientation. The optimized SPV values gathered from isolated RJ SiNWs show a logarithmic behavior with the illumination power but remain well below the V_{OC} reference values. Local SPV analysis on isolated RJ SiNWs cannot quantitatively reflect the optimal value of V_{OC} due in particular to the absence of ITO. Note that the measured SPV not only includes the V_{OC} but also the band-bending change near the surface and further potential steps linked to the presence of surface dipoles.

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