Switching Loss Estimation Using a Validated Model of 650 V GaN HEMTs

Joao Oliveira, Florent Loiselay, Hervé Morel, Dominique Planson

Switching Loss Estimation Using a Validated Model of 650 V GaN HEMTs

Joao Oliveira[1], Florent Loiselay[4]
VEDECOM ITE
23 bis Alle des Marronniers, 78000, Versailles, France
Phone: [1]+33 (0) 6 25 71 40 30 and [4]+33 (0) 6 51 49 81 14
Email: [1]joao-andre.soares-de-oliveira@vedecom.fr and [2]florent.loiselay@vedecom.fr
Hervé Morel[2], Dominique Planson[3]
Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, AMPERE
F-69621, Lyon, France
Phone: [2]+33 (0) 4 72 43 82 38 and [3]+33 (0) 4 72 43 87 24
Email: [2]herve.morel@insa-lyon.fr and [3]dominique.planson@insa-lyon.fr

Keywords

≪Gallium Nitride (GaN)≫, ≪Switching losses≫, ≪Device characterisation≫, ≪Automotive application≫.

Abstract

GaN power devices allow building more compact power converters. In order to study these new devices, it is important to measure and estimate switching losses. Therefore, an instrumented PCB is developed including the measurement points needed for this purpose. The parasitic elements of the PCB layout extracted by ANSYS Q3D and the models of the measurement instruments are also included in the simulation model. In this way, by means of a validated model, it will be possible to evaluate the losses in an optimized circuit. Simulation and experimental results are presented to validate the simulation approach.

Introduction

The high power density capability of Wide Band Gap (WBG) power devices with the potentially fast switching and low losses make them suitable for automotive applications where performance and low weight are keys for the development of more compact power converters. GaN power devices exhibit a better performance when compared with Si power devices thanks to their superior critical electric field and their high electron mobility in the 2DEG. This allows having lower parasitic capacitance values and therefore, high-speed commutation, in addition to having a lower on-resistance. However, these improvements bring new challenges when it comes to the loss measurements of the converters based on GaN material. A half bridge topology is thus developed including the measurement probes needed to evaluate the switching losses in a double pulse test. Furthermore, an evaluation of the parasitic elements of the PCB is considered.

The experimental results are used to validate the SPICE model and also for the loss estimation. Moreover, with the validated model, it will be possible to evaluate by simulation the losses in an optimized circuit without measurement probes [1, 2].

The development of a method that allows the estimation of switching losses is important for the design of converters. Also due to the fast switching, the effect of circuit parasitic elements is strongly important. For this reason, a good method used by converter designers is to analyse, by using simulations, the device switching behaviour under the influence of circuit parasitic elements before performing the physical circuit. This is especially helpful because it allows adjusting circuit layouts or comparing different layouts based on the simulation results [3–5].

GaN HEMTs 650 V Static Characteristics

The GaN device presents some particularities due to the fast switching capability. The transistor characteristics were measured with a Curve Tracer Keysight B1506a. In regard to the loss estimation and efficiency calculation, the I-V characteristics of the device need to be accurately measured. The linear mode for I-V graph is represented by the region when drain-source voltage is below the limit $V_{gs} - V_{th}$. We have to regard this region for a good estimation of the on-losses. At the moment that drain-source voltage is above $V_{gs} - V_{th}$, the curve represents the saturation region, being important for a good estimation of the switching losses [6–9].

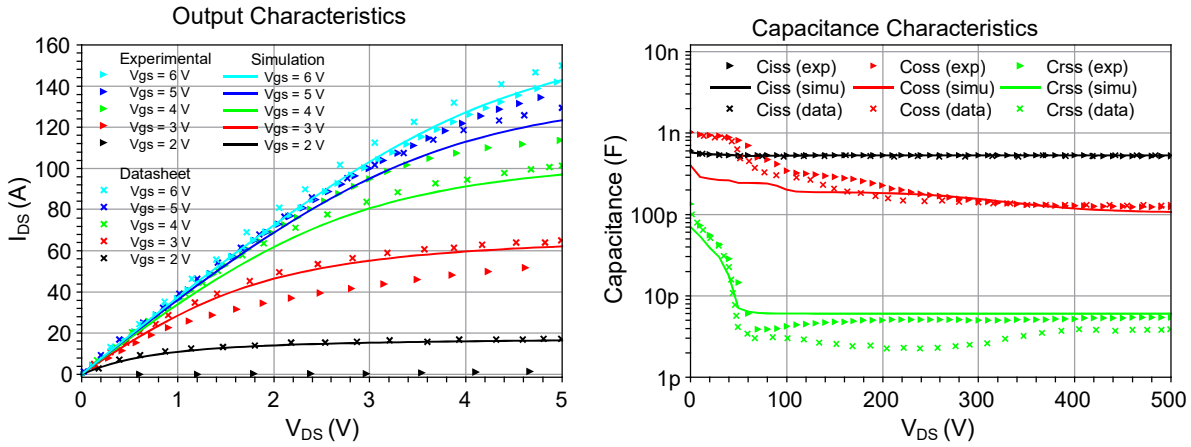


Fig. 1: Output characteristics for the GS66516B (a) and (b) input, output and reverse transfer capacitances.

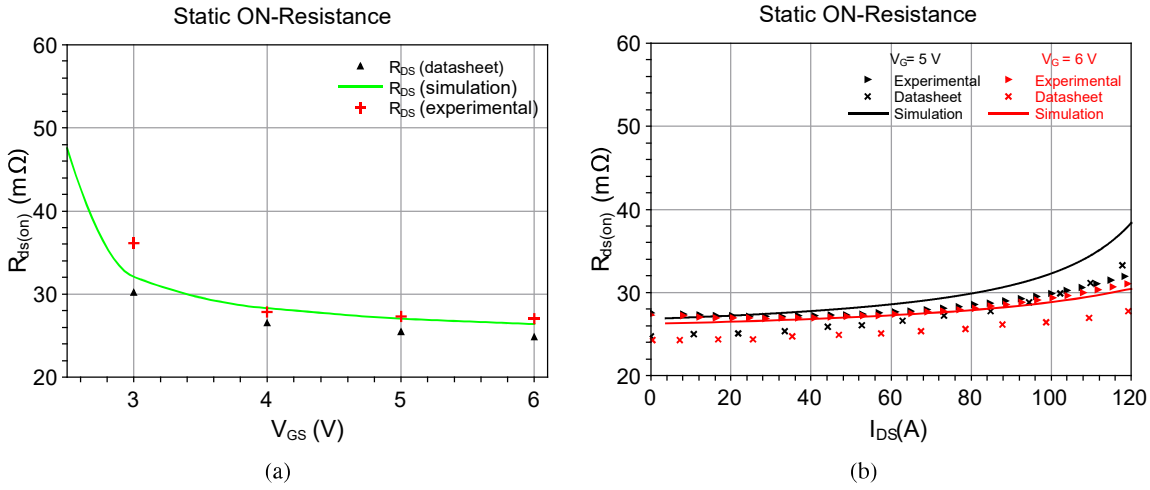


Fig. 2: (a) Static On-resistance and (b) its variation versus drain-source current.

Fig. 1(a) shows a comparison between measurements, datasheet values and the simulations obtained using the manufacturer model (LTspice). Some difference between experimental and simulation results can be noticed, which can be explained by components with different threshold voltages. These results show that some improvements in the default model are needed. The modelling of the input capacitance must be also precisely performed, since it determines the switching speed, influencing consequently the switching losses. The miller capacitance (C_{rss}) is the main component for cross conduction effect, as demonstrated in dynamic characterisation tests [1]. Fig. 1(b) shows a good correlation between

simulation and measurement results. This implies that for switching loss estimation the SPICE model presents a behaviour close to the real component. The on-state resistance can be read directly from the output characteristic curves and are presented in Fig. 2. Dispersion of V_{th} values could mainly explain the waveform variations found for the on-resistance.

Protocol Test

During measurements, it is noticed that the output characteristic for the GaN component was modified if a drain leakage current characteristic was measured just before the output characteristics. The leakage current test consists of a gate-source voltage applied to hold the switch turned-off (0 V, in this study). At the same time, a drain-source voltage is applied to slowly increase its value (up to 400 V). For example, Fig. 3 shows that the curve for the gate voltage equal to 2 V was significantly modified. This effect is due to the current collapse associated with the GaN components [10–13].

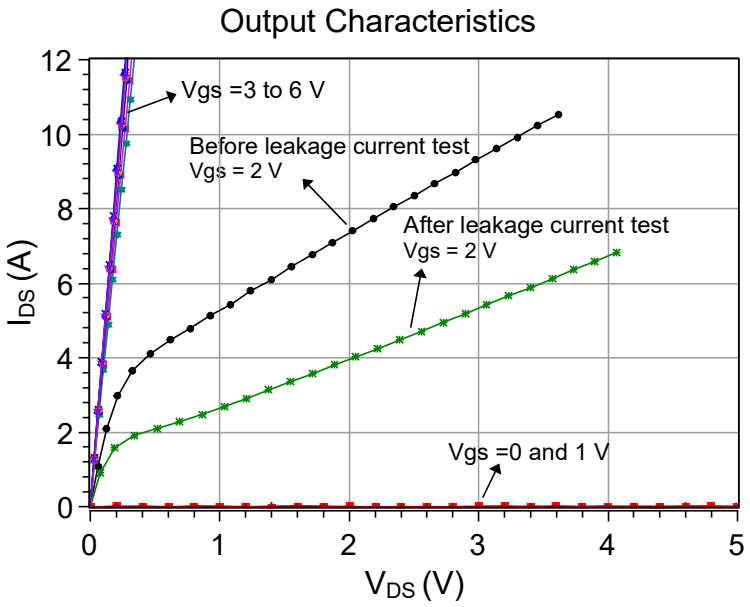


Fig. 3: Output Characteristics for GS66516B GaN Systems.

This is an important point that will be considered for the measurements. To avoid this phenomenon, our protocol includes a measurement of the transfer characteristics from -8 V to 4 V (gate-source voltage) just before performing the output characteristic test. The drain-source on-resistance is measured from the Fig. 3. Hence, at ambient temperature and before the drain leakage test it is found 22.3 mΩ. Thereafter, the on-resistance increases up to 23.5 mΩ.

GaN HEMT 650 V Dynamic Characteristic

Instrumented PCB Analyses

The developed PCB is instrumented to measure voltages (drain-source and gate-source) and currents (gate and drain-source) on the low side switch, as seen in Fig. 4. The command circuit is connected from another PCB, positioned ninety degrees in order to obtain the lowest coupling effect between the power and drive circuits. Furthermore, it is used a ground plane connected to the earth, in order to minimize the mutual inductance values. In the Table I, the measurement instruments are described.

The estimation of switching losses is performed considering three main elements on the spice simulation: the GaN component spice model, measurement instruments modelling and the parasitic elements from 3D wiring model. In Fig. 5(a) the circuit for the double-pulse test (DPT) and its measurement points. The 3D model seen in Fig. 5(b) is also developed in SpaceClaim and simulated on ANSYS Q3D to extract the RLC parasitic matrix.

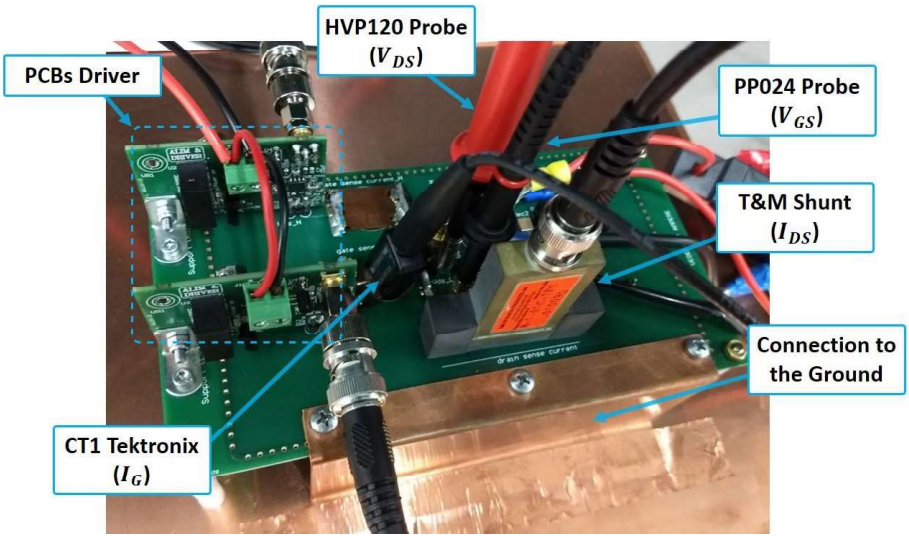
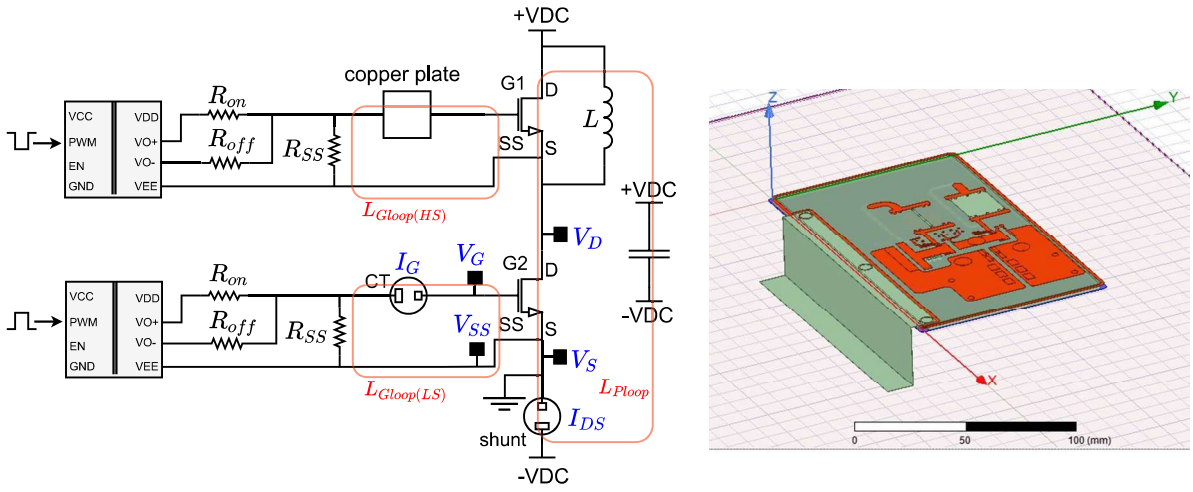


Fig. 4: PCB developed to the double pulse test with the GaN components behind the voltage probes.

Table I: List of measurement instruments used on this study.

Probe Reference	Manufacturer	Usage	Symbol
PP024	Lecroy	Gate-source voltage	V_{GS}
HVP120	Lecroy	Drain-source voltage	V_{DS}
W-1-01C-1FC	TandM Reasearch	Drain-source Current	I_{DS}
CT1	Tektronix	Gate current	I_G

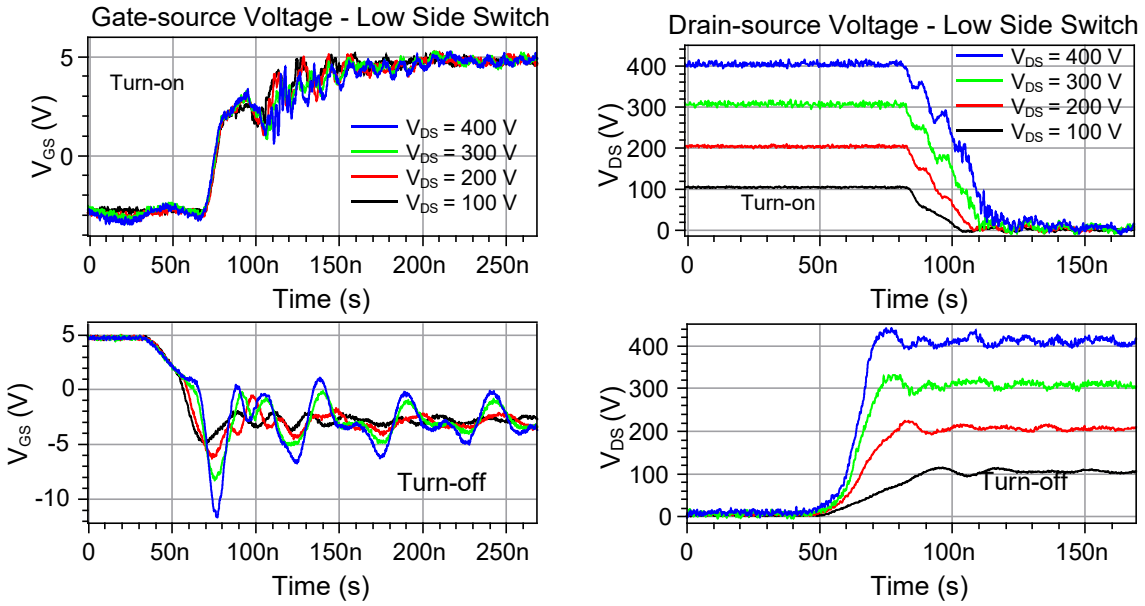


(a) (b)

Fig. 5: (a) Schematic showing all measurement points used to the tests. (b) 3D Model simulated on ANSYS Q3D.

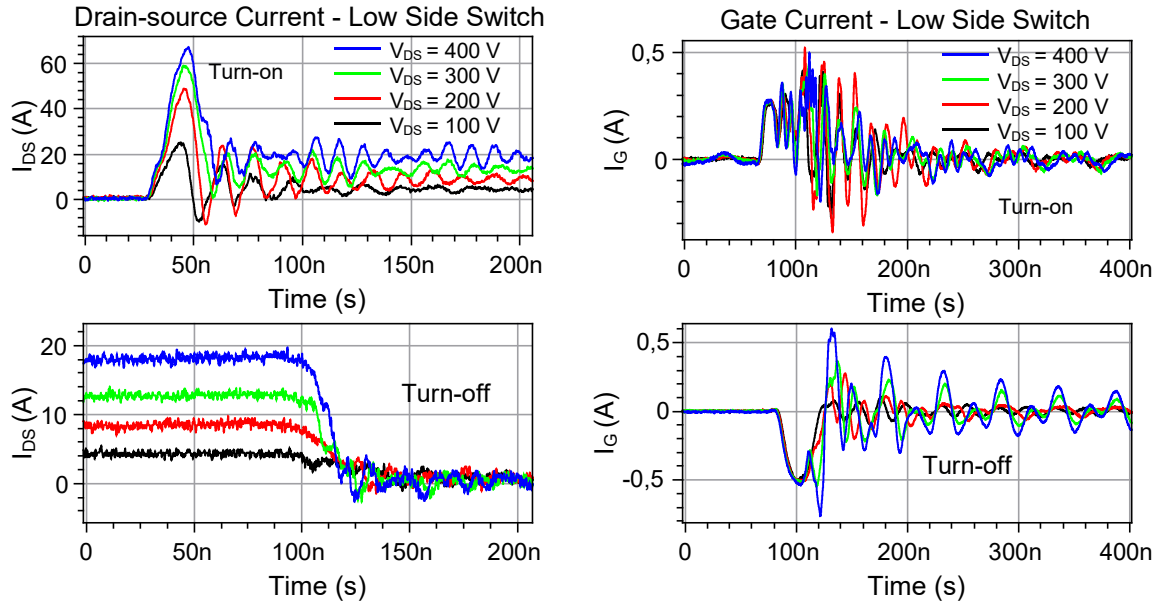
The modelling steps consist of characterizing the PCB without components, thus being able to analyse the parasitic elements associated to the switch, and then perform switching tests for different charge levels. In Fig. 6, the voltage waveforms of gate-source and drain-source on low side switch for different operation points can be seen. In Fig. 7, the current waveforms are shown. The correlation between the spike current and the drain-source voltage applied is clearly verified. The maximum steady drain current reached is about 19 A rated at 400 V. By means of the Fig. 7(a), it is possible to observe that the drain-source current shapes under different operation points are about the same, therefore it indicates that the

influencing of parasitic capacitors is not dependent on the operating point [3].



(a) (b)

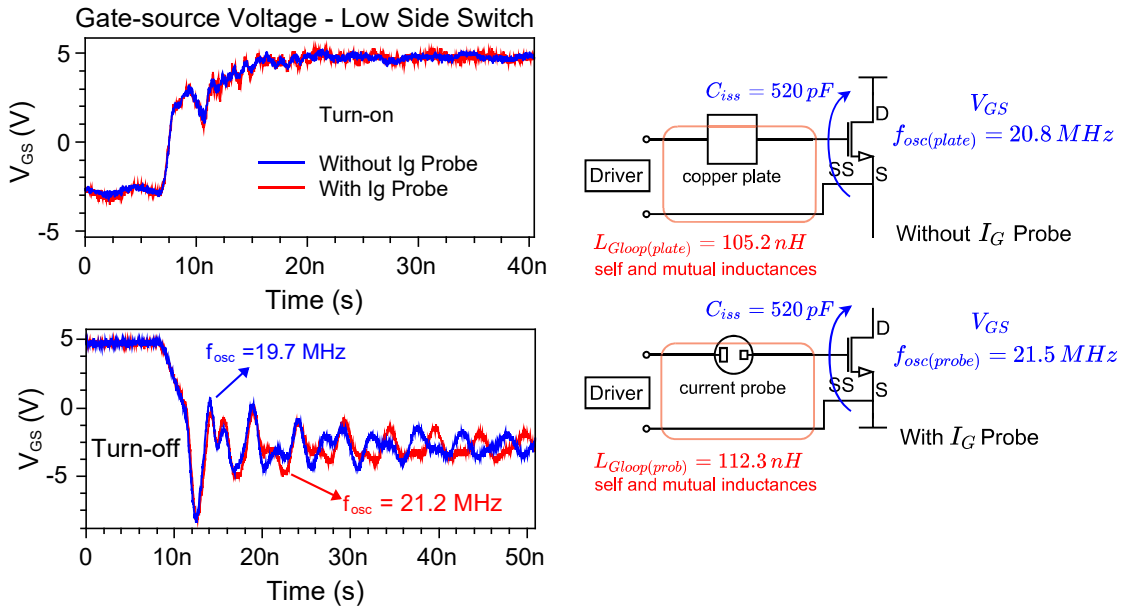
Fig. 6: Experimental results: (a) V_{GS} low side switch and (b) V_{DS} low side switch.



(a) (b)

Fig. 7: Experimental results: (a) I_{DS} low side switch and (b) I_G low side switch.

In Fig. 8(a) the effect of measuring the gate current can be seen. Some disturbances are detected, but the waveform remains nearly the same. The main oscillation frequencies obtained by FFT (Fast Fourier Transform) applied on measured V_{GS} indicates a resonance effect between the input capacitance of the switches and the gate loop inductance. In Fig. 8(b), the analytical calculus is performed to confirm this proposition. Therefore, by adding a probe current for I_G measurement the impact on signals is limited.



(a) (b)

Fig. 8: Experimental result: (a) Comparison of measured gate voltage V_{GS} considering the impact of using a current probe for I_G measurement. (b) Main oscillation frequency from V_{GS} for both cases: without I_G probe and with I_G probe. Test condition: 300 V and 12.6 A.

Analyses of Switching Losses on GaN HEMTs 650 V

In order to evaluate the switching losses in hard switching mode, the high side GaN is driven by a negative voltage (-3 V), thus behaving like a diode. The turning-on period starts with the charging time of the input capacitance (C_{iss}). When the V_{GS} reaches the threshold voltage, the low side switch can begin to conduct current. This phase is terminated when the drain current reaches the steady value for the inductor current. Right after, the drain-source voltage starts decreasing (period of voltage plateau), as long as the Miller capacitance (C_{rss}) is discharged. In addition, it is important to point out that there are parasitic effects which directly influence the oscillations detected during the switching [1, 14].

During the turning-on of a hard-switching, the effective current through the low side switch is a result of the sum of parasitic currents and the charge inductor current, as seen in Fig. 9(a), causing a spike current effect. The energy associated with the output capacitance of both switches (C_{oss}) and (C_{qoss}) is discharged towards the 2DEG channel of the low side switch. Furthermore, we should regard the PCB parasitic capacitance (C_{pcb}) and the intrinsic capacitance associated with the inductor (C_{pl}). Both elements generate high-frequency currents towards the low side switch and are not voltage-dependent. For the turning-off, the drain current is equal to the load current minus the currents related to the parasite capacitance values, as seen in Fig. 9(b) [3].

The loss estimation is performed by using four different simulations. The first one is a simple simulation which is considered the switch spice model (GS66516B), driver circuit, power loop inductance (L_{Ploop}), and the equivalent circuit (RLC) for the load inductor. For a second simulation, the measurement instrument models (voltage probe, shunt and current transformer) are considered in order to add the delay effect coming from the cable length and the disturbances associated to the impedance insertion. Afterwards, the gate loop parasitic inductance (L_{Gloop}, extracted by ANSYS Q3D) is added to the simulation. Finally, a simulation is performed by adding the full matrix Q3D (RLC) coupled with the electrical circuit of the instrumented PCB, including also the probe models.

In Fig. 10 and Fig. 11, the comparison between the performed simulations and the experimental data can be seen. Based on the results, it is reasonable considering the simulation which includes the power and

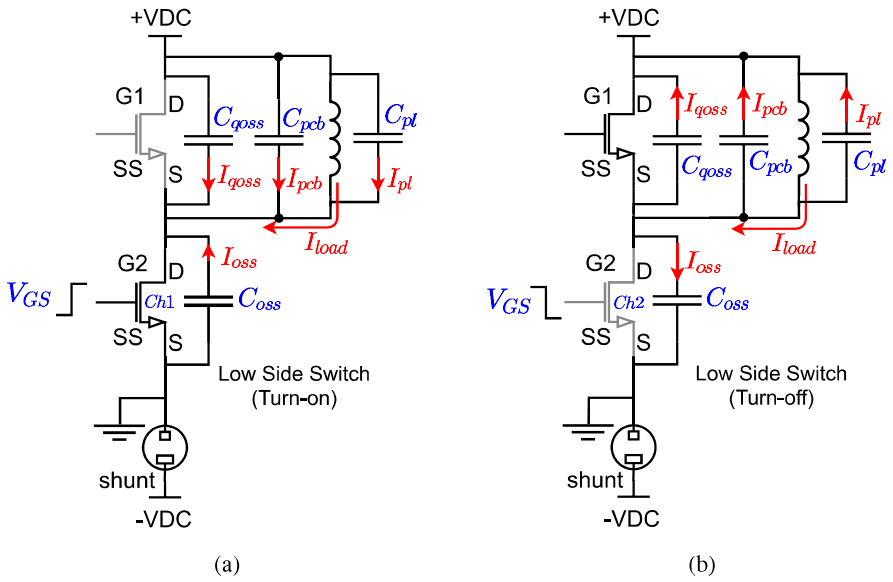
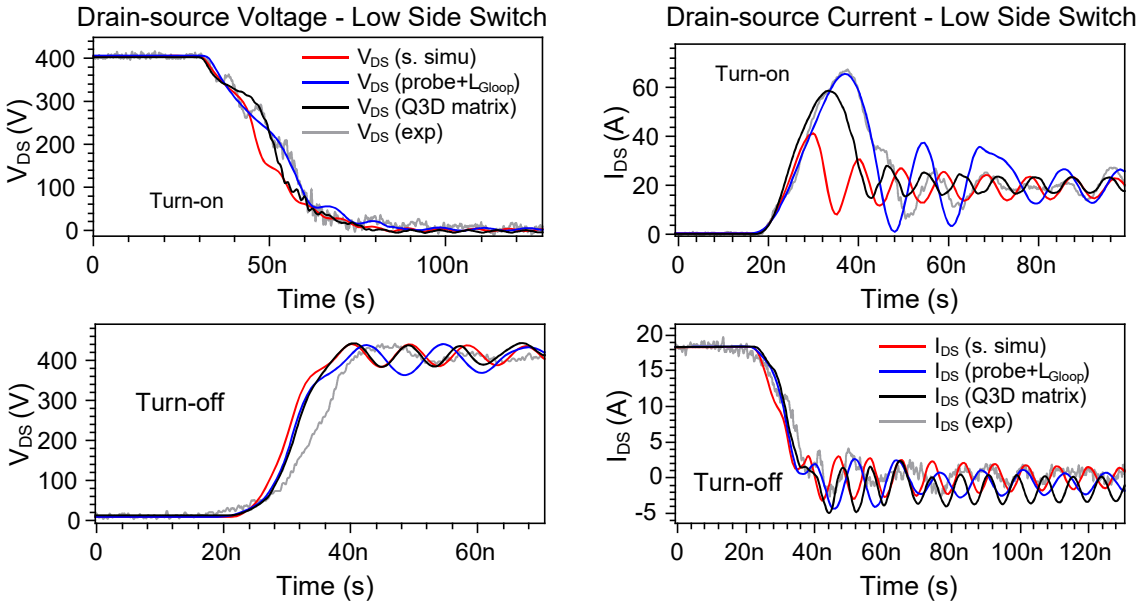


Fig. 9: (a) Current distribution at the moment of turning-on (low side switch). (b) Current on low side switch at turning-off.

gate loop inductances extracted by Q3D to calculate the switching losses. The modelling of parasitic elements and measurement instruments allows us to achieve a good correlation between simulation and experimental results, as seen in Fig. 11 by means of the curves overlay. In fact, the width of the power loss triangle increases with the power loop inductance. Moreover, the width and height of the power loss triangle also increase with the gate loop inductance of the high side switch. The delay added by the cable length of the measurement instruments and the disturbances found on the shape of the drain-source voltage are also strong elements that contribute to a good estimation of switching losses.



(a) (b)

Fig. 10: (a) Drain-source voltage comparison for simulation and experimental results. (b) Drain-source current comparison for simulation and experimental results.

The loss calculation is estimated using the signals from the switch terminal and the scope circuit, in

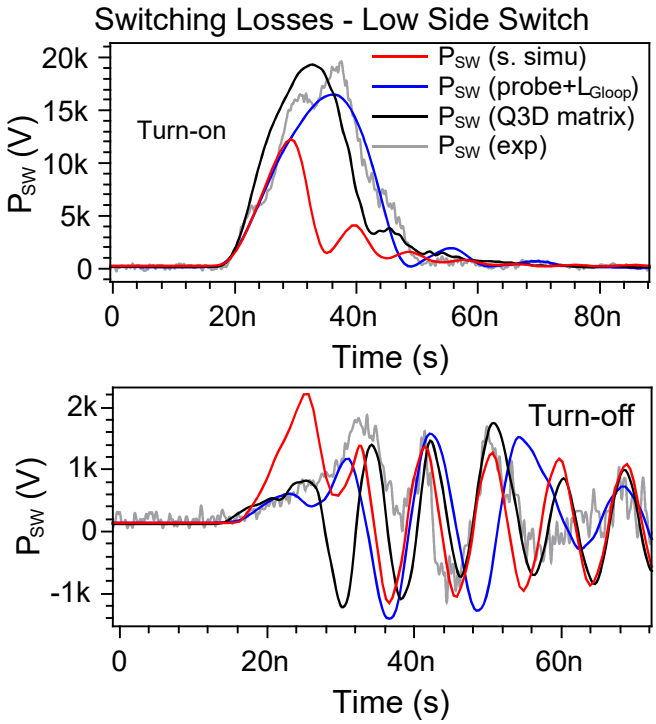


Fig. 11: Power switching loss for GS66516B GaN Systems on PCB instrumented.

order to compare the effect caused by the measurement instruments. For the experimental results, a new column (Delay Comp.) is calculated shifting the voltage signal at 4 ns towards the left of the time axis, implementing an advance on the signal. This value corresponds to the delay added by the cable models from the shunt and voltage probe. Some values of losses are shown in Table II and Table III for different operation points. It is possible to verify that by adding parasitic elements on the simple simulation, the difference between simulation and experimental values becomes smaller. By performing several measurements an uncertainty of 10% was detected on the values of switching losses. This is related to different integration points chosen for loss calculation, different voltages probes used, and the effect of measuring the gate current.

Table II: Switching loss energy of GS66516B for turning-on.

Operation Points (V | A)	Turn-on (μJ)								
	Simple Simulation	Probe Models		Adding L_{Gloop}		With Full Q3D		Experimental	
		Switch	Scope	Switch	Scope	Switch	Scope	Delay Comp.	Scope
100 | 4.3	7.2	6.5	10.3	7.8	13.2	9.4	14.4	10.1	15.2
200 | 8.5	29.1	26.4	39.5	42.2	62.4	49.9	68.7	51.6	71.6
300 | 12.6	65.8	65.1	89.5	113.2	158.6	128.2	160.2	136.5	171.8
400 | 18.3	126.3	127.5	170.5	228.2	285.2	232.7	284.2	261.8	314.7

Table III: Switching loss energy of GS66516B for turning-off.

Operation Points (V | A)	Turn-off (μJ)								
	Simple Simulation	Probe Models		Adding L_{Gloop}		With Full Q3D		Experimental	
		Switch	Scope	Switch	Scope	Switch	Scope	Delay Comp.	Scope
100 | 4.3	2.5	3.6	1.8	1.9	1.2	2.7	1.5	7.47	4.5
200 | 8.5	6.7	6.5	2.5	6.9	2.8	6.2	3.2	13.3	9.5
300 | 12.6	10.8	11.0	2.9	12.3	4.4	11.5	3.7	20.2	11.8
400 | 18.3	14.9	15.7	4.1	20.1	6.3	16.5	5.2	36.8	19.9

It is important to highlight that the oscillations on current waveforms are due to the parasitic elements and

does not affect the integral loss calculation, once the average value of the high frequency of oscillation is almost zero after integration. It can be also noticed that only with the power and gate loop inductances (L_{PLoop} and L_{GLoop}) extracted by ANSYS Q3D and with the instrument measurement models, the divergence between the theoretical values and measured values are relatively small.

Conclusion

The comprehensive analysis of the impact of the wiring parasitic elements can improve the accuracy of switching loss estimation. Furthermore, by means of experimental results the need of a good modelling of instrument measurements and a 3D Model for parasitic extraction is verified. A simulation considering the power and gate loop inductances can yield a good match with experimental data. This approach allows us to validate all models used in spice simulations, and thus to be able to evaluate more accurately the overall efficiency of converters based on GaN components, even those that will be not instrumented.

References

[1] Zheng Chen. *Characterization and modeling of high-switching-speed behavior of SiC active devices*. PhD thesis, Virginia Tech, 2009.

[2] Xiao Shan Liu, Bertrand Revol, and François Costa. Parasitic elements modeling and experimental identification in a GaN HEMT based power module. In *19 ème Colloque International et Exposition sur la Compatibilité ÉlectroMagnétique (CEM 2018)*, 2018.

[3] Ruoyu Hou, Juncheng Lu, and Di Chen. Parasitic capacitance Eqoss loss mechanism, calculation, and measurement in hard-switching for GaN-HEMTs. In *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 919–924. IEEE, 2018.

[4] Olivier Goualard. *Utilisation de semi-conducteurs GaN basse tension pour l'intégration des convertisseurs d'énergie électrique dans le domaine aéronautique*. PhD thesis, 2016.

[5] Fadi Nader Fouad Zaki. *Characterization, modeling and aging behavior of GaN power transistors*. PhD thesis, Université Paris-Saclay, 2018.

[6] Perrin Rémi. *Characterization and design of high-switching speed capability of GaN power devices in a 3-phase inverter*. PhD thesis, Lyon, 2018.

[7] Juncheng Lucas Lu and Di Chen. Paralleling GaN E-HEMTs in 10kW-100kW systems. *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pages 3049–3056, 2017.

[8] Ke LI. *Wide Bandgap (SiC/GaN) Power Devices Characterization and Modeling: Application to HF Power Converters*. PhD thesis, Lille, 2014.

[9] Guillaume Regnat. *Onduleur à forte intégration utilisant des semi-conducteurs à grand gap*. PhD thesis, Grenoble, 2016.

[10] Gaudenzio Meneghesso, Fabiana Rampazzo, Peter Kordos, Giovanni Verzellesi, and Enrico Zanoni. Current collapse and high-electric-field reliability of unpassivated GaN/AlGaN/GaN-HEMTs. *IEEE Transactions on Electron Devices*, 53(12):2932–2941, 2006.

[11] Zhikai Tang, Qimeng Jiang, Yunyou Lu, Sen Huang, Shu Yang, Xi Tang, and Kevin J Chen. 600-v normally off SiNx/AlGaN/GaN MIS-HEMT with large gate swing and low current collapse. *IEEE Electron Device Letters*, 34(11):1373–1375, 2013.

[12] Donghyun Jin. *Dynamic ON-resistance in high voltage GaN field-effect-transistors*. PhD thesis, Massachusetts Institute of Technology, 2014.

[13] Ke Li, Paul Evans, and Mark Johnson. GaN-HEMT dynamic ON-state resistance characterisation and modelling. In *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–7. IEEE, 2016.

[14] Zheyu Zhang, Ben Guo, Fei Fred Wang, Edward A. Jones, Leon M. Tolbert, and Benjamin J. Blalock. Methodology for Wide Band-Gap Device Dynamic Characterization. *IEEE Transactions on Power Electronics*, 32(12):9307–9318, 2017.