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Analysis of Parasitic Elements in Power Modules Based on GaN Components

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Abstract

This paper aims to evaluate a GaN based power module for automotive applications. Simulations and experiments were then performed on a classical double pulse test bench. In regard to EMC, the oscillations on the Vds after device turn-off is quite important. The comparison between a simulation without considering the 3D wiring model and a simulation by considering the wiring elements is presented. The impact of the parasitic elements modelling is seen through the resonance frequencies found. Experimental results of operation of the converter are presented to validate the simulation approach.

1 Introduction

The need to increase power electronic performances has motivated the development of new researches on semiconductor devices, such as GaN-HEMT switches. They are promising components for fast switching, high efficiency and thus high power density power module design [1]. However, as the wide-band gap devices have a high switching speed, combined with parasitic inductive and capacitive elements of the power module, which yields to electromagnetic perturbations [2], [3]. Great efforts have been devoted to the developments of modules based in GaN for medium-voltage switching applications because of their much lower specific on-resistance with respect to voltage breakdown when compared with Si-MOSFETs, their higher switching speed than Si-IGBTs, and their high temperature operation capability.

2 Simulation and Comparison With Double Pulse Test Results

The evaluation plate that we used, consists of a motherboard and an IMS evaluation module. The configuration implemented was a one leg inverter for double pulse tests realization. For all tests we

use a switching frequency of 100 kHz. Several double pulse tests based on GS66516B under different load currents were performed. To realize the measurements, we use the differential ISOVU probe TIVH08/TIVH08L with a bandwidth equal to 800 MHz. That probe was used due to the high frequency of oscillation seen on GaN components, so with a normal differential probe some frequencies are hidden.

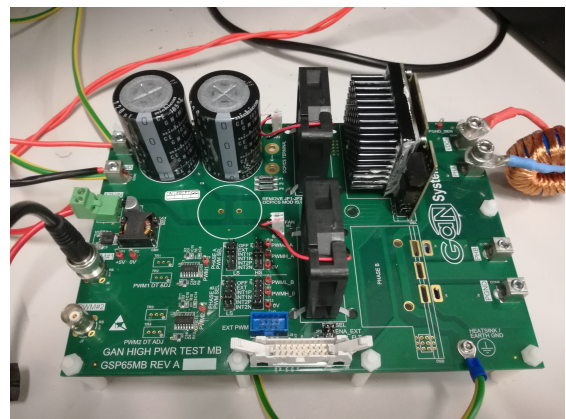
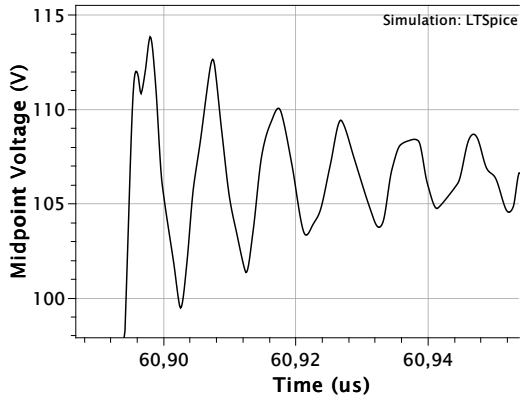


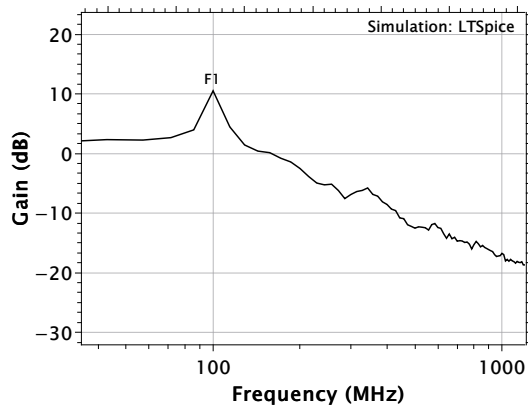
Fig. 1: Evaluation board from GaN Systems.

2.1 Operation Point: 100 V and 35 A

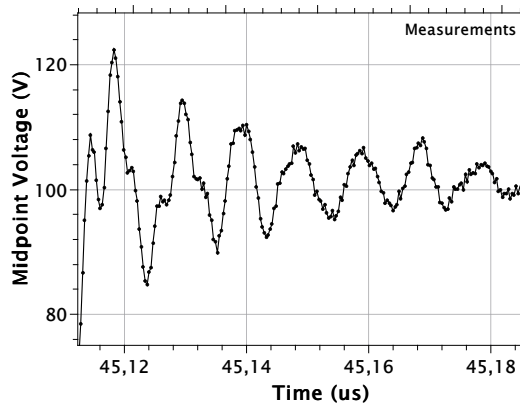
As can be seen in the Fig. 2, a good correlation is seen between the simulation and the test results.



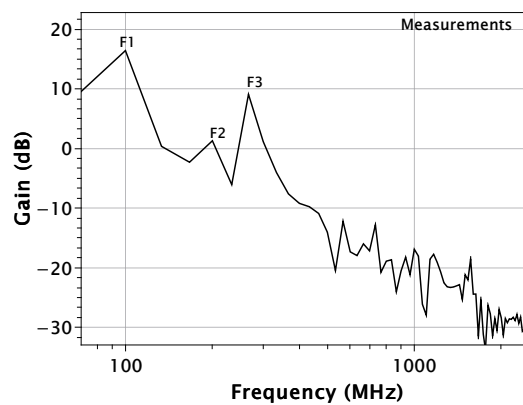
(a)



(b)



(c)



(d)

Fig. 2: Condition test: 100 V and 35 A. (a) Midpoint voltage from simulation and (b) its FFT. (c) The voltage on the midpoint from measurement results and (d) its FFT from the measurement results.

The frequency 100 MHz is seen on the simulation and with the ISOVU probe, but additional ringing frequencies are present, but not on the simulation. This is the first evidence about the parasitic elements due to PCB tracks.

Tab. 1: Comparison between simulated and measurement results under condition: 100 V and 35 A.

Parameters:	LTSpice	ISOVU Probe
Overshooting (V)	114	122
Rise time (ns)	6.4	6.8
Freq. 1 (MHz)	100	100
Freq. 2 (MHz)	---	199
Freq. 3 (MHz)	---	267

2.2 Operation point: 400 V and 41 A

As can be seen on the simulation and test results of Fig. 2 and 3, after the switch turn-off, there is an oscillation at the frequency $1/(2\pi\sqrt{LC})$ between the output capacitor of the switch ($2 \times 300 \text{ pF}@100\text{V}$ and $2 \times 150 \text{ pF}@400\text{V}$) and the parasitic inductance. This oscillation at the frequency $1/(2\pi\sqrt{LC})$ is a well-known effect and is for example presented with GaN in the following paper [3]. In the LTSpice simulation, the parasitic power loop inductance was adjusted at 100 V in order to have the measurement and simulation first frequency matching at 100 MHz. Without having to readjust the parasitic inductance value ($L = 4.1 \text{ nH}$), we also obtained matching frequency for simulation and tests at 400 V, around 140 – 150 MHz. It is also to note that the LTSpice simulation shows an exponential decrease of the oscillation while the measurements of Fig. 3 do not show an exponential decrease.

Tab. 2: Comparison between simulated and measurement results under condition: 400 V and 41 A.

Parameters:	LTSpice	ISOVU Probe
Overshooting (V)	425	438
Rise time (ns)	7.7	11.4
Freq. 1 (MHz)	146	144
Freq. 2 (MHz)	---	223
Freq. 3 (MHz)	---	---

Based on the results achieved, we can conclude that for higher oscillation frequencies, it is noticed a considerable gap between their values and amplitudes. Therefore, it is necessary to add lower capacitances and inductances in the simulation to achieve accurate oscillations simulations at higher frequencies.

3 3D Model of the Power Loop Inside the Simulation

As the voltage and current increase, the parasitic effects become more evident and new oscillation frequencies can be seen. In order to understand the measurement of oscillations containing multiple frequencies, it was decided to include a 3D model of the power loop inside the LTSpice simulation. The power module is modelled with ANSYS SpaceClaim and then the Q3D Extractor is used to extract of the parasitic elements [3].

For modelling of the power module, some considerations should be given. Initially, the geometry is built on SpaceClaim and then exported to Q3D Extractor. Before running the simulation, it is mandatory to check if there are some contacts between the objects of the 3D model. All intersections must be eliminated. Another important point is the definition of the NETs (region with the same electrical potential). Regions simpler implies to a mesh operation easier, therefore with fewer possibilities of error for the simulation. It is also necessary to define the frequency where we only have surface currents on the device. For this case, it is used 150 MHz.

When using Q3D simulation in LTSpice, PCB trace modelling allows us to see higher frequencies on switching waveforms. This is very important for switching loss estimation and knowing where the design of the converter should be improved [4].

3.1 Operation point: 400 V and 71 A

It is important to emphasize the variation of the midpoint voltage waveforms between 41 A and 71 A operation, as seen in Fig. 3 and 4.

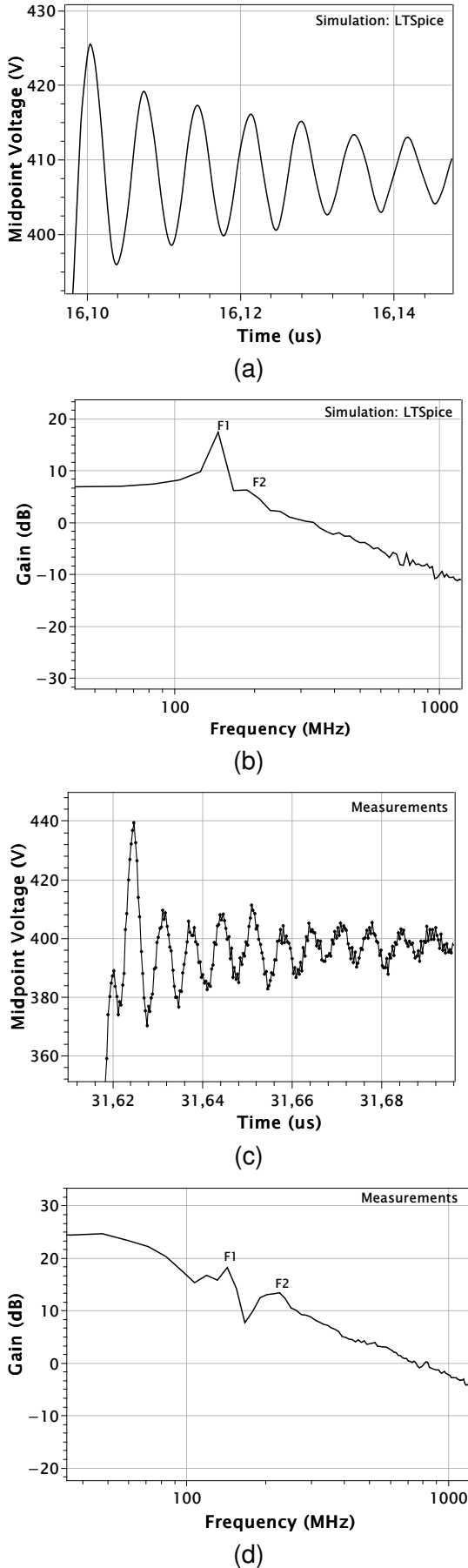


Fig. 3: Condition test: 400 V and 41 A. (a) Midpoint voltage from simulation and (b) its FFT. (c) The voltage on the midpoint from measurement results and (d) its FFT from the measurement results.

Tab. 3: Comparison between simulated and measurement results under condition: 400 V and 71 A.

Parameters:	LTSpice + Q3D	ISOVU Probe
Overshooting (V)	454	426
Rise time (ns)	6.7	8.7
Freq. 1 (MHz)	98	108
Freq. 2 (MHz)	157	146
Freq. 3 (MHz)	275	272

The simulation (LTSpice with Q3D) and the test results show similar behavior with a none monotonous decrease of the oscillation amplitude. This can be explained by the mutual inductance effect and

the accurate calculation of parasitic elements performed by the 3D Model. Stray impedances are extracted by using Q3D extractor providing RLC elements with the same solver by combining finite element method and the method of moments. Moreover, we can note a good frequency match for the operation points evaluated.

The differences found in the switching frequencies for different level currents at the same voltage can be related to the mutual inductances effect. When we increase the current level that crosses a track, the mutual inductance effect on another conductor is more intense. The strong voltage overshoot value is related to the power commutation loop, as well as the distance between the decoupling capacitors and the IMS power module. The ideal case would be to use the capacitors as close as possible to the switches [5].

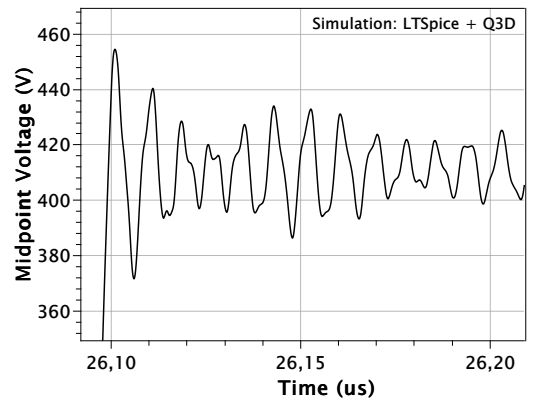
4 Parasitic Analysis

The modelling of partial inductances is based on 3D model of the power module, on different current paths defined by the position of the Q3D excitation, and on the distance between conductors due the coupling effect [6]. In Fig. 5, we can see the modelling of the power module performed on SpaceClaim and Q3D. The system is composed of three main parts: PCB driver, IMS power and a heat sink.

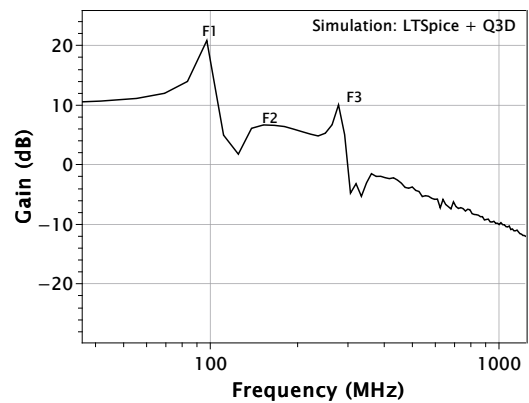
Parasitic capacitance is another point very important to PCB design. The voltage applied on the switches increases, the output capacitance decreases, therefore it is possible to observe higher oscillation frequencies. The common mode capacitances have influences from a frequency of 200 MHz, and this is seen by the values from the capacitance matrix generated by Q3D.

To analyse the role of the parasitic elements, we had tried to analyse for instance the impact of the layout between the middle point and the drain of the low-side switch, Fig. 6.

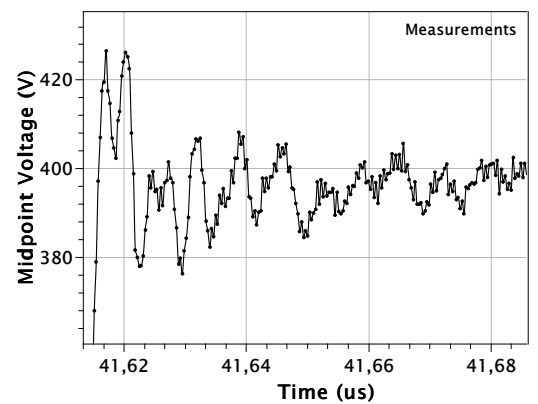
In Fig. 7, it is possible to see the coupling at 100 MHz due the power loop inductance and the equivalent output capacitance, as well as the parasitic elements associated. Similarly, in Fig. 8 we can see that the coupling for a frequency of 280 MHz is due a resonance between the equivalent inductance $L_{eq} = 9.1$ nH on the drain low side switch and



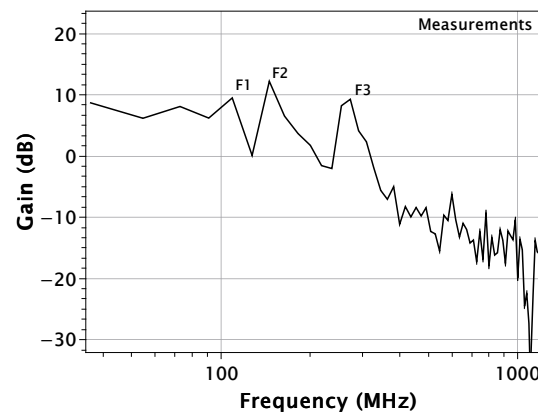
(a)



(b)



(c)



(d)

Fig. 4: Condition test: 400 V and 71 A. (a) Midpoint voltage from simulation and (b) its FFT. (c) The voltage on the midpoint from measurement results and (d) its FFT from the measurement results.

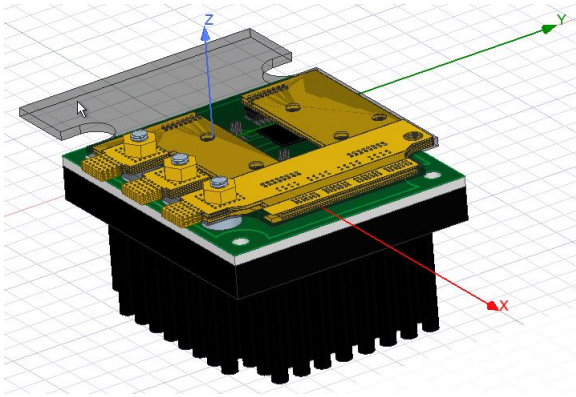


Fig. 5: GaN System power module in Q3D Extractor.

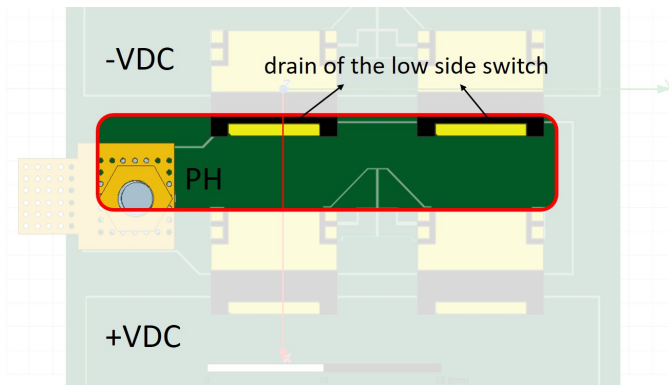


Fig. 6: IMS layout between the middle point and the drain of the low side switch.

the parasitic capacitances. In this case, the equivalent inductance is calculated considering the self and mutual inductances on the power commutation loop. Also, the capacitance of only one switch is considered to explain the 280 MHz frequency. It is possible because when we have a high current level, the unbalanced current becomes more evident [7].

In Fig. 9, by the simulation we can see that the equivalent inductance adjusts the source drain voltage (V_{ds}) to match the middle point voltage waveform (V_{ph}). These components are directly linked to the paths of disturbances in common mode, therefore the modelling of these components is essential in the prediction of voltage disturbances [8]. The influence of the parasitic element L_{eq} can be demonstrated using a superposition of voltage waveforms, Eq. (1).

$$V_{ph-calc} = V_{ds} + L_{eq} \frac{dI_d}{dt} \quad (1)$$

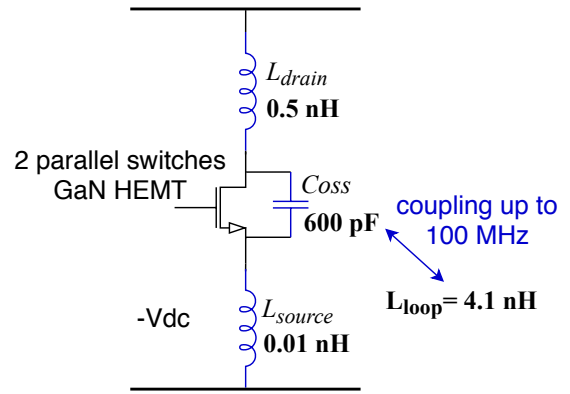


Fig. 7: Electric diagram of the resonant loop to the frequency at 100 MHz.

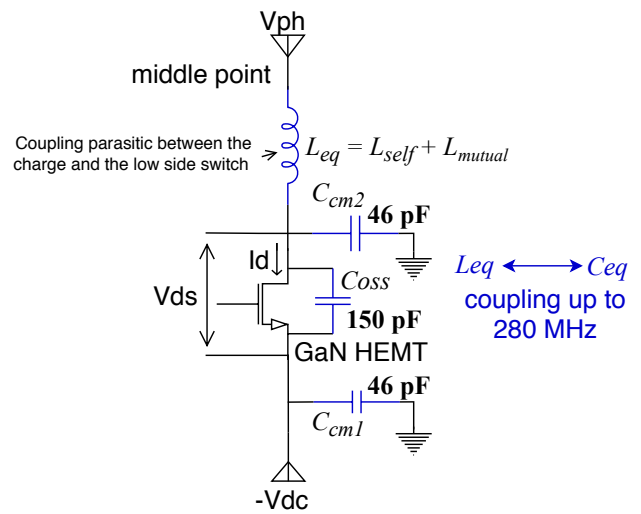


Fig. 8: Electric diagram of the low side switch and parasitic elements associated.

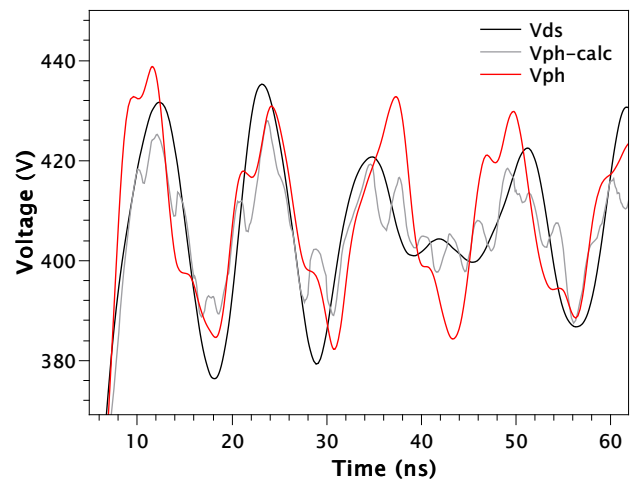


Fig. 9: Comparison between drain-source voltage (V_{ds}), middle point voltage (V_{ph}) and its calculated value ($V_{ph-calc}$).

5 Conclusion

This paper presents an approach for the evaluation of the parasitic elements of the PCB. The base principle is to regard the three main resonant frequencies in the voltage waveforms of the middle point and drain-source. Good results have been found by simulation. The values of the estimated elements have been compared to the ones extracted by a numerical tool. Clearly the use of a 3D model for extraction of the parasitic elements improves the simulation and measurements fitting.

The analysis of the electromagnetic disturbance is easier in the frequency domain than in the time domain. In the frequency domain it is easier to see which frequency bands have more contribution to the source of electromagnetic disturbance and thus to determine a solution to reduce the disturbances.

To further investigate the concept of the parasitic elements on converters based GaN components, the authors are working on an instrumented PCB that will be able to perform impedance measurements, a better 3D modelling and voltage measurements, in order to validate the Q3D model parasitic. The analysis of the role of the parasitic elements need a strong effort to analyse and optimise the layout of the circuit. This will be achieved in a future study.

6 References

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