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Abstract

This paper investigates the gate-driver design challenges encountered due to the fast switching of wide band-gap semiconductors (here, SiC MOSFETs) in the half-bridge configuration. It discusses precisely the common-mode current generated by fast switching passing through gate-driver, which leads to driving-voltage perturbations and disturbs the correct triggering of switches. This phenomenon is described here as self-disturbance and the experimental study shows that it is exacerbated with SiC MOSFETs, when compared with Si IGBTs. The solution proposed in this article is to block the generated noise linked to self-disturbance phenomenon by placing a common-mode choke into the gate path. The proposed solution is compared with the classical active Miller-clamp protection solution. The experimental results from 1.7kV, 300A SiC MOSFET validate the solution. The solution proposed in this work allows to keep the MOSFET gate-voltage perturbation lower than the MOSFET threshold voltage while it does not increase the switching losses. Experimental results show that by implementing the proposed solution, it is possible to reduce the input common-mode current through the gate driver by up to 20%.

1 Introduction

An important objective when designing a power converter is high efficiency. That is why, due to their lower switching losses, SiC MOSFETs became an alternative to silicon IGBTs [1], [2]. In spite of the advantages of the high switching speed including reducing the dead time in a phase-leg configuration and increasing switching frequency [1], [3], it adds difficulties to gate driver design [4], [5]. By increasing the switching speed to obtain minimum switching losses, converter parasitic elements are subject to large dv/dt and di/dt values which can generate disturbances. In a half-bridge configuration, during switching transient, each switch affects the operating of the complementary switch. The fast variation of the voltage across a switch in a half-bridge produces an unavoidable perturbation on the control voltage of the complementary switch due to parasitic elements. In addition, since gate driver acts as an interface between a switch and a control circuit, common-mode current generated by fast switching passes through the gate driver isolation [6] and can disturb the controller of the converter. Therefore, the main objective of this work is to keep the switching speed as high as possible while dealing with the generated disturbances.

The paper is organized as follow. Section 2 explains the experimental set-up used in this work to investigate the problem and validate the solution. Section 3 explains the mechanism of the voltage perturbation in the gate which is called in this work ”self-disturbance” phenomenon. Section 4 compares experimentally the difference between IGBTs and SiC MOSFETs which highlights the causes of self-disturbance phenomenon. The typical solution to reduce the voltage perturbation is discussed in section 5. The proposed solution and conclusion are presented in sections 6 and 7 respectively.

2 Experimental platform

To investigate the self-disturbance phenomenon, the experimental study of switching characteristics has been carried out on a full-bridge double-pulse test bench (see Fig. 1). In this test bench, by turning on and off switch 1 or switch 2 (see Fig. 2), it is possible to control the direction of the current through the inductor. Double pulse test with both current directions enable to characterize the high-side and low-side switch of the half-bridge under test (DUT) in soft switching and hard switching which is the natural switching behaviour of a half-bridge configuration (see figures 1 and 2).

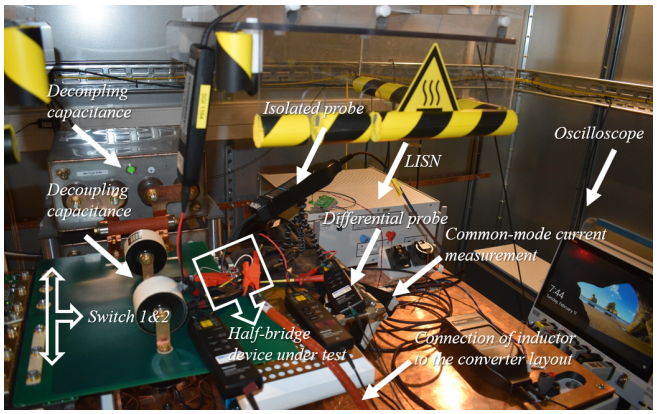


Fig. 1: Experimental set-up.

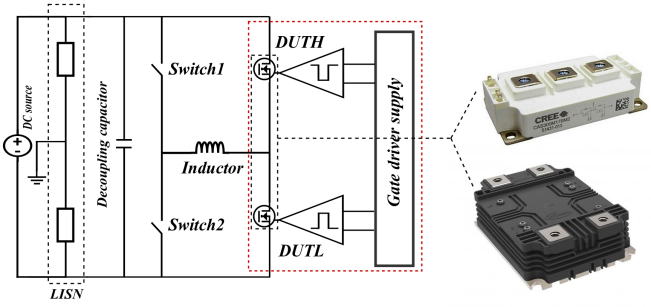


Fig. 2: Experimental set-up schematic.

3 Problem statement

During turn-on transient of the lower switch, the increasing voltage across the upper switch creates an increasing voltage across the Miller capacitance of the semiconductor (C_{dg}). This rising voltage induces a current going to the gate loop and introduces a positive voltage perturbation (see Fig. 3). If this parasitic voltage exceeds the threshold

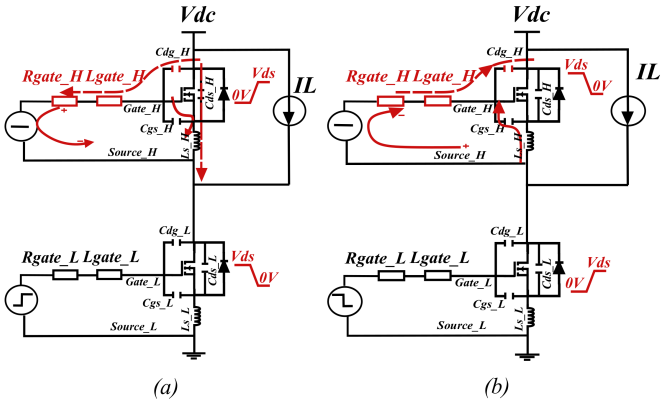


Fig. 3: Gate voltage perturbation mechanism (a) Positive perturbation during turn-on (b) Negative perturbation during turn-off.

voltage (V_{th}) of the switch, it can partially or fully turn-on the device. The partially turn-on results in a shoot-through current leading to additional losses in both switches and potential circuit oscillation [7]. In case of fully turn-on of the switch, a short-circuit happens due to the simultaneous conduction of both switches of the half-bridge which can destroy the semiconductors [8].

Similar to turn-on transition, during turn-off transition of the lower switch, the decreasing voltage across the upper switch coupled to the Miller capacitance and due to the parasitic elements of the gate, creates a negative parasitic voltage across the gate of the switch. If this negative voltage exceeds the maximum allowable negative gate bias of the switch, it can over stress the device and degrade the switch stability [9].

It is noteworthy that the low-side switch is subject to the same phenomenon. This means that, during the turn-off and turn-on of the upper switch, a parasitic voltage appears in the gate of the low-side switch. The presented results here are dedicated to high-side switch due to space limitation but the same analysis can be applied to the lower switch also.

This positive and negative parasitic voltage due to complementary switching transient in half-bridge configuration is called ”self-disturbance phenomenon” in this work since it can disturb the normal operation of the switches and consequently can disturb the converter. This phenomenon has been called in many dissertations ”cross-talk”, ”self-turn-on”, ”false turn-on”, ”false triggering”, etc. The

mechanism of this induced voltage on the gate voltage has been studied in [10]–[13]. Analytical investigation of the circuit during turn-on and turn-off showed that the maximum gate voltage perturbation given by (Eq. 1) [7]. where (see Fig. 3) the dv/dt is the slew rate of the voltage across the switch, C_{iss} is the input capacitance of the DUT, C_{dg} is the Miller capacitance of the DUT and R_{gate_H} is the gate resistance.

$$V_{gs_H}(max) = \frac{dv}{dt} R_{gate\_H} C_{dg\_H} \left(1 - e^{\frac{V_{DC}}{\frac{dv}{dt} C_{iss} R_{gate\_H}}}\right) \quad (1)$$

Based on the figure 3 and equation 1, it can be concluded that the voltage perturbations mainly depend on the voltage variation and the value of the junction capacitances. The impedance of the gate path is an unavoidable factor in the design of the gate driver which has to be minimized. As IGBTs and MOSFETs show up with very different characteristics (e.g. C_{dg} and C_{iss}), for the development of the SiC MOSFET gate drivers, it is necessary to consider the difference between SiC MOSFETs and IGBTs and to focus on the main challenge: self-disturbance.

Tab. 1: Electrical characteristic of the considered MOSFET and IGBT module

Parameter	Unit	SI IGBT	SiC MOSFET
Vth	V	5.2	2.5
Ciss	nF	84	20
Coss	nF	3.5	2.5
Crss (Cdg)	nF	2	0.08
Qg	μC	12.5	0.273
Qrr	μC	230	324
Rint	Ω	1.3	3.7

4 Experimental comparison of SiC MOSFETs and IGBTs power modules

To show the difference between modules based on SiC MOSFETs and IGBTs, a Wolfspeed SiC MOSFET CAS300M17BM2 package (1.7kV, 300A) and an Infineon IGBT FF450R33T3E3, XHP3

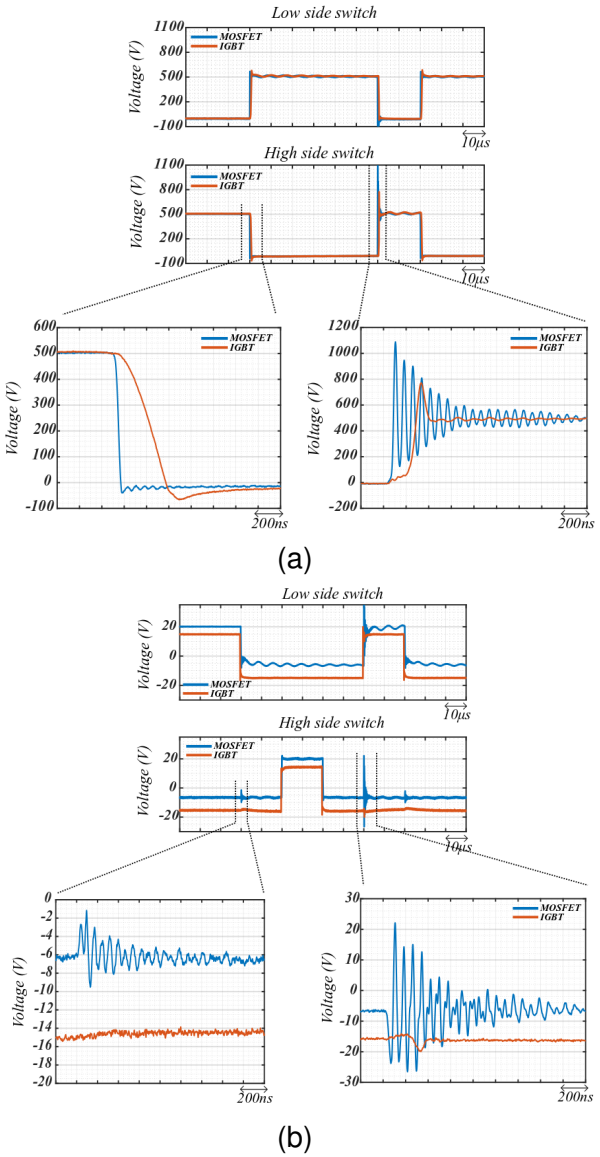


Fig. 4: Experimental results of comparison between the IGBT and SiC MOSFET in 500V, 150A double pulse test (a) Drain-source voltage (b) Gate-source voltage.

package (3.3kV, 450A) have been compared experimentally. Table 1 outlines the main differences between the two devices in terms of junction capacitance, input resistance and threshold voltage. Considering Fig. 3, which shows the elements related to the gate perturbation, in order to keep the effect of the gate impedance constant between both tests, the same gate driver has been used for both devices. L_{gate_H} is unavoidable in the design of the gate driver, due to the connection of the gate driver and the parasitic impedance of the electronic board. Therefore, the same gate driver in the same converter layout has been used for

both DUTs in order to have a fair comparison. The external gate resistance of gate driver has been fixed to 0.2Ω for both cases. The only difference is the driver power supply. The SiC MOSFET gate is regulated between -6 and 20 volts while the IGBT is biased between -15 to 15 volts.

The experimental results shown in figure 4 prove that almost 4 times faster switching speed of the SiC MOSFET compared to IGBT module causes a higher gate voltage perturbation even if the value of the junction capacitance is lower. The significant gate voltage perturbation prevents to test the MOSFET at voltages higher than 500V while this power module is expected to be used in application with DC voltages of up to 1200V. Therefore, in a half-bridge configuration, in order to fully benefit from the potential advantage of fast switching rate of SiC MOSFET and guarantee the proper operation of the power devices, self-disturbance phenomena should be suppressed. For IGBTs, the perturbation is lower and the bigger negative bias reduces the risk of short-through in a half-bridge configuration. That is the reason why the investigation is continued for SiC MOSFETs only.

5 Miller-clamp protection

As it has been shown in section 4, switching speed is the key contributor to self-disturbance phenomenon. Therefore, slowing down the dv/dt can reduce the perturbation in the gate voltage. This is obtained by prolonging the charging of the input capacitances of the device [14]–[16]. Decreasing the switching speed comes with the penalty of increasing losses which is in contrary with the goal of using SiC MOSFETs. There are several works that present the reduction of the self-disturbance phenomena by taking advantage of negative biasing ability of the SiC MOSFETs [8], [17]. In order to reduce the self-disturbance with minimum effect on the switching speed, these methods try to control the gate signal thanks to passive components. In general, they are called "passive methods". However, the passive methods are able to suppress only the positive voltage perturbation [8], [17].

Another category of solutions that has been presented to overcome self-disturbance, is called "active method". For these methods, an assistant circuit is added to the circuit of the gate driver. The assistant circuit is activated during off-state of the switch by an external control signal. The main idea of the active methods is to regulate the impedance of the gate during off-state by proposing a path of lower impedance to the induced current towards the negative bias of the gate [8], [18], [19]. Most of these methods has been presented either for negative either for positive perturbation. Moreover, these methods have not been evaluated in maximum switching speed of high-power SiC MOSFETs modules. In this work, an active Miller-clamp protection as an assistant circuit is added to the gate driver circuit (see Fig. 5).

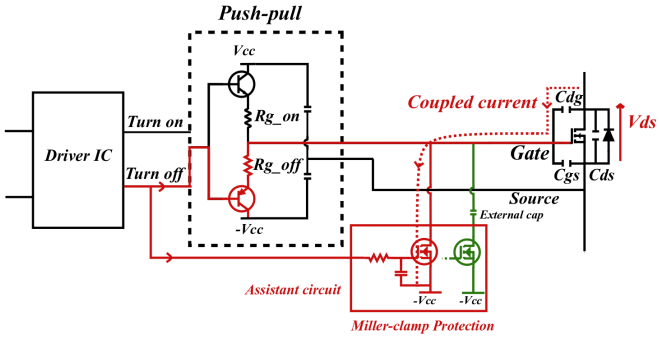


Fig. 5: Miller-clamp protection (the used circuit shown in red, an alternative circuit shown in green).

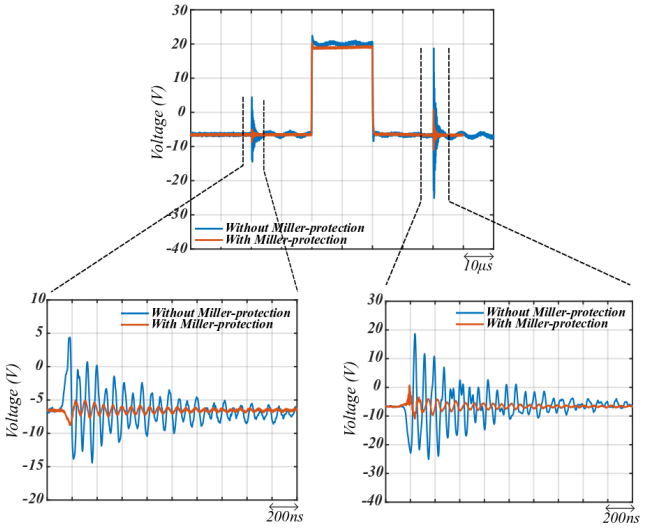


Fig. 6: Experimental result of VgsH considering Miller clamp protection in 500V, 150A double pulse test.

The circuit consists of a N Channel MOSFET which is controlled by the turn-off order of the gate driver IC. During turn-off transition of the SiC MOSFET,

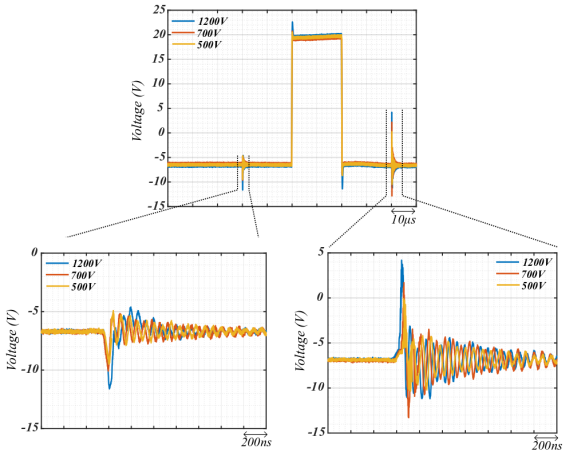
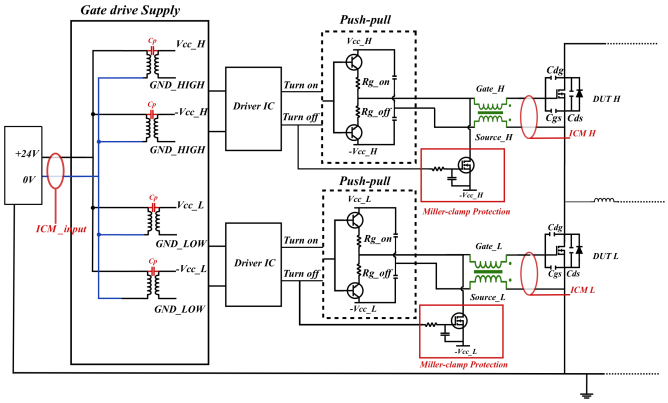
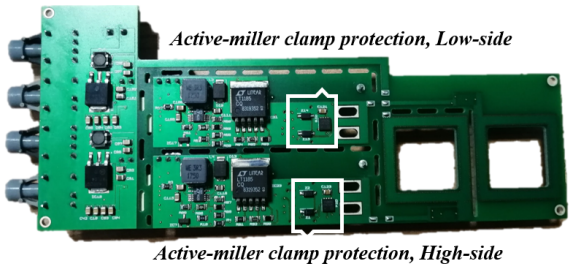


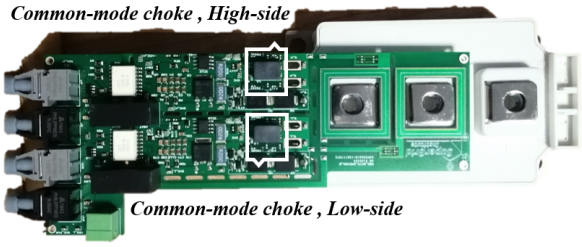
Fig. 7: Experimental result of VgsH considering Miller-clamp protection in 500V, 700V and 1200V and 150A double pulse test.



(a)



(b)



(c)

Fig. 8: Gate driver prototype (a) gate driver schematic (CM choke integrated in green) (b) Bottom view (c) Top view.

the assistant circuit proposes another path for the induced current to the gate driver and clamps the gate voltage to the negative bias of the gate driver. A concern is that, in order to effectively clamp the gate voltage to the negative bias, the Miller-clamp protection MOSFET should turn-on when the device under test is fully turned-off. Therefore, the choice of the MOSFET is an important point. To do so, a resistance and a capacitance have been added to the circuit in order to tune the on-transition of the Miller-clamp protection MOSFET. Unlike the active solution proposed in [18] and [19], the external capacitance (green capacitance in Fig. 5) has not been added to the assistant circuit in order to reduce as much as possible the gate impedance. The added external capacitance can prolong the charging of the input capacitance of the device and consequently slow down the turn-on transition while in this work the goal is to keep the maximum switching speed. The effect of the active Miller-clamp protection is shown in figures 6 and 7. It can be seen that the protection circuit is able to keep the perturbation lower than the threshold voltage for DC voltages up to 500V. During these tests, the voltage between the mid-point of the half-bridge and ground varied with a slope of about $12.5kV/\mu s$. By increasing the DC voltage level up to 1200V (corresponding to a voltage slope of about $30kV/\mu s$), it can be seen that, the protection circuit cannot completely keep the parasitic voltage lower than the device threshold-voltage.

6 Proposed solution and experimental results

Experimental results in section 5 reveal that, thanks to Miller-clamp protection, the gate voltage perturbation is attenuated enough for DC voltage up to 500V. The effectiveness of Miller-clamp protection in maximum switching rate is not validated in higher voltage operation of the SiC MOSFET (see Fig. 7). So as, Miller-clamp protection circuit cannot keep the gate voltage less than the SiC MOSFET threshold-voltage. Hence, for investigating the perturbations, the common-mode (CM) current generated due to the fast switching has been measured across each switch. The details of the generated CM currents and measurement points are shown in figure 8 as

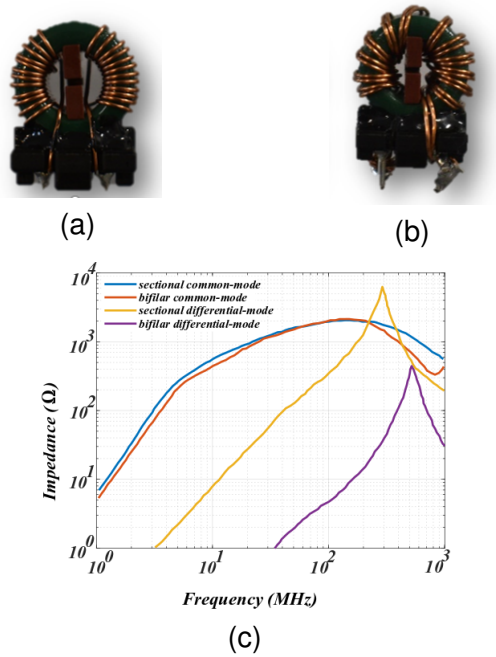


Fig. 9: Common-mode choke winding (a) sectional (b) bifilar (c) Impedance comparison of the common-mode chokes.

ICML, ICMH and input ICM. The measured CM currents are shown in figure 11 as well. Theses measurements show high values of CM currents through gate drivers and these currents have been suspected to be related to self-disturbances. To prove this assumption and to reduce self-disturbances, the proposed solution is to filter the associated CM current of fast switching before it goes through the gate driver. Therefore, a common-mode inductor has been implemented in the gate driver circuit. The chosen filter should have a low impedance for differential mode (DM) in order to not affect the behaviour of the gate drive signal during turn-on and turn-off while it has a big impedance in CM to block the high frequency induced current to the gate and protect the gate driver against voltage perturbation [20].

There are two types of windings for CM chokes: sectional and bifilar. The sectional components have a higher leakage inductance (DM inductor in low frequency) while the performance feature of the two coils is similar in terms of the CM (see Fig. 9). In order to have a minimal impact on the switching speed and gate oscillation, a bifilar choke (one-way winding) has been implemented in the gate driver. Experimental results (see Fig. 10) confirm that, by choosing bifilar winding choke, gate-voltage slope and consequently switching-voltage and switching

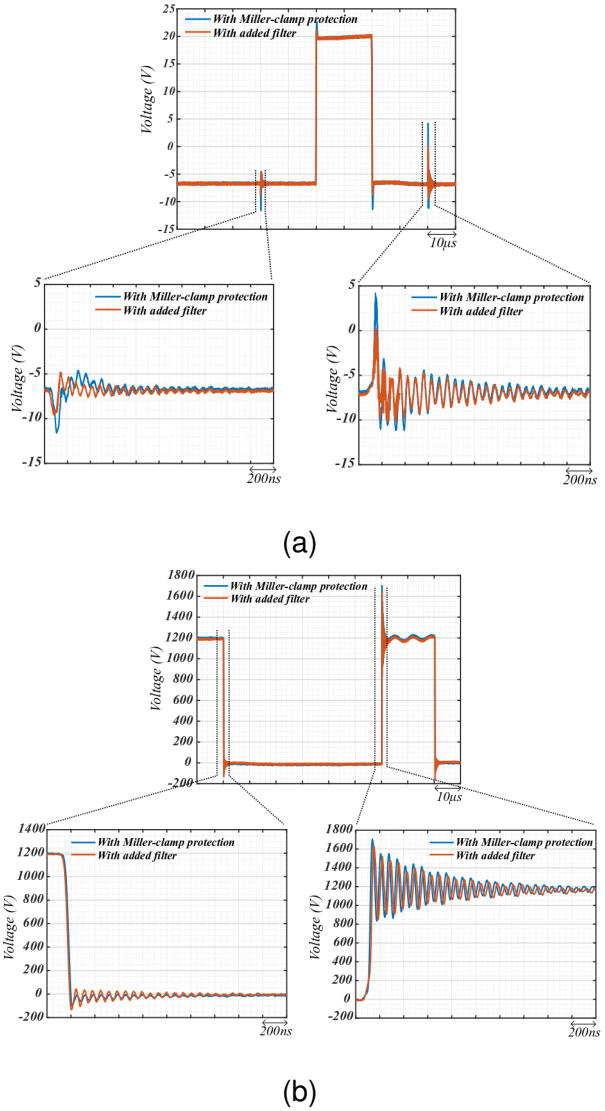


Fig. 10: Experimental results considering proposed solution in 1200V, 150A double pulse test (a) gate-source voltage (b) drain-source voltage.

losses will not be affected by the added component. Experimental results shown in figure 11, illustrate that the CM currents have been reduced in high-side and low-side and proves the effect of the choke. By implementing the filter, input CM current has been reduced by up to 20% (see Fig. 11). Since the gate driver provides a path for common-mode current to the controller, this method helps to reduce the risk of loading the controller and reduces the self-disturbance phenomenon.

7 Conclusion

This article compared the self-disturbance phenomenon in phase-leg configuration with IGBTs

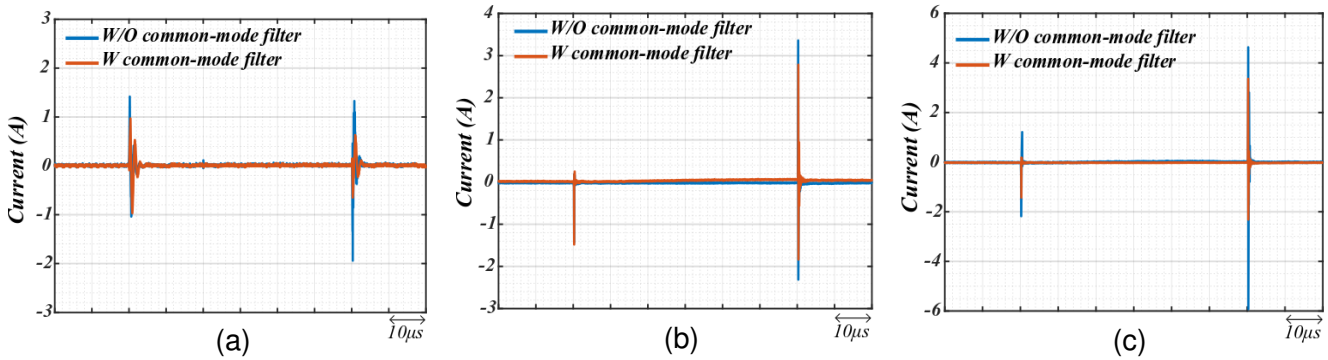


Fig. 11: Experimental results of measured common-mode currents in 1200V, 150A double pulse test (a) ICML (b) ICMH (b) Input- ICM.

and MOSFETs on a double-pulse test-bench. The experimental results show the severity of the problem by SiC MOSFETs compared to IGBTs due to the higher switching speed ability of the SiC MOSFET and different characteristics of IGBT compared to MOSFET. Moreover, the more negative allowable bias of the IGBT reduces the risk of self-disturbance phenomenon. Two solutions have been investigated investigated for SiC MOSFETs. The conventional active Miller-clamp protection has been tested with different DC voltage levels to show the effectiveness of the protection circuit. The experimental results revealed that, in order to use the potential capacity of fast high power SiC MOSFET device, there is a need for another solution.

Here, in order to overcome the self-disturbance, the common-mode current generated by fast switching has been measured and it has been proposed to block this common-mode current before it goes to the gate. By choosing bifilar choke, it is possible to block the associated current and reduce the gate-voltage perturbation. The proposed solution has been validated in 1200V, 150A switching transition and reduces significantly the input common-mode current of gate driver. Then this solution allows to use SiC MOSFETs at maximum switching speed and does not increase switching losses.

Acknowledgement

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