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Conducted EMI reduction in a 100kW 1.2kV Dual Active Bridge converter

Hadiseh GERAMIRAD[1,2], Florent MOREL[1], Piotr DWORAKOWSKI[1], Bruno LEFEBVRE[1], Thomas LAGIER[1], Philippe CAMAIL[1], Christian VOLLAIRE[1,2], Arnaud BREARD[2]

[1] SAS SuperGrid Institute, ITE, France
[2] Ecole centrale de Lyon, Ampère lab, CNRS 5005, France

Corresponding author: Hadiseh GERAMIRAD, hadiseh.geramirad@supergrid-institute.com

Abstract

Medium-frequency transformer is one of the key components of isolated power electronic converters. The parasitic capacitances of the transformer provide paths for the common-mode current inside the converter. The electromagnetic interferences due to fast switching are among the main concerns for the design of SiC MOSFET based power converters. The conducted emissions of the converter are directly linked to its physical layout. In this work, the main loops of the common-mode current in the presence of a 3-phase medium-frequency transformer are discussed. The experimental studies show the effects of the transformer construction and vector group (star/delta) on the common-mode currents through the gate drivers of SiC MOSFETs in a 100kW 1.2kV three-phase dual active bridge converter.

1 Introduction

The maturity of commercial high-voltage high-current semiconductors such as 1.7kV SiC MOSFETs allows converter designers to improve power converters density and efficiency [1]. Using SiC MOSFET results in fast rising and falling of the voltage and current which creates unwanted currents due to the parasitic inductances and capacitances in the layout of the converter [2]–[4]. Therefore, using SiC MOSFETs as switching element of power converters increases the electromagnetic interferences (EMI). For this reason, implementing SiC MOSFETs and dealing with the generated EMI added a new dimension to the design of power converters. To solve an aforementioned EMI problem in a converter, it should be considered that the parasitic elements change over their frequency band, the topology of the converter changes from one design to another one, the switching speed can vary based on the converter, etc. Therefore, there is not a well-defined design methodology. It is then difficult to have a general attitude to solve the problem [5]. In addition, the size and cost of the electromagnetic filter to reduce the EMI become an important factor in high power-density converters [6]–[8]. So reducing the common-mode (CM) noise of the power converter can help to simplify the filter design and to reduce the total size.

In isolated DC/DC converters, there are plenty of coupling capacitances which provide paths for CM current [9]–[12]. In most of the cases, a CM electromagnetic disturbance issue is due to the circulation of the CM current into the layout of the converter [13]. It is always a challenge to ensure that the CM current of a converter is well-controlled in order to not disturb its critical elements like gate drivers and controllers. In the converter, a gate driver has to provide at least two functions, the signal transmission and the power supply for switching [14]. The signal transmission includes signals for switching orders and protection of the device. The power supply design is challenging since this part of the circuit should provide a high isolation with a low coupling capacitance. The gate driver is one of the EMI victims in the converter due to the parasitic capacitances in its isolation stages [15]. Since gate drivers provide an interface between the controller and the switches, the CM current can disturb the controller [16]. A limited

CM current passing through the gate driver is required in order to guarantee proper operation of the converter. For a commercial gate driver, the isolation is defined and cannot be change. However, a proper design of the converter can change the CM current. Hence, identification and investigation on the CM current in an isolated DC/DC converter is the objective of this work.

Understanding the effect of the parasitic elements in the converter layout provides a basis for applying the EMI reduction techniques. There are several studies focused on EMI modelling and analysis of dual active bridge (DAB) converters [17]–[21]. There are some experimental works for fly-back converters [22]–[25] but there are not a lot of researches focused on experimental EMI behaviour of a 3-phase DAB (DAB3) using SiC MOSFETs. The uncontrolled CM currents pass through gate drivers (input CM current) and disturb the proper turn-on and turn-off of the switches. This is the problematic case in this prototype above 800V, 100kW. This phenomenon is called here “self-disturbance”. It was encountered as an obstacle to achieve the nominal operation of the converter. Changing the parasitic elements, once the design completed, is costly and time consuming, therefore, here with comparative experimental study, it is targeted to show the effect of the MFT design on the input CM current of gate drivers and highlight the effect of the transformer design on the self-disturbance phenomenon. So as, this paper analyses the CM current behaviour of the DAB3 based on different transformer structures with the following organisation. Section 2 describes the DAB3 used as a test-platform in this study. Section 3 presents the paths of the CM current in the converter. In section 4, the proposed model is experimentally validated and the influence of different transformer designs on the CM current is analysed. Section 5 concludes the article.

2 Considered converter

A 3-phase DAB is made of two voltage source converters (VSC) connected through a 3-phase medium frequency transformer (MFT). Both VSCs are composed of three legs of half-bridge power semiconductors which are controlled by half-bridge gate drivers (see Fig. 1). In the operation of the DAB, each VSC generates a square waveform. A controlled phase shift δ between the primary and secondary voltages can control the power flow through the MFT. Thus the power can be transmitted from VSC1 to VSC2 or vice versa (the direction from VSC1 to VSC2 is called here as +P and opposite direction as -P).

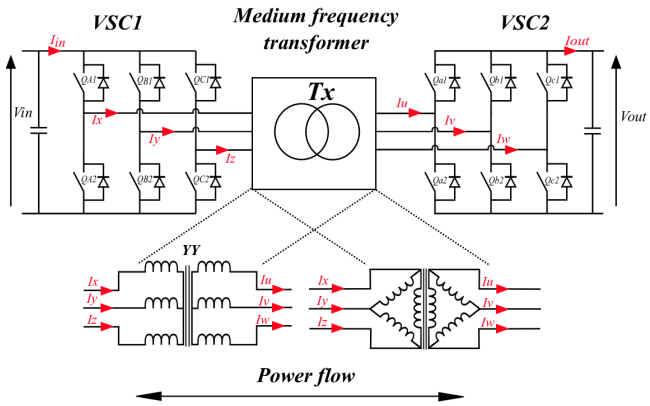


Fig. 1: Dual active bridge schematic.

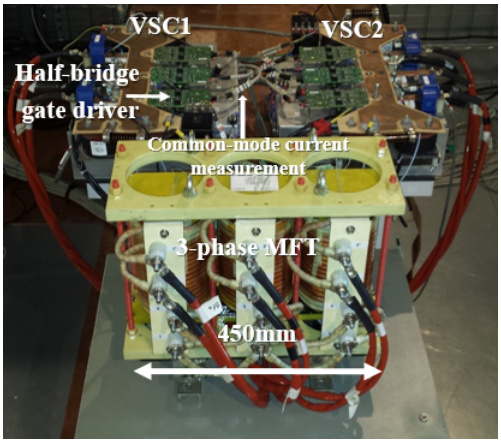
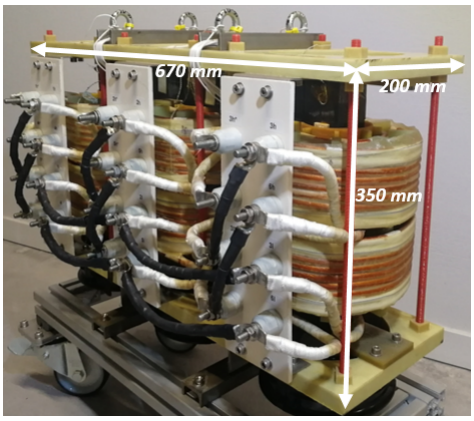


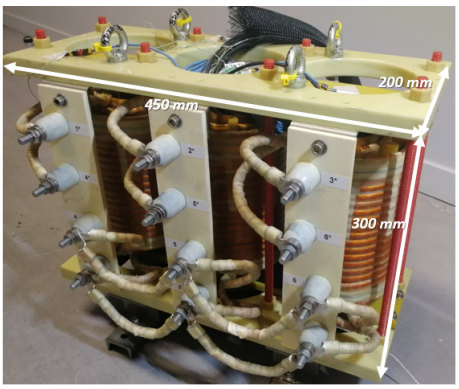
Fig. 2: 100kW, 1200V, DAB3 prototype.

The investigation has been carried out in this work on a new 3-phase 100kW 1.2kV dual active bridge converter prototype (see Fig. 2) [26], [27]. The considered DAB3 is sized for 100kW power transfer at 20kHz switching frequency, 11kV/μs switching speed and benefits from soft switching capabilities in both VSCs with identical gate drivers. The novelty of this DAB3 is the 3-phase MFT design which is focused to establish a power flow between 1.2kV DC-links [28] (see Fig. 3). In the structure of the transformer, there are three types of parasitic capacitances. The parasitic capacitance between winding layers (C_p and C_s in Fig. 4), the inter-winding capacitance between primary winding

and secondary winding (C_{ps} in Fig. 4) and the parasitic capacitance between neutral point to the ground in YY configuration (C_{ng} in Fig. 4). The model parameters of the transformers (see Fig. 4) are presented in table 1. The transformer T1 can operate in $\Delta\Delta$ or YY configurations while T2 can operate only in YY configuration.



(a)



(b)

Fig. 3: Medium frequency transformer (a) T1 prototype (b) T2 prototype.

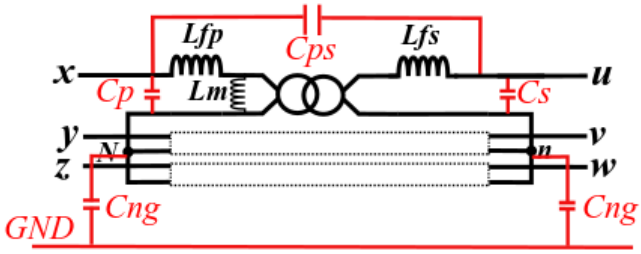


Fig. 4: Transformer model in YY configuration.

3 Common-mode current paths

The noise source in each leg of the VSC is the voltage variation across MOSFETs/diodes. The propagation paths are provided by coupling capacitances in the layout of the converter which experience high $\frac{dv}{dt}$. The main coupling capacitors that are subject to fast variations of the voltage are shown in figure 5. During a fast voltage variation across a switch, the parasitic capacitances in the isolation stages of its gate driver provide coupling paths for CM currents to pass through the gate drivers and consequently to the converter controller [10] (C_{pg} in Fig. 5). The voltage variation along the windings of the transformer makes the parasitic capacitances of the transformer as other paths in which the current can circulate [29] from one VSC to the another and also shunt the CM current to the ground (C_s, C_p, C_{ng} and C_{ps} in Fig. 5) [23]. Parasitic capacitance between the device and the heat-sink [18], provide another path for the CM current to the ground (C_{ph} in Fig. 5). The existence of these parasitic paths in the layout of the converter is unavoidable and also changing the value of the related capacitances can not be done after design phase. In practice, due to physical limitations, it is very difficult to measure all the CM currents which makes the analysis even more difficult. Then, the amplitude of the time domain waveform of the input CM current through gate drivers is the EMI criteria of this study. A comparative study has been done to illustrate the effect of the MFT design on the input CM current through gate drivers.

Tab. 1: Parameters of the transformers based on impedance measurement in YY configuration.

Parameter	Unit	T1	T2
L_{fp}	μH	17	8
L_{fs}	μH	17	8
L_m	mH	1	1
C_p	pF	30	65
C_S	pF	30	60
C_{ps}	pF	80	85
C_{ng}	pF	30	50

4 Experimental results and analysis

The experimental study has been done by conducting continuous-mode tests on the converter

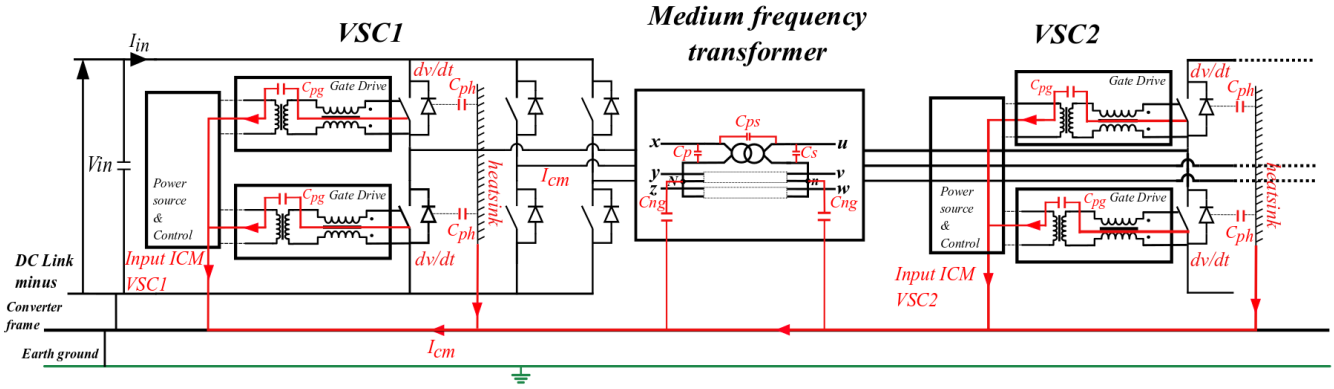


Fig. 5: CM current paths in an isolated dual active bridge converter.

prototype (Fig. 2) at 800V, 100kW with T1 and T2 and it has been completed in nominal operation of the converter at 1200V, 100kW with T2 only. The investigation has been focused on the phase B (y for VSC1 and v for VSC2) of the converter considering that the analysis can be applied for the rest of the system. The input CM current of the half-bridge gate driver of the phase B has been measured with different transformer configurations and with both MFT designs.

4.1 Common-mode current circulation

As each leg of VSCs switches at 20kHz, each switch creates a CM current each 25μs. The experimental results shown in figures 6 and 7 revealed that the generated CM current passing through a gate driver is not dominated only by the voltage variation across the corresponding switch but also due to the voltage variation in other legs of the same VSC and even the complementary VSC.

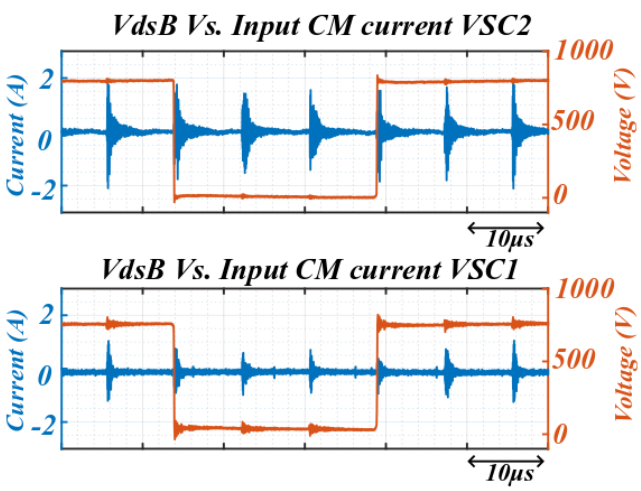


Fig. 6: Experimental measurement of Vds and input CM current in 800V, 0kW, T1 in YY configuration.

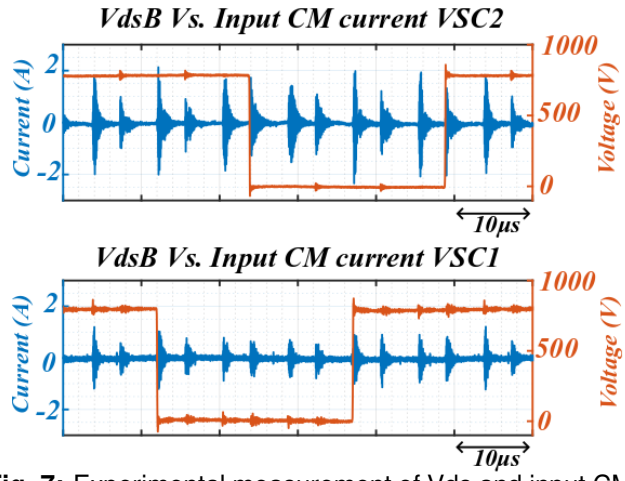


Fig. 7: Experimental measurement of Vds and input CM current in 800V, +100kW, T1 in YY configuration.

It can be seen that due to the physical electrical connection, the CM current passing through the gate driver of one switch is changed based on the phase shift variation in the converter. When the converter operates at zero power, there is no phase shift between the VSCs while by increasing the phase shift, the CM current changed based on the voltage phase shift in both VSCs.

To show the circulation of the CM current from one VSC to another, the CM current of the gate driver has been measured in both power flow directions. Experimental results (see Fig. 8) reveal the difference between the magnitude of the two input CM currents.

By repeating the same measurement but in opposite power flow (from VSC2 to VSC1 indicated as -P), it is shown that the input CM current of VSC2 is similar to input CM current of VSC1 in +P. Due to the phase shift between VSC1 and VSC2 controls, these converters do not switch the

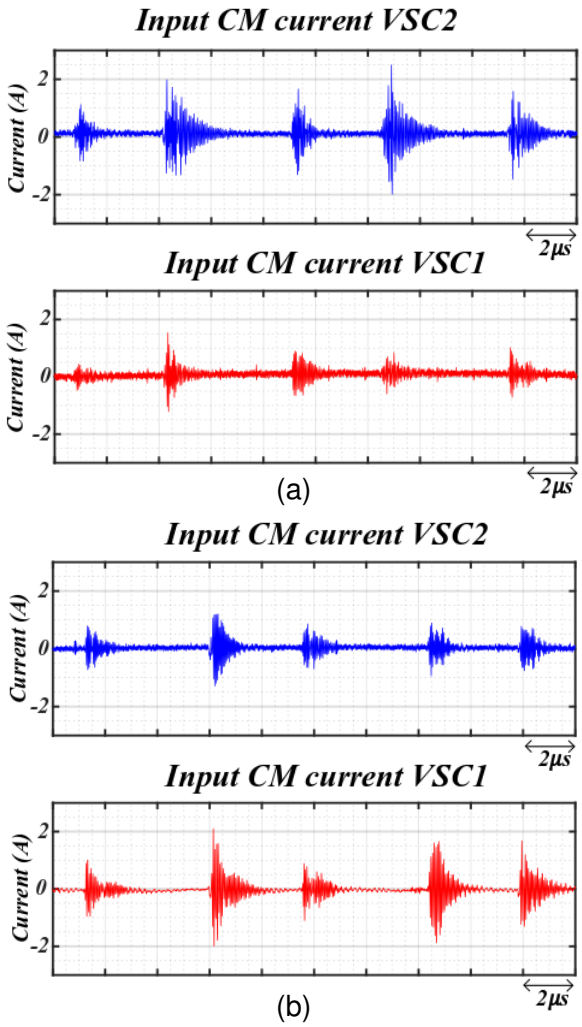


Fig. 8: Experimental comparison of input CM current, 800V, MFT1 in YY configuration (a) +100kW (b) -100kW.

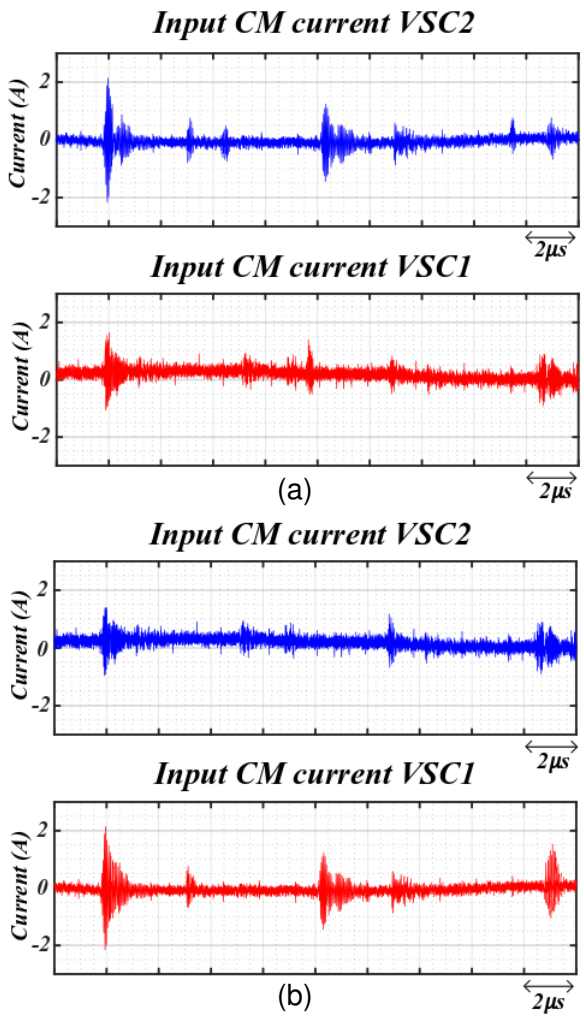


Fig. 9: Experimental measurement of input CM current, 800V, MFT1 in $\Delta\Delta$ configuration (a) +100kW (b) -100kW.

same current amplitudes. That is why the input CM current amplitudes differs by inverting the power flow. The phase shift is reverted in -P and the phenomena observed in VSC2 in P has been occurred in VSC1 in -p [30]. The inter-winding capacitance of the transformer provides a path for the CM to transfer from one VSC to the other (see Fig. 4) which changes the amplitude of the CM current. The performance of the converter with T1 in $\Delta\Delta$ configuration has been tested. It changed the waveforms of the input CM current but its amplitude has not been changed by changing vector group (see Fig. 9).

4.2 Common-mode current reduction

CM current is always passing through the coupling path with less impedance. If the transformer parasitic capacitances are bigger than the parasitic capacitances of the gate driver isolation, then the CM current will pass more through the transformer than through the gate driver. These capacitances (see Fig.4) can change based on the transformer design. In this section, to show the effects of these capacitances on CM current through the gate driver, the CM current has been measured with two different designs of the transformers in YY configuration. Note that with these designs, values of C_{ps} are almost the same while values of C_{ng} are quite different (see Table. 1).

Due to the more compact design of T2 (dimension and size of the windings [28]), the neutral point to ground capacitance (C_{ng}) provides an almost two times smaller impedance path to the ground compared to T1. The bigger capacitance leads

to a smaller impedance, which is preferred to pass through by the CM current. The parasitic capacitances shunt a significant amount of CM current to the ground, and since, the CM current through gate driver is reduced. The minimized loop is shown in figure 10.

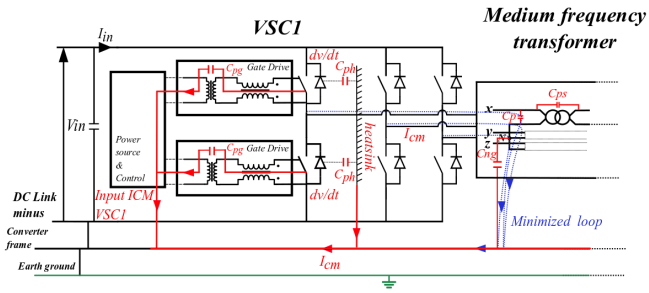


Fig. 10: Minimized loop of the CM current due to a different design of the MFT2.

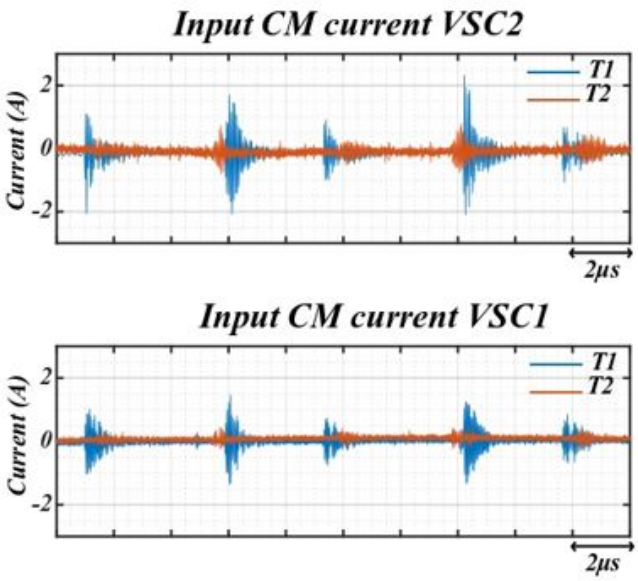


Fig. 11: Experimental result of input CM current of gate driver, comparison between two transformers design in 800V, 100kW.

The input CM current has been measured in the same configuration by changing the transformer. The experimental results validate how parasitic capacitances of T2 shorten the CM current path then reduce the CM current through gate drivers (see Fig. 11). Not only the CM current due to switching in phase B, but also the generated CM current due to the other phases found a shorter impedance to flow. This reduces the CM current of the gate driver significantly. Thanks to the optimised design of the transformer, the nominal operation of the converter has been achieved at 1200V, 100kW (see Fig. 12).

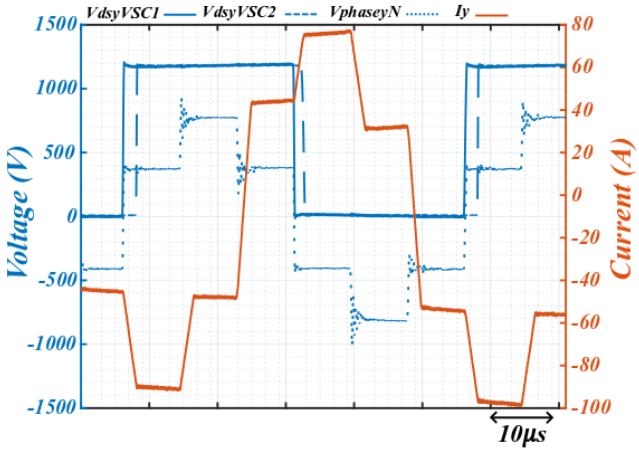


Fig. 12: Experimental converter waveform, isolation with T2 in 1200V, 100kW.

5 Conclusion

In the design of isolated converters, medium-frequency transformers provide a galvanic isolation while introducing, at high frequencies, a low impedance path for common-mode current between primary and secondary. The provided path allows the circulation of current through gate drivers. This paper compared experimentally two different designs of the transformer in the same layout of the converter to show the effects of the transformer design on the common-mode current through the gate drivers. The nominal operation of the converter has been achieved thanks to an improved design of the medium-frequency transformer since it reduces the input common-mode current of the gate driver and solve the self-disturbance phenomenon.

Adopting a filter connected to the transformer star-point in order to reduce the impedance of the CM current from neutral point to ground to minimize the CM current loop and introducing a screen between primary and secondary windings and connecting this screen to ground are possible perspectives for this work.

Acknowledgement

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