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RESEARCH ARTICLE

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Understanding of the influence of localized surface defectivity properties on the performances of silicon heterojunction cells

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Abstract

The industrial fabrication process of silicon heterojunction (SHJ) solar cells can induce locally depassivated regions (so-called defectivity) because of transportation steps (contact with belts, trays, etc.) or simply the environment (presence of particles at the wafer surfaces before thin film deposition). This surface passivation spatial heterogeneity is gaining interest as it may hinder the SHJ efficiency improvements allowed by incremental process step optimizations. In this paper, an experimentally supported simulation study is conducted to understand how the local a-Si:H/c-Si interface depassivation loss impacts the overall cell performance. The defectivity-induced cell performance drop due to depassivated regions was attributed to a bias-dependent minority carrier current flow towards the depassivated region, which is shown to affect all current–voltage ($I(V)$) parameters, and in particular the fill factor. Simulation was used further in order to understand how the defectivity properties (spatial distribution, localization and size) impact the induced performance losses. In the light of all results, we propose ways to mitigate the defectivity influence on the cell performances.

KEYWORDS

defectivity, heterojunction, recombination, silicon solar cells

1 | INTRODUCTION

The deposition of stacks of intrinsic hydrogenated amorphous silicon (*a*-Si:H(i)) and highly doped amorphous silicon (*a*-Si:H(n/p)) layers on the monocrystalline silicon (*c*-Si) wafer provides outstanding surface passivation and carrier selectivity which has enabled heterojunction solar cells (silicon heterojunction [SHJ]) efficiencies (η) around 24% on full size SHJ made on the pilot production line at CEA-INES[1] and about 25% in laboratory.[2,3] With such passivation quality and in a context where multi-millisecond carrier lifetime wafers are commercially available, inhomogeneities at the cell level are inevitably gaining interest on the way to higher efficiencies. Among them, local depassivations of the surface, frequently observed on photoluminescence (PL) images[4] and referred to as 'defectivity' here, is put at the forefront of this study. These localized depassivations are attributable to the manufacturing process itself, such as friction on the trays or particle inclusions between or during the deposition steps. To our knowledge, the physical mechanisms behind the influence of damaged regions on the SHJ cell performance have been very little addressed so far. Nos et al were able to empirically associate fill factor (FF) losses to PL images taken on SHJ cells sampled out of the pilot line at CEA.[5] Furthermore, Breiteinstein and Sontag developed a local efficiency mapping tool based on dark lock-in thermography (DLIT) which allows to locally assess the effects of defectivity on η of SHJ cells taken out of a production line.[6] Both of these studies brought to light the importance of defectivity on the performance losses. However, they were performed on cells with unknown defectivity properties (dimensions, localization and recombination velocity), so the

[Correction added on 27 September 2020 after first online publication: the order of the figures has been corrected in this version of the article.]

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understanding of the mechanisms behind the device performance losses could only be partial.

In this context, the purpose of this work is first to quantify and understand the influence of surface defectivity on the cell current–voltage ($I(V)$) parameters. To this aim, devices with a well-defined and intentionally performed defectivity on their front surface were studied using combined experimental and simulation approaches, in order to validate the simulation code and unveil the nature of the physical mechanisms at play.

In a second time, the defectivity spatial distribution at a given total depassivated surface were studied. Then the physical mechanisms behind the difference between front and back side defectivity was described. Finally, this paper presents the influence of wafer parameters such as the bulk carrier lifetimes and the wafer doping, on the defectivity-induced performance losses.

2 | EXPERIMENTAL, SIMULATION DETAILS AND VALIDATION OF THE SIMULATION CODE

The experimental and simulation details as well as the validation of the simulation code are broadly presented in Giglia et al.[7] Nevertheless, for the sake of clarity, the salient features in Giglia et al[7] are presented in the following.

2.1 | Cells fabrication, controlled defectivity and simulation details

2.1.1 | Cells fabrication and controlled defectivity

All SHJ cells in this work were fabricated using the same process on the CEA-INES pilot production line, based on n-type Cz monocrystalline substrates (M2 format, PSQ $156.75 \times 156.75\,\text{mm}^2$). After a texturation of the wafer, intrinsic and doped *a*-Si:H layers were deposited on both sides, with a n-doped stack (i/n) on the front side and a p-doped (i/p) on the rear, corresponding to the 'inverted emitter' architecture.[8,9] Then, indium-tin oxide (ITO) layers were deposited on both sides, and finally, silver grids were screen-printed on both sides before curing. The process fabrication led to $\eta \approx 22.5\%$.

2.1.2 | Controlled defectivity

In order to quantify the $I(V)$ parameters losses induced by passivation inhomogeneities, one controlled scratch was performed every nine metallization pitches, on the front side through the whole length of 10 busbarless cells, using a diamond tip. This resulted in overall nine scratches over the whole surface. Busbarless cell was preferred as this metallization scheme facilitates in practice the scratching steps (no perpendicular metallization) and also the modelling of the structure (high level of symmetry). A typical PL image after scratches formation is shown in Figure 1. The width of each scratch was fairly constant ($37 \pm 5\mu$m) and proved the repeatability of the protocol. However, given that the diamond tips edges form a 90° angle, the depassivated region forms a groove. Therefore, its cross section was assumed to be around $\sqrt{2} \times 37 \approx 50\mu$ m width. The criticality of this assumption is not strong, since little variations in the width of the scratch around 50 μm will be shown in Section 4 to have negligible effects on the induced performance losses. Furthermore, as revealed by optical microscopy, the scratches remove the whole TCO/*a*-Si:H stack and in doing so, thoroughly depassivate the silicon surface. Thus, the recombination velocity of the depassivated surface is assumed to be limited only by carrier diffusion to the defect. This protocol leads to a defectivity whose shape, localization and recombination velocity are therefore known.

In addition to the intentionally made scratches, other background defects can be observed in Figure 1. The origin of these defects are unintended surface injuries or contaminations stemming from some wafer transportation steps and assumed to have a much less important effect on the cell performances than the intentionally created scratches, as can be visually inferred from Figure 1B.

Due to a prohibitive cell breakage rate, the scratching protocol was not suitable to reach higher defectivity densities, which were instead achieved through rubbing the cells against each other. Although this defectivity distribution is not the same as that simulated, this allowed us to qualitatively compare simulated and experimentally observed trends.

2.1.3 | Simulation details

Simulations were run using the ATLAS package from Silvaco,[10] a multiphysical simulation software. Figure 2 is a representation of the modelled structure, which is a vertical cut of the cell along its whole thickness and nine metallization pitches wide (which is the distance between two experimental scratches cf. Figure 1). Thus, the 2D structure is about 160-μm thick and 16 200-μm wide (for the sake of simplification, only one intermetallization pitch was represented in Figure 2). Furthermore, the properties of each layer are set based on characterization results obtained on the devices we intend to use for the experimental validation of this code. Details can be found in Giglia et al.[7] The substrate resistivity is $4.5\,\Omega/\text{cm}^{-1}$, and the minority carrier lifetime in the *c*-Si and their diffusion length, at the open circuit working point, are τ_{bulk}=1.7 ms and L_D=1.1 mm. These parameters are typical of those of commercially available wafers. In order to implement the depassivated region, the front *a*-Si:H/*c*-Si interface mid-gap trap density D_{it} was locally maximized ($D_{it} = 10^{14}\,\text{cm}^{-2}$) in the middle of the device, on a width corresponding to the experimentally performed scratch width.

For the sake of simplicity, a physical discontinuity of the *a*-Si:H and ITO layers, as created experimentally during scratching was not implemented in our simulations. This implementation would imply to set a more complicated mesh, leading to a prohibitive increase in the computation time. In order to check the degree of acceptability

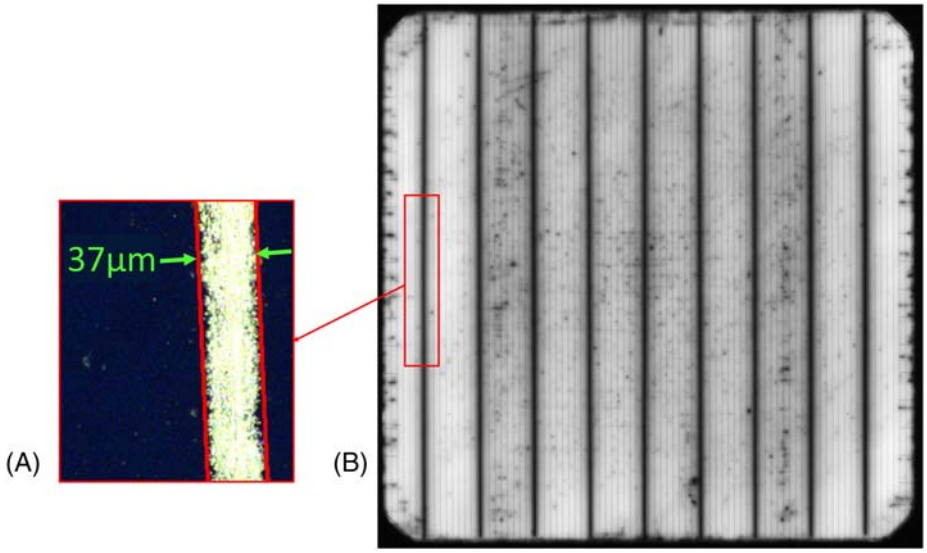

FIGURE 1 Optical microscopy picture of a scratch (A) and photoluminescence image of a cell with nine scratches on its front side (B) [Colour figure can be viewed at wileyonlinelibrary.com]

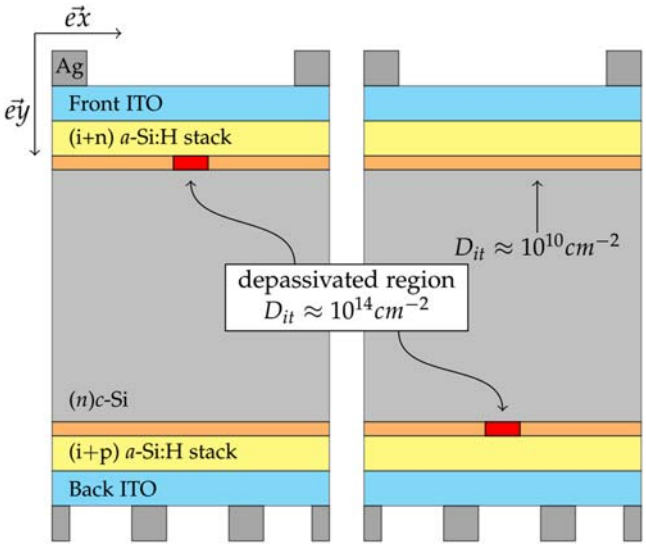

FIGURE 2 Representation of one intermetallization pitch of the simulated structure with the implementation of the depassivated region localized at the (i + n)*a*-Si:H/(n)*c*-Si (left) or the (i + p)*a*-Si:H/(n)*c*-Si (right) interface as a locally increased density of interfacial trap (D_{it})

of this simplification, simulations with and without the discontinuity implementation were run. The difference between the simulated performance losses obtained with these two structures does not exceed 0.02%abs. This is because the attraction induced by the locally maximized D_{it} is much greater than the action of the field effect.

First, the structure is solved at the equilibrium. Then the structure is exposed to a AM1.5G spectrum, and the collected current is calculated for several forward bias voltages in order to derive the cell *I*(*V*) curve. The curve is then used to determine the individual *I*(*V*) parameters: the open circuit voltage V_{OC}, the short circuit current J_{SC}, the fill factor *FF* and the efficiency η.

2.2 | Validation of the simulation code

In order to validate the simulation code, simulation results were compared to measurements performed on actual cells. To this aim, *I*(*V*) measurements were performed after each additional scratch creation on the ten busbarless cells described in Section 2.1. The results are shown in Figure 3. First of all, these results show a good repeatability of the scratches creation protocol as all η drop by the same amount. This figure shows that the efficiency losses are about 6%rel. Thus, the defectivity effect is much more important than the unpassivated surface alone, which covers about 0.2% of the whole cell surface. Furthermore, it must be noticed that the efficiency losses are driven by *FF* losses which is consistent with Balent et al.[11] *FF* losses represent 4% of the 6%rel efficiency losses while the J_{sc} and V_{oc} are both decreased by about 1.3%.

In order to validate the simulation code, simulations were performed (1) without defectivity and (2) with the same defectivity spatial distribution as for actual cells (i.e., one depassivated region every nine intermetallization pitch). The results are shown in Figure 3 as red stars. First of all, we point out that the discrepancies between the absolute values of simulated and experimentally measured *I*(*V*) parameters are lower than 1%rel (see Table 1).

The good agreement between experimental and simulated relative losses demonstrates that simulation is able to predict accurately the defectivity-induced *I*(*V*) losses. Thus, in the following, the simulation is considered as a trustworthy way to investigate the mechanisms behind defectivity-induced cell performance losses.

3 | LOSS MECHANISMS STUDY

In this part, space-resolved simulation outputs are used to explain the mechanisms behind the defectivity-induced performance losses. The simulation software allows the calculation and plotting of physical quantities like quasi-Fermi levels, current densities and carrier

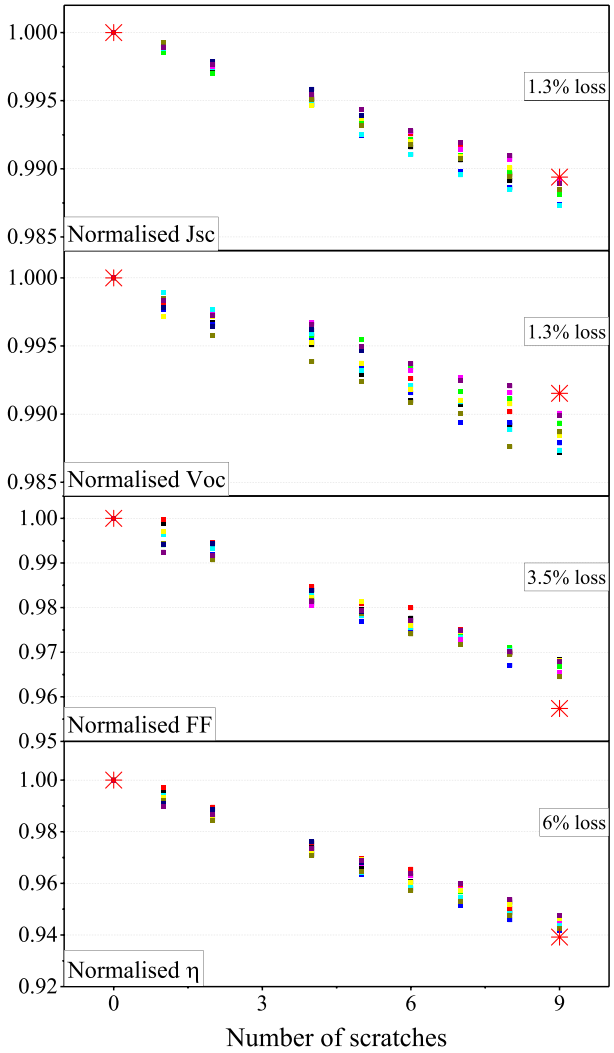

FIGURE 3 Normalized *I*(*V*) parameters evolution with an increasing number of scratches made on 10 busbarless SHJ solar cells. Each colour corresponds to a particular cell. The red stars are the simulated *I*(*V*) parameters for cells with or without defectivity on their front *c*-Si/*a*-Si:H interface

concentrations. The spatial quasi-Fermi level gradient is directly proportional to the force applied to the holes.[12] In Figure 4, the hole quasi-Fermi level $\varepsilon_{F,h}$ is plotted without (A) and with (B) a depassivated region on the cell front *a*-Si:H/*c*-Si interface. The level zero for the quasi-Fermi level is set to its level in the structure at equilibrium. Without the depassivated region, there is only one $\varepsilon_{F,h}$ gradient $\vec{\nabla}\varepsilon_{F,h}(collect)$ which is directed towards the backside *a*-Si:H/*c*-Si interface: photogenerated holes drift towards the (i + p) *a*-Si:H hole contact. It can be noticed that the gradient $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ is decreasing as the voltage increases. When the voltage is lower than a threshold voltage $V_t \approx 0.45V$ the $\varepsilon_{F,h}$ profile does not change significantly, and the collected current is the same for any bias voltage. This can be explained as for $V < V_t$, there is only a slight bias voltage-induced decrease in band bending leading to a slight decrease in field effect which allows for an efficient hole extraction via the junction. For $V > V_t$ instead, the field effect at the (i + p)*a*-Si:H/*c*-Si interface decreases leading to a less effective hole extraction. The collected current decreases (Figure 4C), until open circuit working point is reached where no current flows any longer (corresponding to $\|\vec{\nabla}\varepsilon_{F,h}\| = \|\vec{\nabla}\varepsilon_{F,h}(collect)\| = 0\ eV/\mu m$).

When a depassivated region is present at the front a-Si:H/c-Si interface (Figure 4B), while the picture is basically the same at the backside, a strong additional gradient directed towards the front depassivated region shows up (Figure 4). This component is denoted $\vec{\nabla}\varepsilon_{F,h}(def)$. Thus, the total $\varepsilon_{F,h}$ gradient is expressed as $\vec{\nabla}\varepsilon_{F,h} = \vec{\nabla}\varepsilon_{F,h}(collect) + \vec{\nabla}\varepsilon_{F,h}(def)$. If the bias voltage increases from V_t to V_{oc}, the $\vec{\nabla}\varepsilon_{F,h}(def)$ contribution to $\vec{\nabla}\varepsilon_{F,h}$ gains importance until the open circuit working point where $\vec{\nabla}\varepsilon_{F,h} \approx \vec{\nabla}\varepsilon_{F,h}(def)$. From this observation, it can be noticed that the $\vec{\nabla}\varepsilon_{F,h}(def)$ relative contribution to $\vec{\nabla}\varepsilon_{F,h}$ increases with increasing bias voltage. As a consequence, the relative current losses at a given bias voltage increases from V_t to V_{oc} (Figure 4C).

These observations can be used back to explain quantitatively the results of Figure 3. First, as exposed above, at the open circuit working point, $\vec{\nabla}\varepsilon_{F,h} \approx \vec{\nabla}\varepsilon_{F,h}(def)$. Therefore, charge carriers wherever they are located experience a force directed towards the depassivated area. However, on average, they can only reach the depassivated area provided that they have been photogenerated at a distance L from the depassivated area smaller than their diffusion length L_d. Assuming roughly that all holes photogenerated at a distance $L < L_d$ from the depassivated area recombine there, we can approximate that the depassivated region affects a $2L_d$ wide region centred on the scratch. This corresponds to 16% of the whole cell surface leading to 16% carriers being lost by recombination on the defect. The effects of that can be inferred starting from the following expression of the open circuit voltage:

$$V_{oc} \approx \frac{kT}{q} ln\left[\frac{\Delta p(\Delta n + n_0)}{n_i^2}\right],$$

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, Δn and Δp are the excess carrier concentrations (or injection levels) at V_{oc} operating point, n_0 is the equilibrium free electron concentration and n_i is the intrinsic carrier concentration. In this study, the open circuit excess carrier concentrations far from a depassivated area is $\Delta n = \Delta p = 1.6 \times 10^{16}\ cm^{-3}$, as obtained from simulations. When applying a 16% carrier concentration loss due to the front side defectivity, at $T = 298K$, $n_0 = 1 \times 10^{15} cm^{-3}$ and $n_i^2 = 6.7 \times 10^{19} cm^{-3}$,[13] the V_{oc} is decreased by 1.2%, which is consistent with the results shown in Figure 3. An analogous analysis can be carried out for the J_{sc} losses. As exposed above, at this working point, $\vec{\nabla}\varepsilon_{F,h}(def)$ only slightly affects $\vec{\nabla}\varepsilon_{F,h}$ in comparison with that at V_{oc}. Thus, the depassivated region affected area is very little extended compared to that at V_{oc}. Furthermore, given that photogeneration under an AM1.5 spectrum occurs mostly at the vicinity of the front *c*-Si surface, the J_{sc} loss is determined by the area where $\vec{\nabla}\varepsilon_{F,h}$ is directed towards the depassivated area close to this interface. The hole current densities at this interface is mapped in Figure 10A.

TABLE 1 Comparison between simulation and measured *I*(*V*) parameters (averaged over 10 cells) with and without implemented defectivity

	Isc (A)		Voc (mV)		FF (%)		Eff (%)	
	Measurements	Simulation	Measurements	Simulation	Measurements	Simulation	Measurements	Simulation
Without scratches	9.39	9.27	733.8	736.6	79.56	79.74	22.45	22.29
With 9 scratches	9.28	9.17	725.4	730.3	76.92	76.34	21.21	20.93

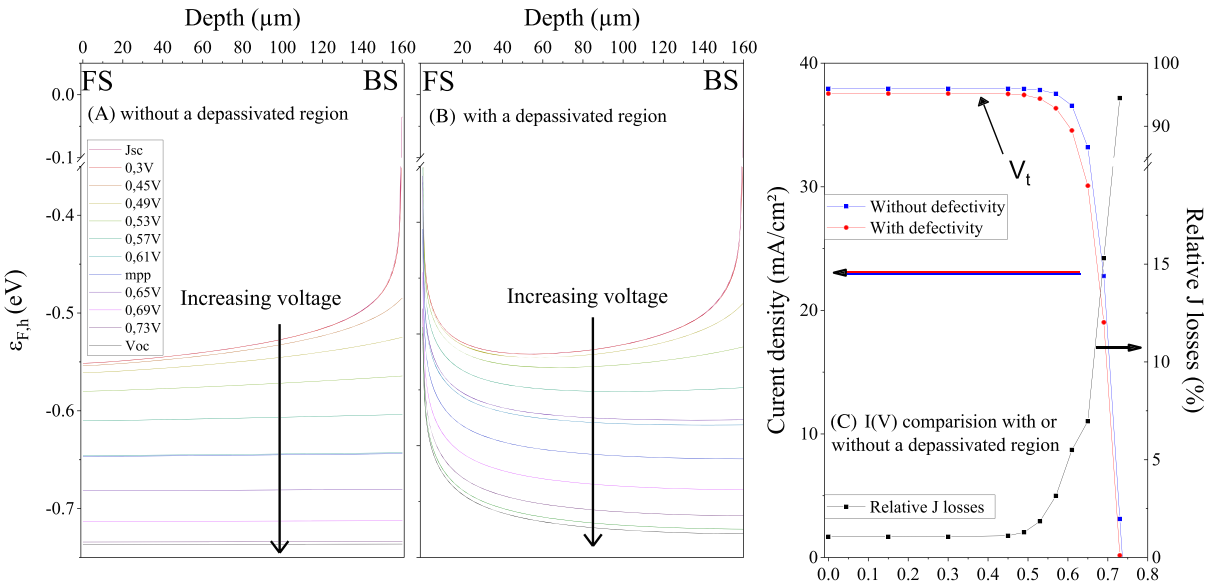

FIGURE 4 Vertical profiles of the hole quasi-Fermi level $\varepsilon_{F,h}$ (relative value with respect to its value in the structure at the equilibrium) along the c-Si thickness from the front side FS (left) to the back side BS (right) without (A) or with (B) a depassivated region at the front *a*-Si:H/*c*-Si interface at several working points under a AM1.5G illumination. *I*(*V*) measurement for cells with or without a depassivated region and the associated current relative losses are plotted in (C)

From this figure, the frontier line between the regions near the front surface where the holes flow to the depassivated area (red zone) and where they flow to the back side (green zone) is situated at a distance $L < 120\mu$m from the depassivated region in the first microns from the front *c*-Si interface. However, the red zone does not cross the whole cell depth, and considering that the photogeneration can not be assumed to fully occurs in the vicinity of the front *c*-Si interface, it is necessary to combine a photogeneration profile along the whole cell height to this map in order to determine the fraction of photogenerated carriers lost by recombination at the defect.

In order to estimate the fraction of carriers lost by recombination at the defect, the cumulated photogeneration within the red zone was subtracted to the cumulated photogeneration in the whole cell. This leads to 1.2% of the photogenerated carriers lost by recombination at the defect. Thus, the short circuit current losses are expected to be 1.2% in relative, which is again consistent with the results presented in Figure 3.

Finally, let us transpose the analysis for the η losses. At the maximal power working point, the $\vec{\nabla}\varepsilon_{F,h}$ was analysed in the same way as for the J_{sc}. It appears that 6% of the photogenerated carriers are lost through recombinations on the depassivated region. This observation leads to the conclusion that the efficiency losses are expected to be about 6% which is again consistent with the results presented in Figure 3. Furthermore, the cell-produced power relative losses are given by $\Delta P = \Delta V_{oc} + \Delta J_{sc} + \Delta FF$; it can be deduced that the *FF* losses are about 3.6% which is consistent with the results in Figure 3.

4 | EFFECTS OF THE DEFECTIVITY SPATIAL DISTRIBUTION

In the previous part, the studied defectivity spatial distribution was not representative of that of an actual cell. In order to better understand the defectivity-related issues in actual cell we studied the influence of the defectivity spatial distribution on the minority carriers current and thus the device performances. To this aim, a textbook case has been studied. In the first time, using the scratch creation protocol presented in Section 2.1, eight evenly spaced 37±5μm width scratches were made on two SHJ cells before I(V) measurements were performed. Subsequently, on the first device, some scratches were expanded up to 0.7-mm width. Not all scratches were enlarged, to prevent the cell from breaking. After each scratch enlargement, *I*(*V*) measurements were performed. On the second cell, the number of scratches was doubled leading to sixteen 37±5μm width scratches

uniformly distributed on the cell front face. The measured efficiency losses with successive enlargements and the efficiency of a cell with sixteen 37-μm uniformly distributed scratches are plotted in Figure 5. It is important to note that the η losses are more severe with the 16 uniformly distributed scratches, whereas the total scratched area is five times lower than that of the cell with enlarged scratches. This shows that the defectivity spatial distribution strongly modulates the influence of defectivity. The spatial concentration of defectivity is clearly a way to mitigate its influence, if defectivity can not be suppressed. Every transportation means (trays, belts, grippers, etc.) should be engineered so as to reduce and concentrate defectivity.

In order to understand this result, let us study the hole current densities around the depassivated region presented in Figure 6. This figure allows to bring to light two distinct recombination behaviours. On the one hand, around the depassivated region edges, the hole current densities are very high. Indeed, the defect attracts photogenerated carriers from the whole affected area, which is much wider than the defect itself (Figure 10). These carriers photogenerated far from the depassivated region are recombined by the depassivated region edges as soon as they reach them. On the other hand, the hole current densities under the central part of the depassivated region are much lower and directed straight towards the depassivated region. We conclude from that, that the depassivated region central part only allows the recombination of the carriers photogenerated directly below it.

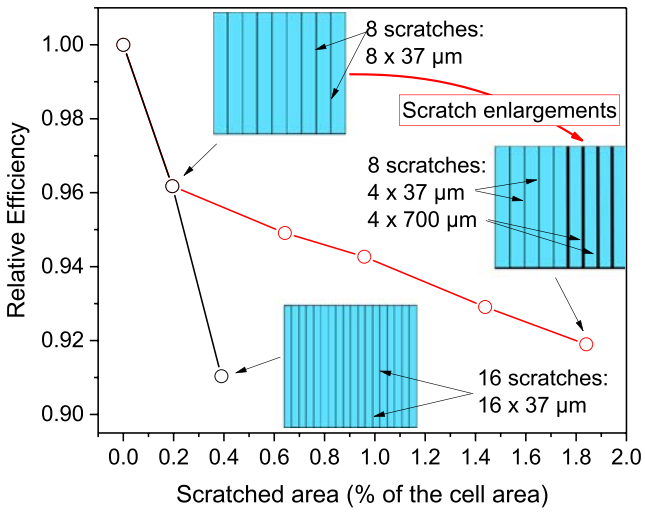

FIGURE 5 Comparison of efficiency losses with (grey) and without (red) defectivity spatial concentration

These observations led to study the influence of the depassivated region width on the induced cell parameters losses. Figure 7 depicts the variation of the efficiency losses induced by a defectivity distribution similar to that presented in Figure 2 for several depassivated region width. The trend is divided in two distinct regions. On one hand, when the depassivated region width is greater than 20 μm, the thinning of the depassivated region has a linear influence on the performance losses since the little recombination-active depassivated region central part is still present. On the other hand, when the depassivated region width is below 20 μm, the efficiency of the cell greatly increases with the thinning of the depassivated region, since the two highly recombination-active regions on the depassivated region edges start to merge. Indeed, for a very thin depassivated region, the recombination rate does not allow to recombine as many carriers as a bigger depassivated region would. Thus, the depassivated region-induced $\varepsilon_{F,h}$ increase at its vicinity is lower compared to that of a larger depassivated region. Consequently, at a given position in the *c*-Si, the $\vec{\nabla}\varepsilon_{F,h}(def)$ contribution to $\vec{\nabla}\varepsilon_{F,h}$ is reduced for thinner depassivated regions leading to a better carrier extraction. Consequently, a 100-μm-wide depassivated region will for instance be less detrimental to the cell performances than a distribution of twenty 5-μm-wide independent depassivated regions.

As a conclusion, in order to mitigate the defectivity effects for a given total depassivated surface, the depassivated regions width

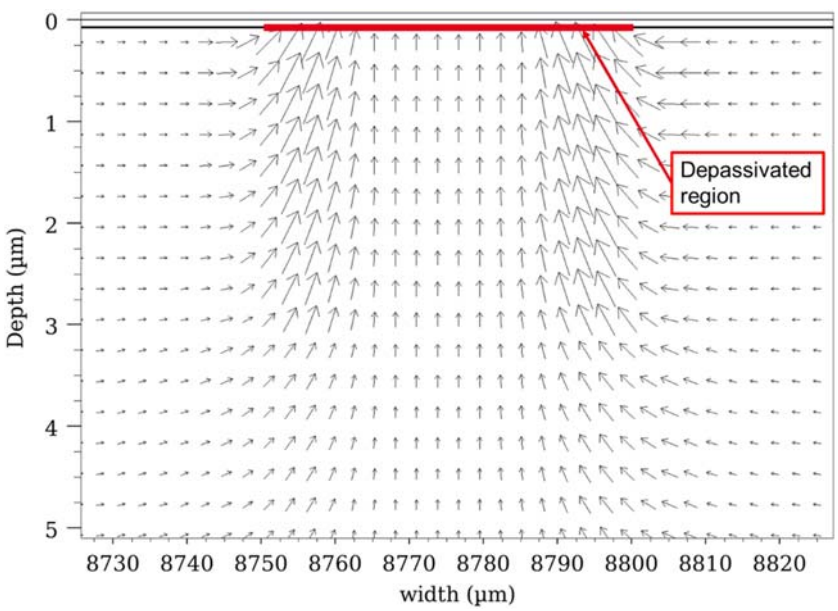

FIGURE 6 Map of hole current densities at the open circuit working point, in the *c*-Si around the depassivated region. The current densities are proportional to the length of the arrows

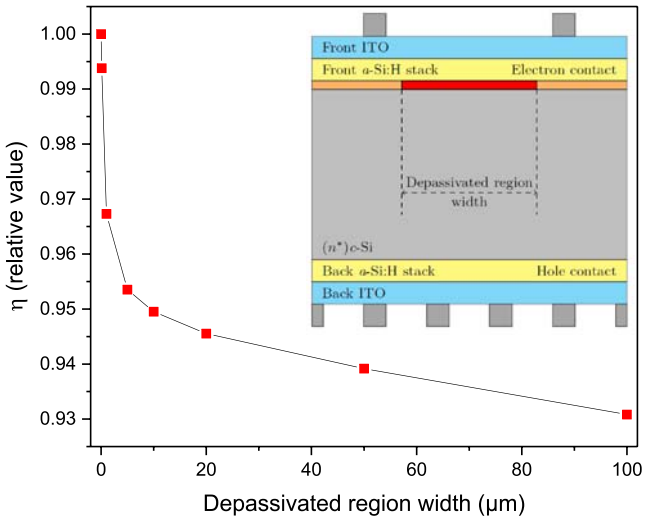

FIGURE 7 Variation of the defectivity-induced performance losses when varying the width of the front-side depassivated region

should be greater than 20 μm. As an illustration, the clipping of the pyramids by friction during the manufacturing steps, generating depassivated many regions of a few microns, constitutes the worst possible defectivity spatial distribution.

In order to improve the understanding of the defectivity-related issues, it is still necessary to study the case of two depassivated regions sufficiently close to each other so that their affected areas may overlap. This configuration echoes the one found in the defectivity induced by the belts on production lines (see Figure 1).

Given that the area affected by a single scratch increases with the bias voltage, the overlap width increases in the same way. In order to study this phenomenon, simulations were run with two depassivated regions implemented at the front *a*-Si:H/*c*-Si interface. Figure 8 shows the variation of the efficiency losses with the distance between the two depassivated region edges ($d_{inter-def}$). This graph can be divided into two regions bounded by a critical value of $d_{inter-def}$:

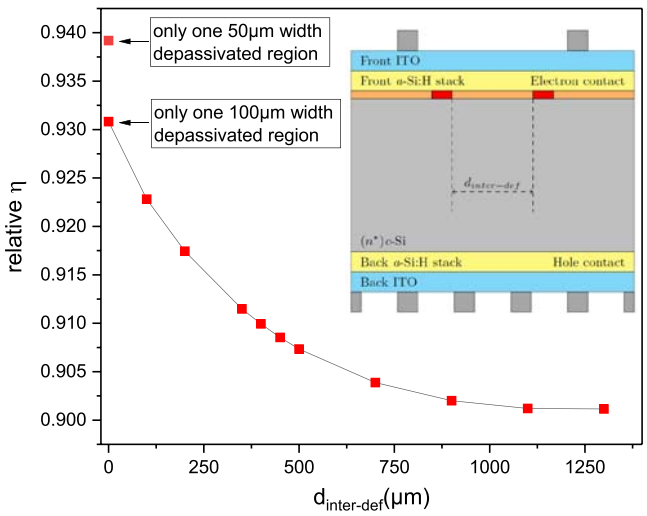

FIGURE 8 Variation in efficiency losses with two depassivated regions per unit cell implemented at the front *a*-Si:H/*c*-Si interface as a function of the distance between them

- When $d_{inter-def}$ is greater than ≈1 mm, the critical value the depassivated regions induced η losses reach a plateau
- When $d_{inter-def}$ is lower than ≈1 mm, the decrease of $d_{inter-def}$ induces a reduction in η losses.

This is consistent with the results presented in Giglia et al[7] considering that the η increase would be explained by the overlap of the regions affected by the depassivated regions which leads to reduce the total affected region. Thus, the defectivity spatial concentration has beneficial effects only if $d_{inter-def}$ is lower than 1000 μm (for the cell parametrization presented in Section 2).

This result is dependent on the *c*-Si properties, and thus, the critical $d_{inter-def}$ has to change with the bulk properties. However, as a general rule, it can be predicted that the critical value of $d_{inter-def}$ is expected be a little lower than the carrier diffusion length.

Another observation can be made from Figure 8. The η losses are not doubled between the case of a single depassivated region and the one of two independent depassivated regions. This phenomenon, existing because of the presence of a high defectivity surfacic density, will be explained in Section 5.

In conclusion, the defectivity spatial concentration, for a given total depassivated surface, can allow to mitigate the defectivity-induced performance losses. Furthermore, the study of the combination of Figures 7 and 6 taught us that two depassivated regions should be separated from each other by a distance smaller than 1 mm in order to mitigate the defectivity effects for the cell parameters presented in Section 2.

5 | EFFECTS OF THE DEFECTIVITY LOCALIZATION (FRONT SIDE VS. BACK SIDE)

The aim of this section is to compare the effects of a front side and a back side localized defectivity. For that purpose, a depassivated region was implemented in the simulation structure presented in the above,

first at the front (n)*a*-Si:H/(n)*c*-Si and then, at the back (p)*a*-Si:H/(n)*c*-Si interface.

In order to unveil the trends of the *I*(*V*) parameters losses dependence with the defectivity localization, several defectivity densities were simulated. In order to vary the defectivity density, the space between two successive scratches was set to nine, five, three and finally one intermetallization pitches (corresponding respectively to 16, 27 and, finally, 81 scratches or alternatively to 0.6%, 0.9% and 3% of the cell area). To achieve similarly high defectivity densities, the cells were this time rubbed together. Figure 9 is a plot of *I*(*V*) parameters losses induced for several defectivity densities obtained by both simulation and experimental measurement. It is important to notice that the abscissa axes are not the same, the two different defectivity spatial distributions (scratches vs. rub-induced defectivity) being hardly comparable (according to Section 4). The defectivity density for the measured cells was estimated by the method presented in Nos et al.[5] However, this figure allows to compare the *I*(*V*) parameters losses trends for a back side or a front side defectivity as a function of its density.

The results plotted in Figure 9 show that the efficiency losses are nearly the same whether the defectivity was implemented at the front or the back (n)*c*-Si/*a*-Si:H interface. However, although the V_{oc} losses are the same in both cases, the J_{sc} and *FF* losses have significantly different behaviours depending on the defectivity localization. Indeed, a back *a*-Si/*c*-Si interface defectivity tends to more dramatically affect the *FF* than a front side defectivity. Regarding the J_{sc} losses, the opposite holds true. Thus, the similarity of the efficiency losses in these both cases is in fact due to a compensation between the J_{sc} and *FF* losses behaviours.

These observations are explained in the following, on the basis of the analysis of $\vec{\nabla}\varepsilon_{F,h}$. In the first time, as explained in Section 3, at V_{oc}, $\vec{\nabla}\varepsilon_{F,h}$ has only one component directed towards the depassivated region because $\vec{\nabla}\varepsilon_{F,h}(collect)$ vanishes at V_{oc}. Thus, at V_{oc}, $\vec{\nabla}\varepsilon_{F,h}$ is only governed by the depassivated region properties. Furthermore, the diffusion length L_D is much greater than the wafer thickness. Thus, although the carrier are mainly photogenerated near the front *a*-Si:H/*c*-Si interface, they are virtually as likely to reach a front side or a back-side depassivated region. Consequently, the hole current densities at the open circuit working point (Figure 10E,F) are equally impacted by a depassivated region whether it is located at the front or the back side of the cell. Thus, the defectivity localization does not impact the induced V_{oc} losses.

In the second time, at the J_{sc} working point, the area affected by the depassivated region is very little extended (Figure 10A). As photogeneration mainly occurs near the front *a*-Si:H/*c*-Si interface, the carriers are more likely to recombine on the depassivated region if this region is located at the front *c*-Si/*a*-Si:H interface, which explains why the J_{sc} losses are more important with a front side defectivity. To illustrate that, hole current density maps are plotted in Figure 10A,B with a depassivated region at the front side or the back side of the cell at the short circuit working point. It appears that only the carriers photogenerated directly above the depassivated region are lost through recombinations. Indeed, in Figure 12, we show that $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ in the *c*-Si bulk increases along the cell depth (rear emitter configuration). Consequently, at given spatial coordinates in relation to a depassivated region, $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ is greater if this depassivated region is located at the back side of the cell. At the short circuit working point, with a front-side depassivated region, the competition between $\vec{\nabla}\varepsilon_{F,h}(def)$ and $\vec{\nabla}\varepsilon_{F,h}(collect)$ was shown to be very strong (see Section 3). The same situation transposed to the back side of the cell where $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ is greater, makes the $\vec{\nabla}\varepsilon_{F,h}(def)$ contribution to $\vec{\nabla}\varepsilon_{F,h}$ negligible. This is why, for a back-side depassivated region, only the carriers photogenerated above the depassivated region itself recombine at the defect.

Finally, in order to study the FF losses, a study of $\vec{\nabla}\varepsilon_{F,h}$ can be carried out at the maximum power point (P_{mpp}). The study of Figure 4A shows that $\vec{\nabla}\varepsilon_{F,h}(collect) \neq \vec{0}$ at this working point. Thus, the total $\varepsilon_{F,h}$ gradient is $\vec{\nabla}\varepsilon_{F,h} = \vec{\nabla}\varepsilon_{F,h}(collect) + \vec{\nabla}\varepsilon_{F,h}(def)$. In order to understand the differences between the front side and back side

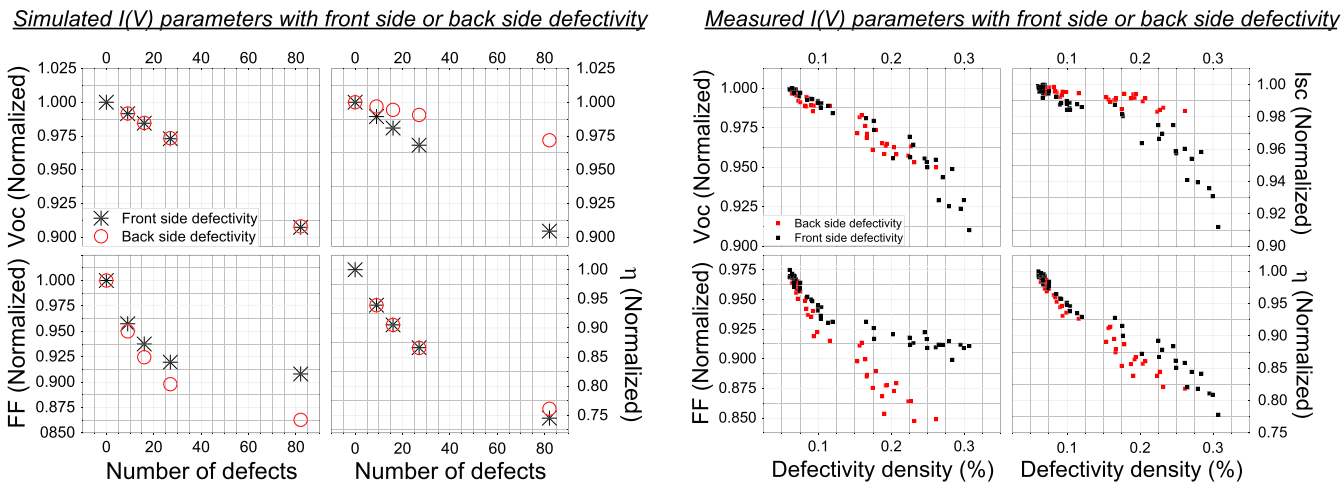

FIGURE 9 Comparison between the effects of front side and back side defectivity as a function of the defectivity level. Normalized simulated *I*(*V*) parameters are plotted on the left, and normalized experimental *I*(*V*) parameters are plotted on the right. The defectivity scales are not the same. This figure is intended to depict the trends of the defectivity effects

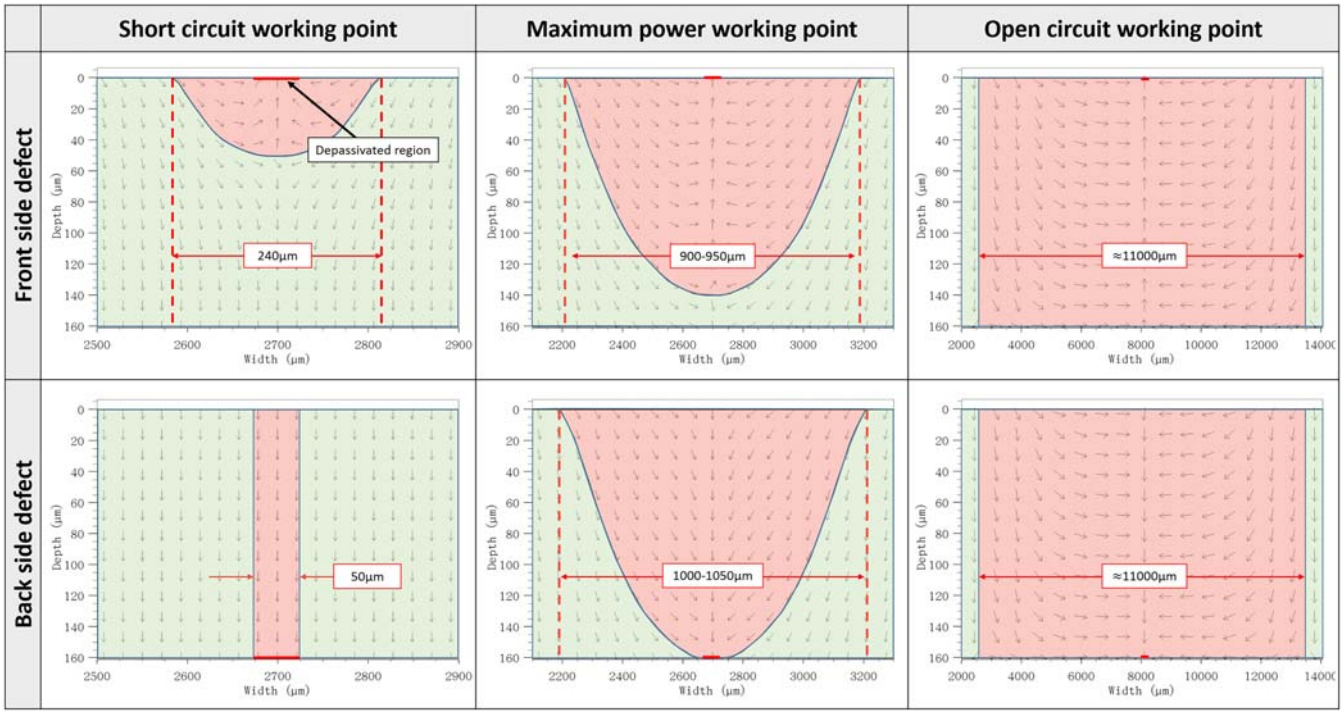

FIGURE 10 Hole current density map within the *c*-Si for a cell with a front side or a back-side depassivated region at the short circuit, maximum power and open circuit working points. The red zone on each graph illustrates the impact of the depassivated region on the current flows

defectivity effects on the FF, this vectorial sum was studied with a depassivated region at the front or at the back *c*-Si interface.

Contrary to $\vec{\nabla}\varepsilon_{F,h}(collect)$, $\vec{\nabla}\varepsilon_{F,h}(def)$ can be divided into two components: $\|\vec{\nabla}\varepsilon_{F,h}(def,x)\|.\vec{ex}+\|\vec{\nabla}\varepsilon_{F,h}(def,y)\|.\vec{ey}$ the x direction being the horizontal axis and the y direction is the vertical axis on Figure 2. It can be noticed that the vertical component $\|\vec{\nabla}\varepsilon_{F,h}(def,y)\|$ is added to $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ if the depassivated region is located at the back *c*-Si interface and subtracted to $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ if the depassivated region is at the front *c*-Si interface. This difference between a front and a back-side depassivated region induces a modification of the current density map as shown in Figure 10C,D. When the defect is located on the front side, owing to the competition between $\vec{\nabla}\varepsilon_{F,h}(def,y)$ and $\vec{\nabla}\varepsilon_{F,h}(collect)$, there is a specific depth in the *c*-Si, under the depassivated region, where $\vec{\nabla}\varepsilon_{F,h}(def,y)=-\vec{\nabla}\varepsilon_{F,h}(collect)$. This leads to an inversion of the hole current density direction under the front side. With a back-side depassivated region, this inversion is not observed as both gradients are collinear.

As a result, at this bias voltage, the collected current losses are more important with a depassivated region located at the back *c*-Si interface leading to more important *FF* losses.

In addition to this, it can be noticed that, for high defectivity densities, the efficiency losses are not directly proportional to the number of scratches even if the distance between two consecutive scratches is higher than the carrier diffusion length and that therefore, all defective areas are independent of each other. In order to explain this observation, let us look at the J_{sc}, V_{oc} and *FF* trends. The J_{sc} and V_{oc} losses are directly proportional to the number of scratches unlike the *FF* losses. The nonlinearity of η losses with the number of scratches is due to the *FF* losses behaviour. When the defectivity density increases, the *FF* and, thus, the maximum power voltage V_{mpp} also decrease. However, as exposed in Figure 4, when the bias voltage decreases, $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ contribution to $\|\vec{\nabla}\varepsilon_{F,h}\|$ increases. Thus, the attraction of the hole towards a given depassivated region tends to decrease if the cell defectivity density increases. This explains why the *FF* decreases at a slower rate when the number of scratches increases.

6 | INFLUENCE OF SUBSTRATE PROPERTIES ON THE DEFECTIVITY-INDUCED PERFORMANCE LOSSES

In view of all the understanding presented above, the substrate properties are expected to modulate the defectivity-induced performance losses. In order to quantify these modulations, simulations were performed with several values for the doping and τ_{p0} (hole capture characteristic time) defined as $\tau_{p0}=\frac{1}{N\sigma_p v_{th}}$ where N is the density of recombination centres, σ_p, their cross section and v_{th} is the thermal velocity (10^7 cm/s). Figure 11 depicts the simulation results.

First of all, in agreement with our previous results, it must be noticed that, for several *c*-Si and defectivity properties, the performance losses are almost the same with a front side or a back side defectivity thanks to the compensation of the variation of J_{sc} and *FF* losses. In a second time, it can be noticed that the performance losses tend to increase with increasing holes lifetimes. This result

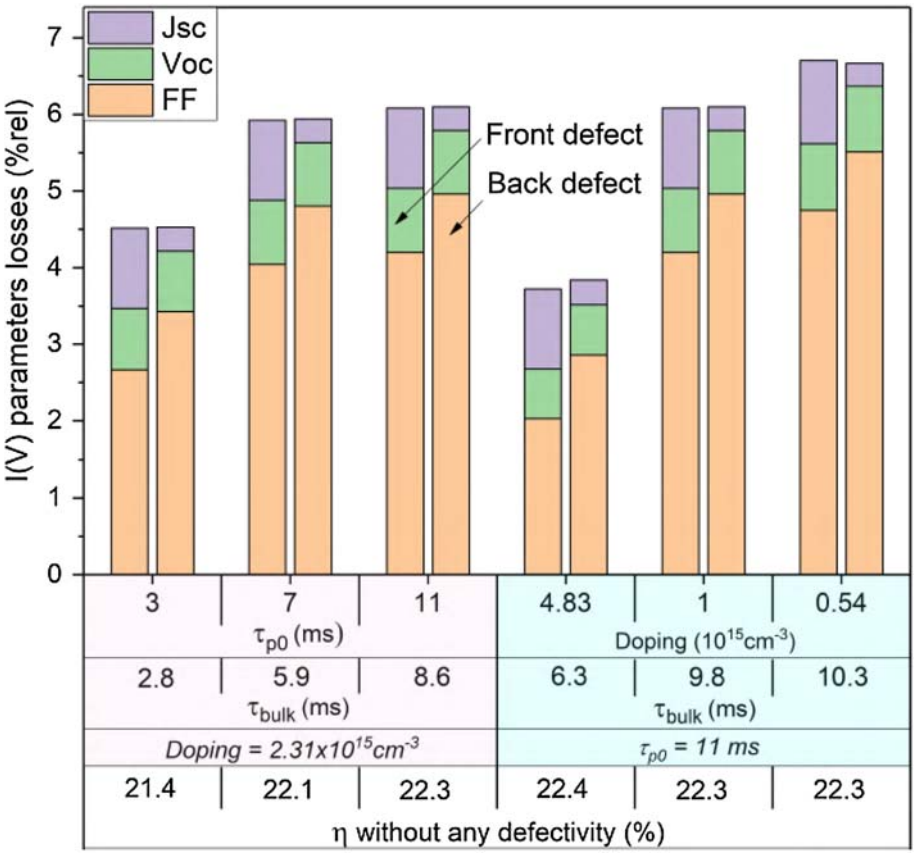

FIGURE 11 Variation of simulated efficiency losses split in *I*(*V*) parameters losses with wafer properties for a front side or a back side defectivity. τ_{bulk} was calculated separately for $\Delta n = 5 \times 10^{14}$ cm^{-3}

highlights the importance of defectivity study. Indeed, with the ongoing improvement of wafer quality, the importance of the defectivity effects on the whole cell performances becomes even more relevant.

Concerning the effects of the *c*-Si doping on the defectivity-induced performance losses, our results reveal that *c*-Si wafers with higher doping could reduce the defectivity effect as well. It must be also noticed that the variation of doping and τ_p mostly impacts the *FF* losses. The V_{oc} and J_{sc} losses are virtually the same for each condition. This is still consistent with the results presented in Section 3. Indeed the high hole lifetime eases the carrier transit towards the defect leading to an increase of the current towards the depassivated region at a given bias voltage and, thus, to large FF losses.

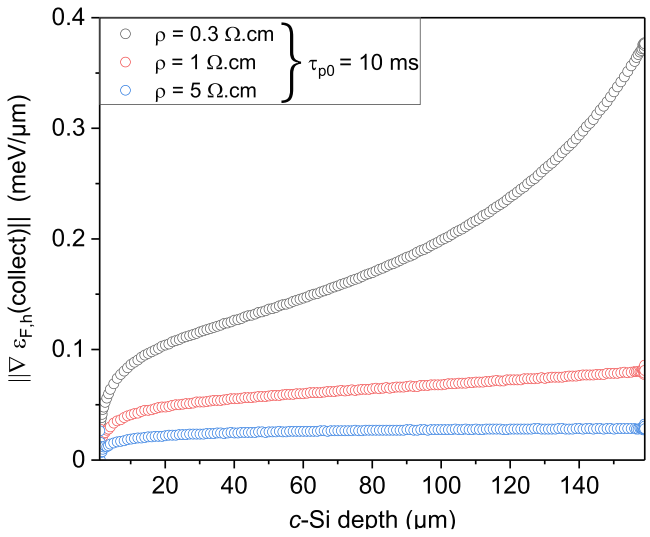

FIGURE 12 profile of $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ along the *c*-Si depth for several resistivity values for a given $\tau_{p0} = 10ms$ and bias voltage=610mV

The influence of the *c*-Si resistivity on the defectivity-induced losses is still to be studied. The simulation software allows to plot the band diagram within the *c*-Si for several wafer resisitivities and for a given τ_{p0}. For increasing resistivities, the electrical neutrality equation requires the band bending at the rear *c*-Si/*a*-Si interface to increase. Consequently, as depicted in Figure 12, $\|\vec{\nabla}\varepsilon_{F,h}(collect)\|$ is likely to increase at a given bias voltage for lower resistivity wafer-based SHJ cells. Thus, in case of a depassivated region at the *c*-Si interfaces, for a given bias voltage, the $\vec{\nabla}\varepsilon_{F,h}(def)$ relative contribution to $\vec{\nabla}\varepsilon_{F,h}$ is lower for low resistivity wafer-based SHJ cells (for a given τ_{p0}).

In addition, on Figure 12, it can be noticed that, for decreasing resistivities, the defectivity-induced performance losses are mitigated whether it is located at the front or the back *c*-Si/*a*-Si interface. This can be explained on the basis of the results presented in Section 5. In the case of a depassivated region located at the back *c*-Si/*a*-Si interface, $\vec{\nabla}\varepsilon_{F,h}(collect)$ drives holes towards the depassivated interface. In the case of a front *c*-Si/*a*-Si interface located depassivated region, $\vec{\nabla}\varepsilon_{F,h}(collect)$ drives the holes even more efficiently, with decreasing resistivities, away from the depassivated region. One could think that, for decreasing resistivities, holes are even more likely to recombine at a back-side depassivated region given that $\vec{\nabla}\varepsilon_{F,h}(collect)$ tends to drive holes towards the depassivated region. However, holes which are in the vicinity of the back-side depassivated region experience a strong $\vec{\nabla}\varepsilon_{F,h}(collect)$ induced force towards the emitter. This force allows them to be collected rather than being recombined. This is the reason why the mitigation of the defectivity-induced losses are virtually the same whether the depassivated region is located at the front or the back *c*-Si/*a*-Si interface.

7 | CONCLUSIONS AND PERSPECTIVES

In this work, we investigated by means of experiments and simulations the impact of local surface defectivity on the SHJ solar cell performances. First, a protocol of controlled defectivity formation was established, which was subsequently used to investigate the influence of incremental defectivity creation on all *I*(*V*) parameters. This first experimental study demonstrated a strong effect on the efficiency, amounting to −6%rel for 'only' 0.2% of the surface being defective, mostly driven by an FF loss. In the second part, we resorted to numerical simulations in order to explain the physical mechanisms behind this effect. In the first step, the ability of simulation to predict the cell degradation was ascertained by comparison with experimental values on a textbook case. Simulation results were then trusted further, and a deeper analysis was carried out on the basis of the calculated quasi-Fermi level mappings throughout the cell. In particular, we evidenced how the depassivated region at the cell front side creates a bias voltage-dependent current towards itself and explained how this reduces the overall cell performances. Then the influence of the defectivity spatial distribution has been studied. First, we have brought to light that the defectivity spatial concentration, for a given total defectivity density, allows to efficiently mitigate the defectivity-induced losses. It has been shown that the effects of two depassivated regions can be greatly reduced if the distance between them is lower than 1 mm for the considered *c*-Si bulk properties. In the second time, the differences between a front and back side defectivity-induced performance losses were studied. In particular, we highlighted a similar qualitative influence for both type of defectivity (front and back side) with however different contributions of J_{sc} and *FF* to the overall η losses. In light of the understanding of the mechanisms behind the defectivity-induced performance losses, solutions were proposed to reduce these losses, for example, the choice of higher resistive *c*-Si wafers or re-engineering some production equipments in a way to spatially concentrate the defectivity if it cannot be totally suppressed.

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