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Reliability Analysis of NAND-Like Spintronic Memory

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Abstract

This work deals with magnetic tunnel junction (MTJ) based non-volatile memories (NVMs) and focuses on radiation issues. We investigate the Single Event Transient (SET) effects on a 28 nm FDSOI NAND-SPIN. The objective is to check the influence of the common current path in the metal strip of NAND-SPIN shared among various MTJs in terms of SET impact. The critical charge is determined according to the SET striking time and hardening strategies that improve the write operation robustness against SETs are proposed.

1. Introduction

Magnetic tunnel junction (MTJ) based non-volatile memories (NVMs) have been widely considered as a candidate for the future memories due to their outstanding performance in terms of high density, infinite endurance, and switching energy efficiency [1, 2, 3]. Although the intrinsic magnetic storage device MTJ has high tolerance to radiation [4], the MOS access transistors used in MTJ-based memory structures are prone to radiation effects such as transient disturbances called Single Event Transient (SET) [5]. A SET occurring at the MOS transistor can lead to incorrect value stored in the magnetic random access memory (MRAM) cell [6, 7]. Downscaling transistors to nanometers makes them more vulnerable to SET [8] and thereby makes MTJ-cell more prone to errors.

The structures of MTJ based MRAM reported in the literature differ in the number of MOS transistors and the write operation approach [2, 9, 10]. The spin transfer torque magnetic tunnel junction based MRAM (STT-MRAM) requires only one transistor per bit-cell allowing higher density memories, but it has a considerable asymmetry in the write operation [9, 11]. On the other hand, the SOT-MRAM presents almost symmetric write operation, but requires two access transistors for each bit-cell, which reduces its integration density capacity [2, 10]. Recently, a memory device called NAND-SPIN has been proposed [2]. This structure includes two unidirectional currents for writing, which leads to better energy performance compared to STT-MRAM approach. Also, MOS transistors are shared by several MTJ devices, allowing the NAND-SPIN memory integration density to overcome the one obtained with SOT-MRAM.

This work addresses MRAM radiation issues and focuses on NAND-SPIN structures, as SET effects on STT-MRAM and SOT-MRAM have been reported in [5, 12]. We investigate the SET effects on a 28 nm FDSOI NAND-SPIN. The influence of the common current path in the NAND-SPIN shared among the MTJs is analyzed in terms of SET impact. Moreover, some hardening strategies are proposed in order to improve the write operation robustness of the NAND-SPIN against SETs.

The rest of the paper is organized as follows. Section 2 briefly explains the MTJ as well as the MTJ based memories devices. The SET model is described in Section 3. Simulation results are presented and discussed in Section 4. Finally, Section 5 concludes the work.

2. Basics on MTJ based Memories

2.1. Magnetic Tunnel Junction (MTJ)

Fig. 1 illustrates the basic MTJ structure. It is composed by two ferromagnetic layers (the reference layer and the free layer) separated by the insulator layer MgO [13]. The magnetization direction of the reference layer is fixed, while the free layer has the magnetization direction changed due to a polarized switching current. The magnetic field switches the MTJ resistance. That is, MTJ resistance depends on the orientation of MTJ magnetization with the parallel (P) and anti-parallel (AP)

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states. Low-resistance state is achieved with parallel magnetization, while anti-parallel magnetization leads to a high-resistance. MTJ can be integrated in memories and logic circuits to represent logic 0 or logic 1 [14].

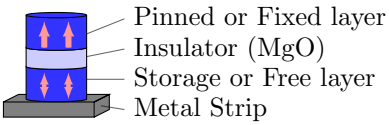

Fig. 1: Magnetic tunnel junction (MTJ).

2.2. STT-MRAM and SOT-MRAM

Fig. 2a illustrates the STT-MRAM bit-cell structure. It is composed by 1 NMOS and 1 STT-MTJ. A bi-directional current I_w is responsible to write in the MTJ, that is, to switch between the AP and P states. During the read operation, a read current I_r flows through the MTJ and its state is defined comparing I_r with a reference current [15].

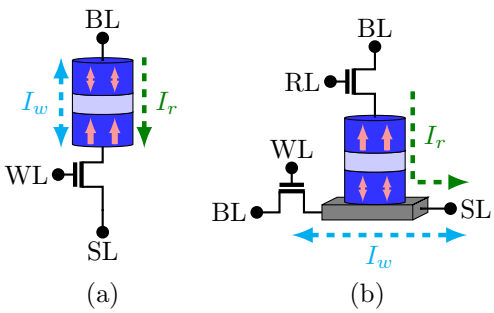

Fig. 2: Memories devices: (a) STT-MRAM (b) SOT-MRAM.

The typical SOT-MRAM bit-cell structure composed by 2 NMOS and 1 SOT-MTJ is shown in Fig. 2b. During the write operation, a voltage is applied between the source line (SL) and the bit line (BL) to generate I_w (write current). This current will be polarized and will switch the magnetization direction of the free layer. As can be noticed in Fig. 2b, the write path and the read path are different. That is, in a read operation, the read current I_r flows through the MTJ. The state of the MTJ is read according to the magnitude of I_r [16].

2.3. NAND-SPIN

The NAND-SPIN structure was proposed in order to achieve a high storage density and low write energy [2]. Fig. 3 illustrates a 4-bit NAND-SPIN structure. Each pinned layer of the MTJ is connected to an access transistor. And all free layers of the MTJ are contacted with the heavy metal strip. Moreover, two other transistors are required: PT (PMOS transistor) and NT (NMOS transistor). They are located on the ends of the heavy metal strip.

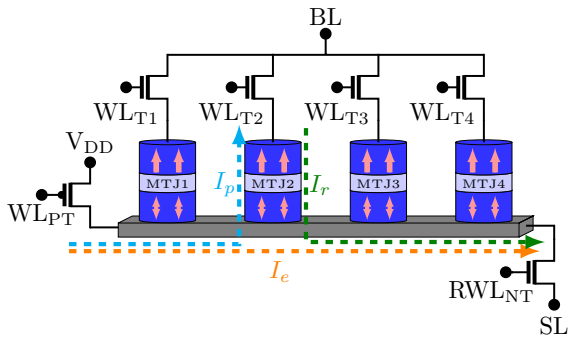

Fig. 3: 4-bit NAND-SPIN structure.

Fig. 4 gives the timing diagram for the read and write operations over MTJ1.

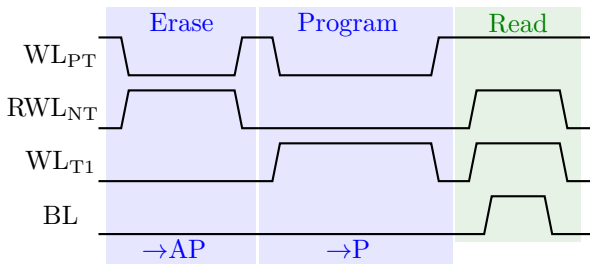

Fig. 4: Timing diagram of write and read operations for the NAND-SPIN over MTJ1.

As can be seen, there are two steps for a write operation in NAND-SPIN:

- erase step: the contents in the MTJs are erased and the MTJs are initialized at AP states. PT and NT are on and the access transistors are off. A write current I_e is generated in the shared metal strip.
- program step: the MTJ that attempts to be written is switched to its P state. In order to do this, PT and the corresponding access transistor are on. The state is switched to P by the STT mechanism, that is, a current I_p flows through the MTJ from the free layer to the pinned layer.

Fig. 5 illustrates the write operation on MTJ3. mz_i is the magnetization orientation of MTJi. The corresponding P and AP states are represented by $mz \approx 1$ and $mz \approx -1$, respectively. In this example, the initial states of the MTJs are different. However, after the erase step,

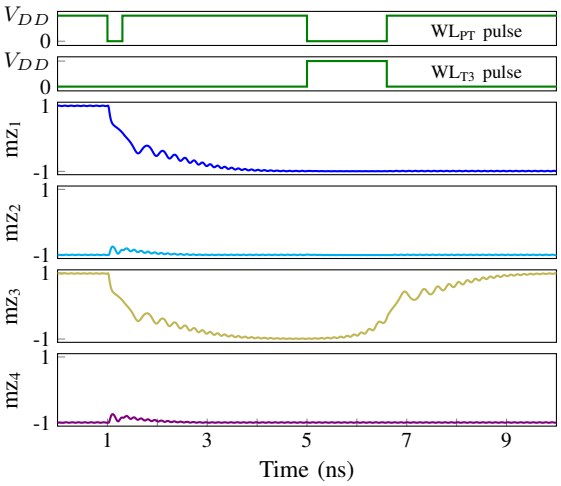

Fig. 5: Timing diagram of write operation on MTJ3.

all MTJs go to AP state. And after the program step, only MTJ3 changes to P state ($mz \approx 1$).

During the read operation, NT as well as the access transistor that corresponds to the MTJ concerned by the read operation are on. Then, the MTJ state is read comparing I_r with a reference current.

3. SET Model and Simulations Setup

3.1. SET model

The current $I_{inj}(t)$ defined by (1) is the most widely used model for describing a SET, that is, a SET is represented by a double-exponential current pulse $I_{inj}(t)$ on the transistor [17, 18]. Q_{inj} is the charge injection level calculated by (2), τ_1 is the collection time constant for a junction, τ_2 is the ion track establishment time constant, and K is related to the material characteristics and the radiation intensity [17, 18].

$$I_{inj}(t) = K.(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}) \quad (1)$$

$$Q_{inj} = \int I_{inj}(t)dt \quad (2)$$

However, TCAD simulations show that the SET-induced current pulse can not be well represented by a simple double-exponential expression for higher Linear Energy Transfer (LET) values [19, 20].

In this work, SET is generated by a voltage-dependent current model based on conventional double-exponential current pulse on the transistor taking into account the voltage across the node [21]. Let V_{DS} be the voltage between the drain and the source of the transistor, the current $I_{inj}(t)$ is defined by (3). This model mitigates the problem generated by independent SET sources (as defined in (1)). In other words, considering the model (3), the current $I_{inj}(t)$ only exists if there is a voltage differential between the source and the drain of the transistor.

$$I_{inj}(t) = K.V_{DS}.(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}) \quad (3)$$

3.2. Simulations Setup

A 28 nm CMOS FDSOI design-kit is utilized to implement and simulate the 4-bit NAND-SPIN memory architecture in Fig. 3. $V_{DD} = 1.2V$, the access transistors have channel width $W = 100$ nm and channel length $L = 30$ nm. The SET charge was varied until 10 fC and the considered MTJ device has design parameters as listed in Table 1 [2].

Table 1
Design specification of MTJ compact model.

Parameter	Value
Free layer thickness	1 nm
Heavy metal thickness	4 nm
Damping factor	0.02
Resistance-area product	$5\,\Omega\,\mu m^2$
Saturation magnetization	$1.15 \times 10^6\ A/m$
Spin Hall angle	0.3
Tunneling spin polarization	0.62
Heavy metal resistivity	$200\,\mu\Omega$ cm
Exchange bias	15 mT

3.3. Failure condition

Write failures occur when the MTJ in the bit-cell does not appropriately switch between parallel and anti-parallel states. In other words, because of the SET, the MTJ does not switch when it has to or the MTJ switches when it should not to do.

Critical charge Q_c is defined as the minimum SET charge that leads to an undesirable MTJ state switching when it reaches the access transistor. To analyze the sensitivity of the circuit against SET, a SET pulse is simulated to strike an access transistor.

Fig. 6 illustrates the occurrence of a SET with 2 fC in T1 in two different striking times. The yellow curve represents the normal operation of MTJ1, that is, after the erase pulse, its state changes from P ($mz_1 \approx 1$) to AP ($mz_1 \approx -1$). The red and the blue curves represent the operation of MTJ1 after a strike at 1.1 ns and 1.2 ns, respectively. As can be seen, even if both strikes have the same charge, an error appears only for the red curve, proving that the failure occurrence depends on the striking time.

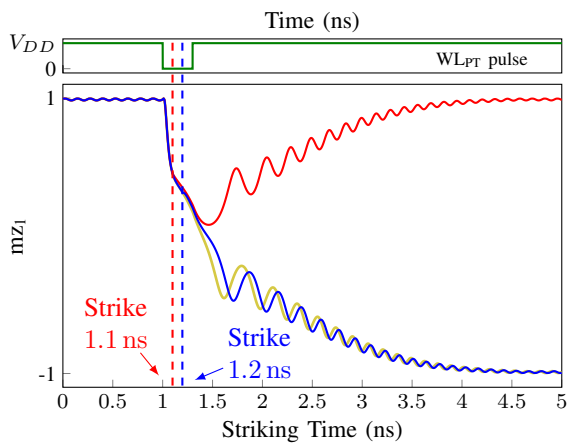

Fig. 6: Time diagram with SET in two different striking time.

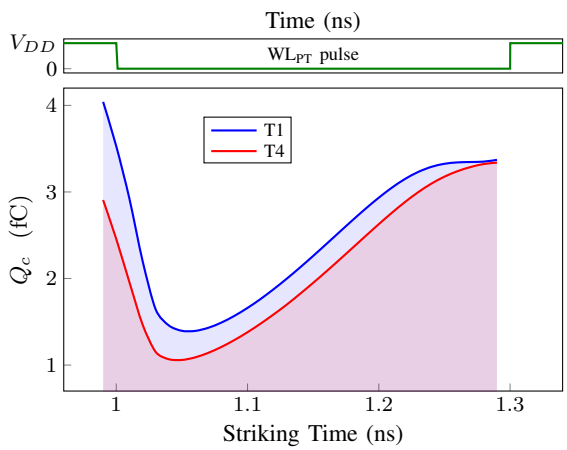

Fig. 7: Value of Q_c during the erase step for Case 1.

4. Simulations Results and Discussions

This section presents the SET analysis on the NAND-SPIN for erase and program steps.

4.1. SET during the erase step

In this step, a correct operation means that after the write pulse, all MTJs will be at AP state. Therefore, a write failure means that at least one of the MTJs is not at AP state. Two (extreme) cases are considered:

- Case 1: all MTJs are at P state before the write pulse.
- Case 2: all MTJs are at AP state before the write pulse.

Fig. 7 shows the Q_c value at different striking times for Case 1. A write pulse is applied in PT (green curve) and the SET is simulated over the transistors T1 (blue curve), T2, T3, and T4 (red curve), one at a time. The striking time is related to the write pulse, that is, striking time equal to 1 ns means that the striking time is exactly at the beginning of the write pulse. The shaded areas represent the safe regions of write operation. In other words, charge values in these regions do not lead to write failure.

This figure also shows that the critical striking time (lowest Q_c value) is 1.05 ns, that is, 50 ps after the beginning of the write pulse. Moreover, different Q_c values are required to lead to a write failure depending on which access transistor is reached by the SET. While a SET with a charge greater than 1.39 fC in T1 can result in a write failure (i.e. at least one MTJ don't switch to AP state), a SET with a charge only greater than 1.05 fC that reaches T4 is enough to lead to a writing error.

Furthermore, it can be noticed that when a SET reaches the access transistor during the write pulse, the circuit is not SET robust (small Q_c can lead to a write failure). On the contrary, if the SET reaches the access transistor before or after the write pulse, even with high level of charge (as big as 10 fC), it does not result in a failure. This is because without write pulse during the erase step, PT and NT transistors are off and no current goes through the MTJs. However, it is worth pointing out that if the SET occurs just before the beginning of the write pulse, it can lead to some write failure, because some charge can be accumulated until the write pulse starts.

Considering Case 2, no failure was observed, even with SET charges up to 10 fC. This shows that the circuit is robust for this configuration.

The obtained results show that the NAND-SPIN is vulnerable during this phase of the write process. A strategy to increase its robustness consists into setting BL to V_{DD} during the write pulse of the erase step, since it prevents any MTJ from getting into P state. In other words, even if a SET reaches an access transistor, it will not generate a current I_p that leads the MTJ to its P state.

4.2. SET during the program step

In this step, a correct operation means that, after the write pulse, the MTJ concerned by the write operation changes its state from AP to P. Therefore, a write failure means that the MTJ concerned by the write operation still continue at AP state or that any other MTJ not concerned by the write operation changes its state. Two representative cases are analyzed:

- Case 1: the MTJ1 is the device concerned by the write operation and the SET reaches T1.

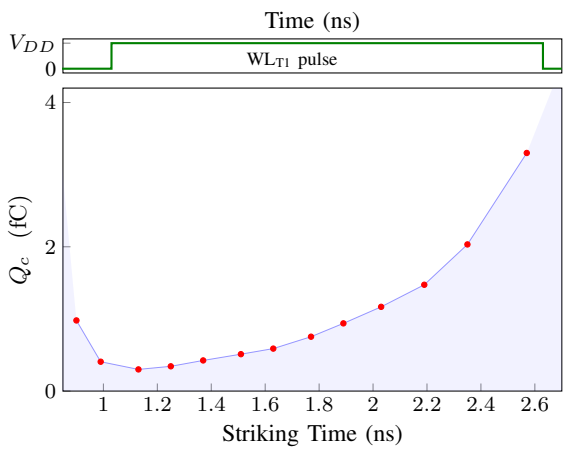

Fig. 8: Value of Q_c during the program step for Case 2.

- Case 2: the MTJ1 is the device concerned by the write operation and the SET reaches T4.

For Case 1, the SET occurrence will not negatively impact the circuit operation because the SET will increase the current I_p. Therefore, MTJ1 will continue to change to its P state and this SET will not influence any other MTJ since the other correspondent access transistors will be off.

For Case 2, three different situations can lead to a write failure:

- The SET generates a current that decreases the current through the MTJ1. This maintains MTJ1 at AP state (that is, a write failure). However, the SET will not change the state of any other MTJ.

- The SET generates a current that decreases the current through the MTJ1. This maintains MTJ1 at AP state (that is, a write failure). Moreover, the SET can change the state of at least one other MTJ so leading at least one other MTJ to P state.

- The SET generates a current that changes the state of at least one other MTJ to P state while maintaining MTJ1 at P state.

The situations above were analyzed varying the SET charge. Fig. 8 shows the Q_c value at different striking times for Case 2. The green curve represents the write pulse in WL of T1. The shaded area represents the safe region of write operation. The critical striking time (lowest Q_c value) is 1.12 ns, that is, 0.12 ns after the beginning of the write pulse. For this striking time, if a SET with charge greater than 0.3 fC reaches T4, it will lead to a write failure.

The results show that the robustness of the NAND-SPIN against SET is highly dependent of the striking time. The SET robustness also depends on the step of the write operation (see Fig. 7 and Fig. 8). Comparing Fig. 7 and Fig. 8 at critical striking time, it can be seen that the critical charge in erase step is bigger than in program step. However, in both steps, the write process is significantly more sensitive to SET effects when the SET occurs during the write pulse, specially during its beginning.

It is worth mentioning that STT-MRAM are prone to writing failures similar to those of the Case 2, since BL and SL are both activated for various bit-cells during the write operation. For example, suppose that the selected device for write operation is MTJ$_a$ and let MTJ$_b$ be another MTJ in any adjacent bit-cell. If a SET reaches the access transistor related to MTJ$_b$, this SET can lead to a change in the MTJ$_b$ value so resulting in a write failure.

The width of the access transistors were changed in order to verify the influence of this parameter on the SET robustness during the program phase. Table 2 presents the critical striking time (T_c) and the corresponding Q_c for Case 2 considering different widths of the access transistors.

Table 2
Critical striking time and Q_c for the program step varying W.

	W = 100 nm	W = 120 nm	W = 140 nm
T_c	1.12 ns	1.12 ns	1.12 ns
Q_c	0.3 fC	1.5 fC	2.7 fC

It can be noticed that any analyzed width value of the access transistors leads to the same critical striking time, suggesting that changes in the width of these transistors do not influence the instant in which critical charge is minimal.

As the access transistors width increases, their current-absorbing capacity is expected to increase due to its bigger capacitance, as seen in Table 2. Hence, transistors resizing may be a suitable strategy to harden NAND-SPIN structure against SET. Despite the area overcost, hardened NAND-SPIN remains less expensive than SOT-MRAM (which requires two transistors per bit-cell).

Another possible improvement consists into modulate the channel lengths (poly-biasing). In order to verify how this variation impacts the SET occurrence, the value of the channel length L of the access transistors was varied. Table 3 presents T_c and Q_c for Case 2 considering W = 140 nm and poly-biasing.

As can be seen in Table 3, not using the minimal value

Table 3
Critical striking time and Q_c for the program step varying L.

	$L = 30$ nm	$L = 34$ nm	$L = 40$ nm
T_c	1.12 ns	1.12 ns	1.12 ns
Q_c	2.7 fC	2.0 fC	0.8 fC

for channel length does not lead to better endurance against SET. On the contrary, the results show that the circuit becomes even more vulnerable to write failure in case of SET.

5. Conclusion

This paper dealt with SET impact on MTJ based memory cells. The vulnerability of the recent NAND-SPIN structure was investigated considering the SET striking time. The obtained results show that NAND-SPIN cell is vulnerable to SET during its write steps. Even if NAND-SPIN has advantages to be employed as a device memory, write failures can happen if protection measures against radiation effects are not taken. To harden the NAND-SPIN against SET, some strategies were proposed and discussed here. They allow NAND-SPIN to become robust against SET without considerable drawbacks. Future works include exploring how variations in MTJ parameters influence the NAND-SPIN robustness against SET as well as more accurate models using TCAD simulations.

Acknowledgement

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