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CSME: A Novel Cycle-Sensing Margin Enhancement Scheme for High Yield STT-MRAM

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Abstract – Spin-transfer torque (STT)-magnetic random access memory (MRAM) requires yield-aware design for hybrid magnetic-CMOS integration. In this paper, a novel cycle-sensing margin enhancement (CSME) scheme with pMOS assisted voltage-type sense amplifier (p-VSA) is proposed to alleviate imperfect process induced performance fluctuations. With iterated charging-discharging through non-volatile data path and reference path, read margin can be significantly improved thanks to the enlarged sensing window. Simulation is performed using MTJ compact model and an industrial 28-nm CMOS process. Results show that with 0.6V supply voltage ~14.1% read yield improvement can be realized at 50% tunnel magnetoresistance (TMR) ratio comparing to conventional VSA.

1. Introduction

Spin-transfer torque (STT)-MRAM demonstrates excellent endurance, retention, fast access speed, and low power switching characteristics [1-3]. It has been used in last-level cache [4-5], embedded systems [6-8], microcontroller unit (MCU) [9] and so on. Non-volatile magnetic RAM (MRAM) design shows high yield requirement due to sub-28-nm CMOS process and sub-100-nm magnetic tunnel junction (MTJ) device applied to hybrid integration [10].

For read operation, STT-MRAM suffers from several read reliability problems caused by physical parameter fluctuations in MTJ and CMOS devices, especially at low supply voltage (V_{dd}) and high temperature scenario. Previous works mainly focused on robust sense amplifier (SA) [11-15] design in order to alleviate variability induced failure.

High- V_{dd} strategy is the most direct and effective method to achieve yield enhancement. Related to MRAM read operation, using above nominal voltage for reading leads to extra power dissipation, the incremental sensing current generates reliability concerns such as read disturbance. Additionally, variability-aware transistor sizing strategy in SA could accordingly suppress the influence of imperfect process. However, increasing the size of SA is also an inappropriate solution in nanoscale technology node because of the serious random dopant fluctuation (RDF) [16-17]. Another solution is to cancel the SA offset voltage (V_{OS}). But many offset cancellation schemes could not effectively cancel V_{OS} and require sensing latency overhead [11].

For energy efficient and fast MRAM read operations, the 2T-2M (two access transistors and two MTJs) bit-cell structure [18-19] is a proper choice. Its differential bit-lines (BL and BLB) enable an enlarged sensing margin. However, 2T-2M STT-MRAM read operations still face the read reliability challenges.

In this paper, we proposed a novel Cycle-Sensing Margin Enhancement scheme named CSME to provide an extended sensing margin window, as well as higher input bit-line voltage difference (V_{in}). The main contributions of this work include:

- Read reliability challenges of STT-MRAM have been surveyed. Previous VSAs in MRAM have been reviewed, including sensing margin/window and bit-line voltage (V_{BL}) swing.
- The CSME scheme using pMOS assisted voltage-type sense amplifier (p-VSA) with dual-transistor sensing is

proposed to overcome imperfect MTJ/CMOS hybrid process induced performance fluctuations.

- The enhanced sensing margin and V_{BL} driving ability benefit read yield improvement, ~14.1% at $V_{dd}=0.6V$ and $TMR=50\%$ with CSME scheme.

The rest of this paper is organized as follows: Section 2 reviews reliability challenges during read operation in STT-MRAM. Section 3 presents the proposed CSME scheme with circuit-level implementation. In section 4, we simulate the proposed scheme and circuits using 28-nm CMOS and MTJ behavioral model. Results are compared with previous VSA. Section 5 concludes this paper.

2. Preliminaries

2.1. STT-MRAM read reliability challenges

Table I lists main reliability concerns during read and write operations of STT-MRAM [20-22]. According to their key causes, the write reliability type can be divided into three categories: transition faults, coupling faults and write polarization asymmetry. The read reliability challenge includes decision fault, read disturb, incorrect read fault and retention failures.

Table I - Writing/reading failure mechanisms and key causes

Affect	Mechanisms	Key cause
Read	Decision Fault	*Process variations *Limited TMR *Low supply voltage
	Read Disturb	*Read and write share the same path *Growing with technology scaling
	Incorrect Read Fault	*Opposite Temp. dependence resistance *Parasitic effects *Short sensing margin window of VSA
	Retention failures	* Intrinsic thermal instability * Thermal noise
Write	Transition faults	*Stochastic nature of write operation *Thermal Fluctuations
	Coupling faults	*Neighboring cells switching
	Write polarization asymmetry	*P to AP needs higher switching current *The writing time required varies

In this work, we concentrate on read operation. Table II shows the main physical parameters affecting the read reliability of MRAM [20]. Among them, the finite TMR is a key macroscopic parameter which determines the margin during sensing. The limited TMR generates similar parallel resistance (R_P) and antiparallel resistance (R_{AP}) value, which causes an overlapped R_P/R_{AP} distribution in their tail regions. Even if MRAM sensing block is implemented with an ideal reference cells, SA cannot distinguish high and low states of MTJ.

Table II – Key parameters affecting the reliability of STT-MRAM

MTJ parameters	Transistor parameters
The magnetic anisotropy (H_K)	Threshold voltage of the access transistor (V_T)
Saturation magnetization (M_S)	
Tunnel Magneto-resistance Ratio (TMR)	Length and width variations of the access transistor
Oxide thickness of MgO layer (t_{ox})	
Planar dimensions of the MTJ	

2.1.1. Read disturb

MRAM V_{dd} scaling is the most efficient method to reduce power consumption [23]. Both writing and reading V_{dd} can be reduced below 1V. Near threshold (near- V_T) configuration can be used for energy efficient sensing.

Writing operation in STT-MRAM is executed with the bipolar switching current. Notice that read and write operations share the same current flow path. Therefore, path overlap becomes an important concern. Along with bit-cell dimension shrinking and switching energy reduction, MRAM write current is continuously decreasing to get close to current range during read. Therefore, the sensing current has probability to switch the resistance state. This issue becomes an obvious trend with technology scaling of MTJ because of the reduced thermal stability factor and critical write current [24–25].

2.1.2. Incorrect read fault

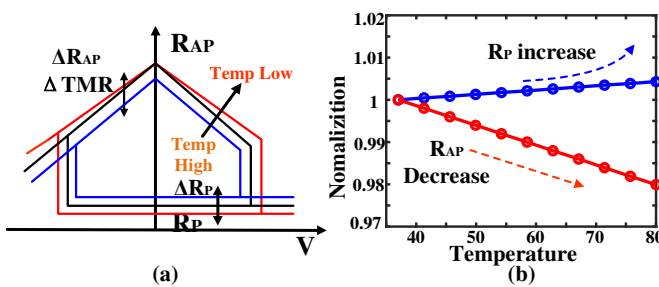


Fig. 1. (a) MTJ resistance versus bias voltage under different temperature, (b) temperature dependence of resistance of parallel and anti-parallel state, normalization at room temperature

As illustrated in Fig. 1, temperature fluctuations show significant impact on resistance of MTJ, whereas R_P and R_{AP} have the opposite trend of temperature dependence [24]. When the temperature increases, R_P gradually increases and R_{AP} gradually decreases, which leads to a reduced TMR and limited read margin. The antiparallel state is sensitive to the bias voltage of MTJ as shown in Fig. 1(a). That is, the TMR decreases with the increase of the bias on MTJ until its state switched, which inevitably leads to loss of sensing margin.

Several previous works announced that embedded MRAM

places MTJ in the lower metal layers for better routing ability at chip level [25]. Compared with high-level metals, the low-level solution shows serious parasitic effects. Besides, the lower layer should be optimized for a tight routing pitch and compatibility with logic platform due to its thin-layer characteristic. Parasitic resistance and capacitance of different bit-line (BL), source-line (SL) and their variations degrade the read margin.

2.1.3. Retention failures

MRAM is with intrinsic thermal instability, which results to bit-flip of cell resistance state, denoted as retention failure [22]. If the data stored in MRAM bit-cell suffers data corruption before read operation, it is impossible to read the correct data during a successive read process. This issue is limited by the technological level of MRAM, and can be improved for the exploration of thermal stability factor at MTJ device level.

2.2 Conventional VSA

Fig. 2(a) shows the working waveforms of conventional latch-type VSA in STT-MRAM [15], whose circuit is shown in Fig. 3(c). A read cycle starts with a precharge phase, BL and reference line (BLB) firstly precharge to read voltage. In the next phase, the word-line (WL) is on and BL begins to discharge, the resistance state of MTJ determines the discharge current. Finally, the latch-type VSA compares the V_{BL} with reference voltage (V_{BLB}) and outputs a digital result.

SAs have input offset caused by transistors mismatch [28]. The mismatch comes from transistors parameter variations (seen Table II). As V_{BL} and V_{BLB} both drop from read voltage to 0 quickly, the sensing margin window is short, as shown in Fig. 2(a). Theoretically, the maximum read yield acquired when sensing at the highest point of V_{in} . V_{in} is denoted as $|V_{BL} - V_{BLB}|$. MTJ process variations cause the maximum V_{in} occurs at different times for different cells as shown in Fig. 2(b) and 2(c). Replica bit-line technique is a proper timing scheme for suppressing timing variation and tracking MRAM process fluctuations [29]. Additionally, V_{BL} and V_{BLB} drop to a low level at sensing time, which produces a weak driving ability for NMOS sampling transistors.

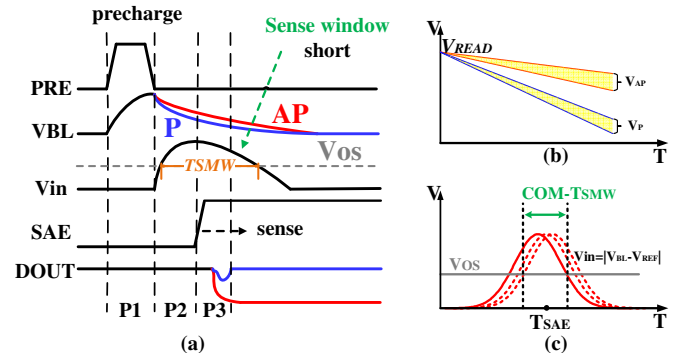


Fig. 2. (a) Waveforms of conventional VSA for STT-MRAM, (b) variations in V_{BL} and V_{BLB} swing during read operations, (c) Sensing margin window is limited by BL voltage variations

Therefore, a larger V_{in} is required to provide tolerance against above challenges. In this work, CSME scheme by charging and discharging bit-line along time has been proposed to improve read reliability at limited TMR and low supply

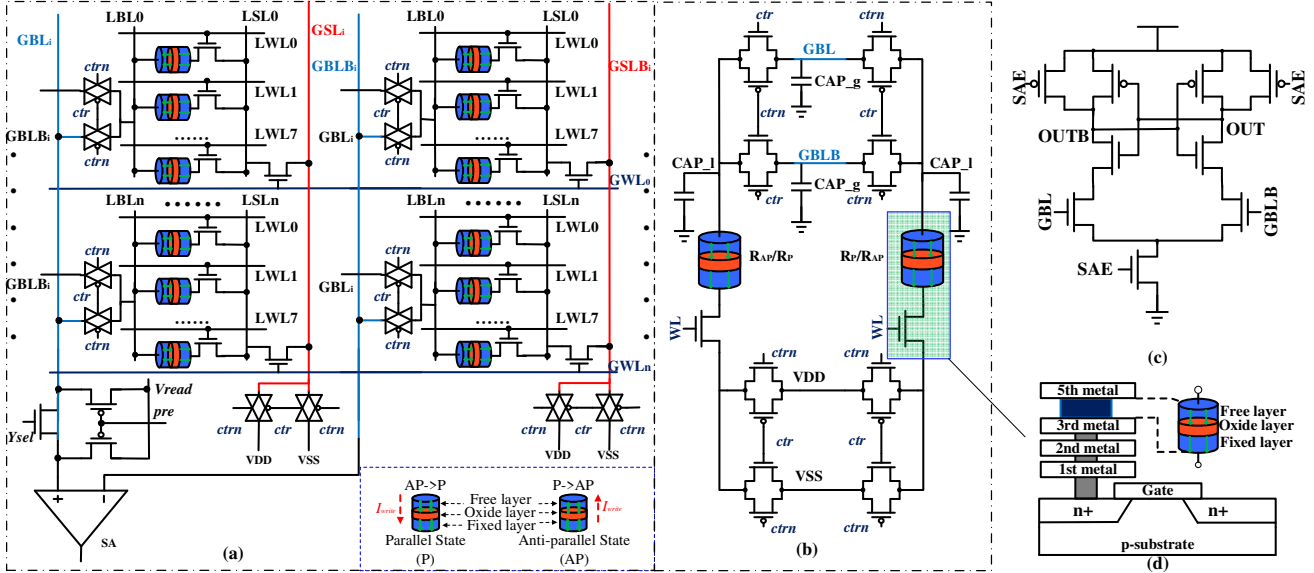


Fig. 3. (a) MRAM array (256 × 256) with the proposed CSME structure, (b) The schematic of CSME voltage difference optimization circuit, (c) The schematic of latch-type VSA, (d) The cross section view of 1T-1M bit-cell and MTJ device.

voltage.

3. Proposed read reliability enhancement scheme

3.1. CSME circuit implementation

The proposed cycle-sensing margin enhancement circuit with hierarchical bit-line technique is shown in Fig. 3(a). A hierarchical bit-line technique is necessary to ameliorate read disturbance [5] and reduce the height of memory bank [30]. 8 local columns are connected to global bit-line (GBL/GBLB) to reduce parasitic resistance of read paths for read margin enhancement. This scheme can also reduce write power consumption because the local bit-line (LBL) capacitance is reduced, the charging time is short, and thus the cell current can be suppressed. Fig. 3 (b) shows the CSME input voltage difference optimization conception diagram. Two transmission gates are used to isolate global and local bit-lines. In read operation, LBL can be alternately connected to GBL and GBLB. Another two transmission gates are used to control the charge and discharge operation of capacitance in global bit-lines. Fig. 3 (d) shows the cross section view of a 1T-1M (half of 2T-2M) MRAM bit-cell. Fig. 4 shows the detailed CSME timing sequence. *ctr* signal (*ctrn* is reversed *ctr*) is the switch of transmission gates. It is enabled only when current sub-array is selected. In the first phase (pre-charge), the capacitances of global bit-lines are pre-charged to the level of read voltage.

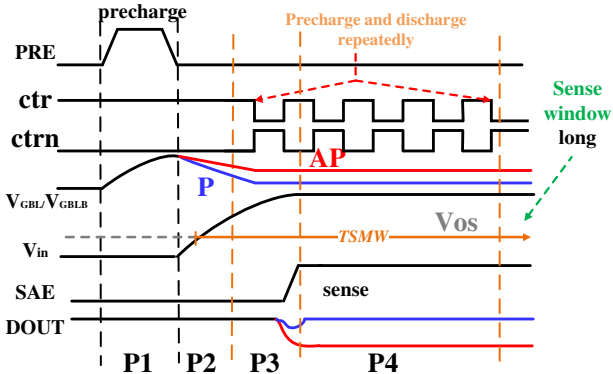


Fig. 4. The working waveforms of proposed CSME.

In the second phase (BL develop), the capacitance of GBL and GBLB begin to discharge and form an input voltage difference. The discharge current is depended on the resistance of accessed cell. When the resistance state of the accessed cell is R_{AP} , the cell read current is smaller than reference cell. Thus, the discharge speed of GBLB capacitance is faster than GBL, causing GBL voltage (V_{GBL}) larger than reference voltage (V_{GBLB}). Latency of this phase is similar with conventional VSA in order to acquire maximum value of $|V_{GBL} - V_{GBLB}|$.

In the third phase (sensing margin enhancement), the *ctr* signal changes to cycle pulse, and the charge/discharge operation of bit-cell alternately appears to further improve sensing margin. When *ctr*=1 (*ctrn*=0), the GBL capacitance discharges through the cell path and GBLB capacitance discharges through the reference path. Assume that the data stored in accessed cell is '1', so that the cell resistance is larger than reference resistance. The discharge current of data path is smaller than reference current, consequently causing the V_{GBL} larger than V_{GBLB} . When *ctr*=0 (*ctrn*=1), GBLB capacitance is connected to accessed cell and GBL capacitance attaches to reference cell. The charge current of data path is smaller than reference path. Therefore, the charging speed of the GBL capacitance is faster than the charging speed of the GBLB capacitance, and also causing V_{GBL} larger than V_{GBLB} .

It is obvious that both charge and discharge processes enlarge V_{in} . After several cycles, the global capacitances charge and discharge capacity reach equilibrium. V_{GBL}/V_{GBLB} tends to be stable and the input voltage difference remains unchanged. In the final phase, the SAE enable signal (SAE) is activated. VSA senses the voltage difference and generates a digital output.

The main difference between the proposed CSME and conventional VSA is the application of cycle pulse. The alternating occurrence of the charging and discharging process stabilizes and improves the input sensing margin.

3.2. p-VSA circuit implementation

In addition to the short duration of the sensing margin window, STT-MRAM suffers insufficient driving ability of the bit-line voltage to the NMOS sampling transistor (MN5/MN6

in Fig. 5), which is caused by low read voltage and the fast discharge speed. In order to overcome this issue, p-VSA with dual transistors enhanced sensing is proposed as shown in Fig. 5.

The p-VSA circuit is composed of two parts, the voltage difference conversion circuit and dual-transistors enhanced sensing circuit. A voltage difference conversion circuit is added on the basis of conventional VSA to auxiliary sense at low V_{BL} . This circuit can convert lower bit-line voltage to higher input voltage. When the input bit-line voltage is high enough to drive NMOS transistors, MN5 and MN6 complete sensing operation. When the V_{GBL}/V_{GBLB} is low, which cannot activate MN5 and MN6. But low input read voltage activates transistor MP1 and MP2, then the left circuit transforms the low input read voltage to high voltage, which increases the driving ability of NMOS transistor. SAE is the SA enable signal and SAEN is reverse SAE. Firstly, SAE is set to low, SAEN is high, D/DN will be discharged to GND and OUT/OUTB is precharged to V_{dd} . When V_{GBL} is higher than V_{GBLB} , the charging current flows through MP2 is larger than MP1. Thus, the voltage of DN becomes larger than D. Dual-NMOS sensing scheme works well despite the existence of bit-line voltage discrepancy of different cells during read operation. Dual-transistors sensing increases sense sensitivity and speeds up sensing.

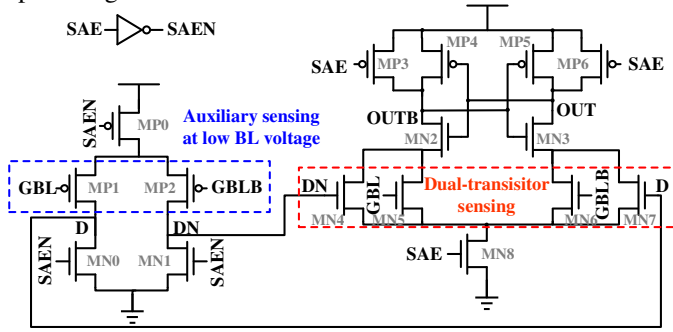


Fig. 5. The proposed p-VSA circuit with pMOS transistor auxiliary sensing at low BL voltage

4. Simulation Results

Table III. Physical parameters of STT-MTJ compact model used in this work [31].

Parameters	Description	Default Value
α	Gilbert Damping Coefficient	0.027
g	GyroMagnetic Constant	1.76e7
M_s	Saturation Field	15800
t_{ox}	Oxide thickness	0.85nm
t_{sl}	MTJ free layer thickness	1.3nm
RA	Resistance area product	5
TMR	Tunnel magnetoresistance ratio	10%-100%
R_p/R_{AP}	Parallel and anti-parallel resistance	5 k Ω /10 k Ω (Initial)
Area	MTJ layout surface	40nm \times 40nm
V_{BL}	Bit-line voltage (traditional sensing/this work)	150 mV/300 mV

The proposed CSME scheme was evaluated with an MTJ Verilog-A compact model and a commercial 28-nm CMOS process. Minimum transistor dimension ($W/L = 80\text{nm}/30\text{nm}$) is used to realize p-VSA circuit (see Fig. 5). A 256×256 MRAM cell array is simulated for sensing operation. Table III shows

the parameters of the used MTJ compact model.

Fig. 6(a) illustrates the input bit-line voltage and voltage difference during transient read operation of conventional VSA and this work. As conventional and our proposed scheme perform identical discharge, initially their voltage differences show same trend. As shown in Fig. 6(a), the sensing margin window lasts about 2.5ns in conventional scheme. Whereas in the proposed CSME scheme, the input voltage difference is continuously enlarged until it stabilizes at a relatively high value, e.g., 95mV when $V_{read} = 0.6\text{V}$ and $TMR=50\%$. 1,000 runs Monte Carlo simulation are performed considering TMR fluctuations. Results show that CSME achieves $\sim 2.4\times$ larger margin than previous work (see Fig. 6(b)).

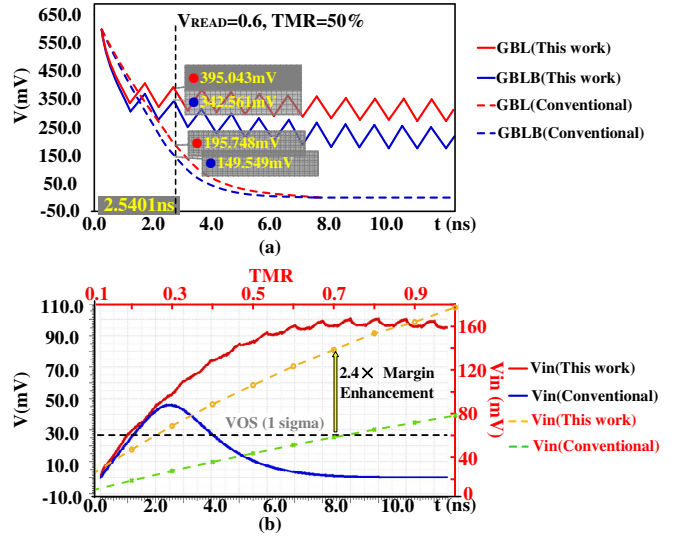


Fig. 6. Simulation results of (a) bit-line voltage and (b) V_{in} of conventional VSA scheme and this work

As the capacitance in GBL/GBLB is supplementary charged, V_{BL} in CSME scheme is about 200mV higher than previous VSAs. Thus, the ability of NMOS sensing transistor (MN5 & MN6) is enhanced.

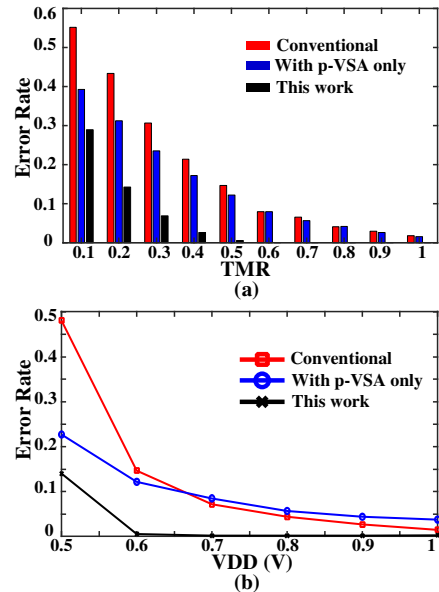


Fig. 7. 1000 times Monte Carlo Simulation results for read error rate estimation, with conventional VSA, p-VSA only and this work at (a) TMR fluctuation, (b) wide range supply voltage.

Our proposed scheme shows a significant read reliability

improvement. Fig. 7 (a) shows the simulation results of read error rate at TMR from 10% to 100%, the supply voltage and read voltage is set to 0.6 V. Comparing to conventional VSA, this work gets max 29.1% read error rate reduction. The read with p-VSA only also obtains max 15.9% read error rate reduction. The read yield improvement of CSME benefits from the high sensing margin and extended sensing margin window. These advantages make it robust for the intrinsic offset voltage of SA latch. Moreover, the increased sense sensitivity of dual transistors also contributes to the yield improvement.

Fig. 7 (b) shows the simulation results with wide range V_{dd} , this work obtains effective read yield improvement especially when V_{dd} is less than 0.7 V. The CSME scheme strengthens read reliability at wide operation range. The p-VSA only method is well-behaved at low voltage.

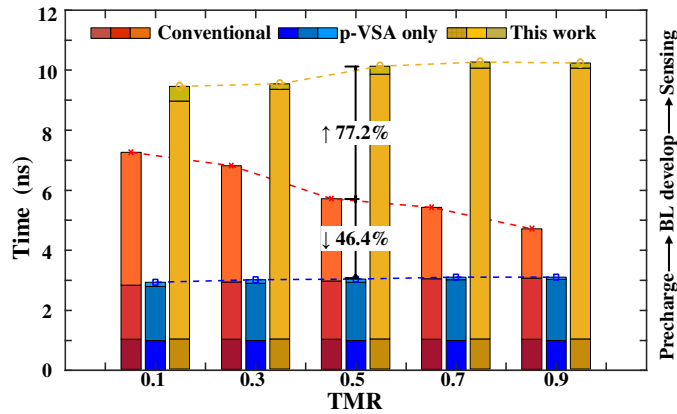


Fig. 8. Simulation results of latency for conventional VSA, p-VSA and this work at different TMR

Table IV – Performance comparison of the VSAs in 28nm CMOS with the same transistor size ($V_{dd}=0.6V$, TMR=50%)

	Conventional VSA	p-VSA only	This work	CRE-VSA[15]
Power (μW)	9.51	17.58	20.77	9.03
Latency (ns)	5.68	3.04	10.06	3.71
Normalized latency	1	0.54	1.77	0.65
Energy(fJ)	54	53.53	208.94	33.5
Normalized energy	1	0.99	3.85	0.62
Yield	0.879	0.99	0.995	0.958
Normalized yield	1	1.126	1.132	1.09

The improved yield of the proposed scheme comes at the expense of power consumption and latency. Fig. 8 demonstrates the simulation results of latency for conventional VSA, working with p-VSA only and this work at different TMR. The three methods have similar precharge time. Working with CSME has a longer BL develop time because it needs more time to stabilize V_{in} , which is 4 times longer than conventional VSA and p-VSA only. However, CSME has a short latch time, which benefits from the increased read margin, extended sensing margin window, high input bit-line voltage and the dual-transistors enhancement sensing. Overall, working with p-VSA only has the fastest access speed and CSME has the longest latency.

Table IV shows the performance comparison of the VSAs during the transient simulations. CRE-VSA is added for comparison. Simulation results indicate that CRE-VSA can only work well when the variations of CRE circuit is small enough. CRE-VSA achieves a fast access time and a reduced read power. The proposed CSME has the best read yield improvement among them.

5. Conclusion

A novel CSME scheme with p-VSA implementation was proposed to improve the read reliability of MRAM at low voltage and limited TMR scenario. The proposed scheme can demonstrate high-tolerance to MTJ/CMOS variations. Comparing to conventional VSA, an extended sensing margin window and higher SA input voltage were realized. The proposed scheme was evaluated with 28-nm CMOS and 40-nm MTJ compact model. Simulation results indicated a minimum 2.4 \times margin improvement and 14.1% read error rate reduction, which successfully benefits low TMR rate (50%) and low V_{dd} (0.6V) MRAM sensing scenario.

Acknowledgment

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