Building blocks of silicon photonics

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I. Introduction

Silicon is one of those materials that drastically changed the scientific, technological and societal world from the invention of the transistor by Bell Labs in 1947 [1]. The amazing shrinkage in feature size and the increase in transistor numbers [2] led the development of the electronics industry towards cheaper, smaller and faster devices. This integrated circuits (IC) evolution has primarily been driven by the so-called Moore's law, announced by Gordon Moore in 1965, predicting an exponential increase of the number of transistors per chip each 18 months [3].

Silicon (Si) is unbeatably the preferred material for the semiconductor industry because it has very interesting characteristics that may be advantageously exploited. In particular, (i) it is the second most abundant element on earth after oxygen, making it a very cheap material; (ii) its energy bandgap of 1.1 eV allows for efficient devices at room temperature; (iii) it presents higher processing temperature than other common semiconductors; and (iv) it is also ease of growing silicon dioxide and related materials on Si, allowing for fabrication techniques such as parallel and planar circuit processing [4]. Year after year, highly efficient silicon-based transistors and ICs have been developed. However, recently used metal-based electrical interconnects (EIs) are reaching their performance limits and are facing difficulties to keep up with the surge in the data rate demand over the last decade. The communications bottleneck is identified as one of the grand challenges in the progress of silicon computation and can be stated as: while individual logic elements have become significantly faster, computational speed is limited by the communication between different parts of a processor [5]. The main limitations of EI's are, among others, the constrained interconnect shrinkage, high-energy consumption, and signal delay, as well as limited bandwidth and data rate [5–7]. Particularly, power consumption in data processing is now so large that it is starting to be environmentally significant. To overcome this limitation, optical interconnects (OIs), where an optical signal is used instead of an electrical signal, have been considered, for many years, to provide a solution to the communication bottleneck and to energy consumption by replacing electrical wires with faster and low power optical devices in integrated circuits [8]. This visionary objective in the 1990's has matured, and year by year, silicon has become the revolutionary platform for photonics, especially through the emergence of versatile silicon-on-insulator (SOI) substrates. Indeed, additionally to extraordinary electrical properties, silicon also offers a range of excellent optical properties, including its large wavelength transparency window from 1.1 μm up to 7 μm. Furthermore, the large refractive index contrast between silicon, Si ($n_{Si} \approx 3.47$) and silicon dioxide, SiO_2 ($n_{SiO2} \approx 1.45$) enables development of compact devices that are suitable for large-scale and high-density integration on a chip. The strong evolution of silicon photonics has opened new routes for many applications, especially in all-optical communication systems. Indeed, the rapid increase of the digital data volume circulated around the globe, mainly within bandwidth-hungry datacenters, modified the horizon of silicon photonics. This evolution is driven by the change of Internet communications used via mobile devices and the development of the "Internet of Things". Therefore, some new challenges have to be considered in terms of speed, power consumption, flexibility, and reliability for the implementation of optical transceivers in the future datacenters.

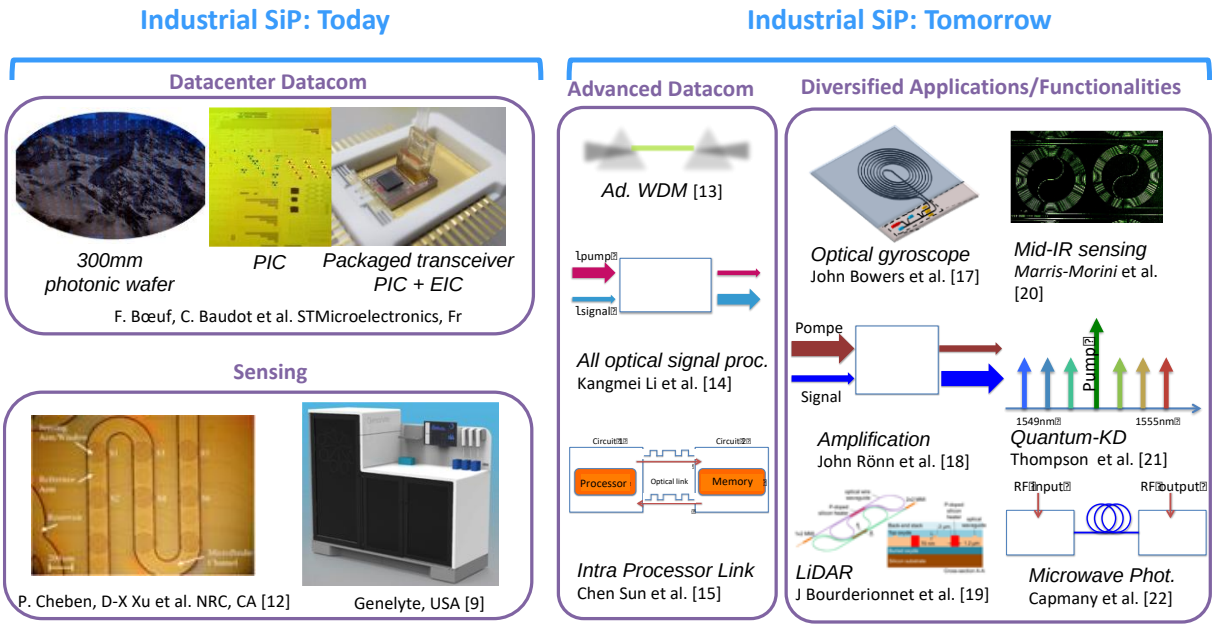

Fig. 1: Evolution scheme of the industrial silicon photonics. [9]

For a few years, some industrial solutions combining both photonics and electronics have been available in order to address datacenter requirements [10]. In parallel, due to the low-cost and high-volume capability of silicon photonics, biological and chemical sensors have also become available as commercial products [11,12]. As reported in Fig. 1, nowadays, transceivers for datacenter and packaged resonators for bio-and chemical sensing are the first silicon photonics products available in the market. This fast evolution from fundamental physical concepts in the 1980's towards products has generated a strong interest in others applications. Indeed, additionally to the development of the next generation of devices and circuits for advanced datacom, including wavelength division multiplexing systems [13], all optical signal processing [14], and intra-processor links [15,16], new applications, circuits, and devices are now considered: optical gyroscopes [17], on-chip amplifiers [18], LIDAR [19], optical spectroscopy [20], Quantum photonics [21], microwave and opto-RF photonics circuits [22], to name a few.
Efficient on-chip devices to emit, modulate, and detect light have to be developed in the silicon photonics platform (Fig. 2). Thereby, numerous devices have then been demonstrated to realize a complete optical link, including efficient input/output (I/O) light couplers [23-46], low-loss passive waveguides, and optical resonators [47], high-speed modulators [48-68], as well as high-speed and high-responsivity photodetectors [69-84]. Due to the huge impact of silicon photonics in many application domains, most of these components are recently fabricated in accessible industrial and academic foundries via multi-project wafer (MPW) shuttle services (CEA/Leti, IMEC, AIM Photonics, IME…) that are widely available to the silicon photonics community. Among all devices, the optical source on silicon remains a daily challenge, because silicon is an indirect band semiconductor material with poor efficiency in light emission. From band and strain engineering, some promising results have been obtained with germanium-on-silicon lasers [85-86]. However, today, the most common approach is based on hybrid co-integration of III-V materials with silicon [87-95], well-known for their efficient laser properties in a wide wavelength range.
In this chapter, an overview of the main silicon-based building blocks, including passive devices, optical modulators, photodetectors, and light sources is presented. As pure silicon devices to generate, modulate, and detect light are not realistic yet, hybrid integration of active materials on

the silicon photonics platform is also discussed in the last section with the presentation of few examples that highlight benefits of hybrid silicon photonics.

II. Silicon-based building blocks

An integrated optical link, i.e. optical transceiver, is generally formed at least by three main optoelectronic elements, as schematically illustrated in Fig. 2: the emitters, responsible for the electrical-optical signal conversion; the analogic or digital optical modulators to code the information, and the receivers, where the optical signal is converted back to an electrical domain. To complete the link, structures, which guide the light into the different elements of the photonic IC and ensure the in/out light coupling from/to optical fiber are included. Therefore, each building block has to be implemented so that its overall speed, size, the global loss (insertion and propagation losses), and energy consumption satisfies the required limits, driven by the target application as well as its compatibility with silicon technology in microelectronics pilot lines. For optical interconnects, the energy consumption of transceivers should be 50 - 200 fJ/bit and should meet the global demands in the near future, i.e. this value should be lowered to 10fJ/bit, according to an analysis presented by Miller [96].

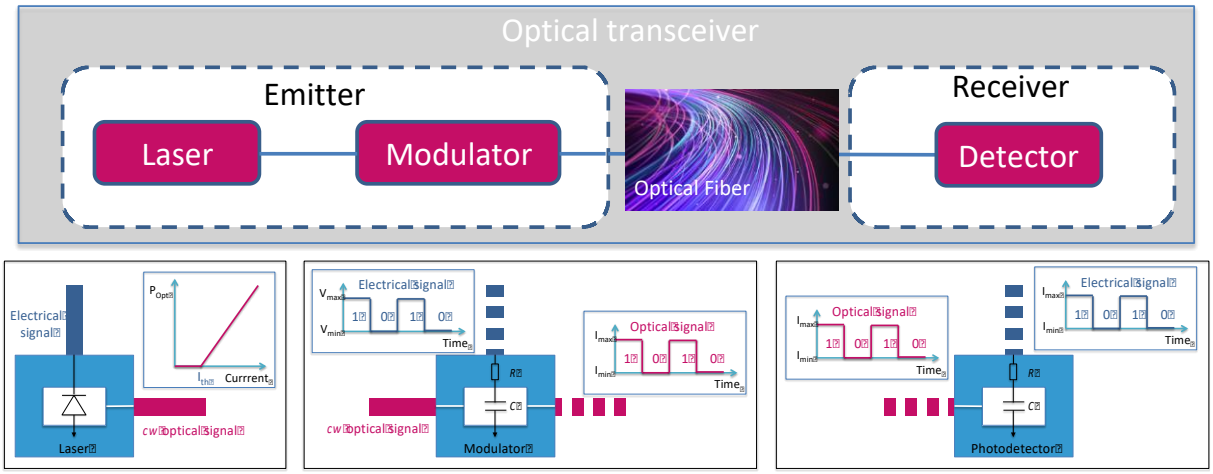

Fig. 2: Optical transceiver: main building blocks including laser, modulator and detector.

II.1 Passive devices

The objective of this section is not to report on an exhaustive overview of all possibilities afforded by silicon photonics for the development of passive devices. The aim is to present the two fundamental blocks necessary to build up a photonic circuit: waveguides as basic component, allowing the implementation of more complex devices such as resonators [47], wavelength multiplexers [97], and modulators [68], to list a few, and the surface grating couplers as a direct link towards the external world accessed through the optical fibers.

Thanks to the high index contrast between silicon and silicon dioxide cladding in the SOI platform, strong modal confinement is readily achievable. This leads to a great flexibility in light guiding on a chip, i.e. compact waveguides, splitters and resonators of sharp bends. Several types of waveguide geometries have been implemented in silicon, each targeting a different optical functionality, while providing specific advantages and drawbacks. Figure 3 schematically shows the four most commonly used waveguide geometries. Main characteristics of these waveguides are briefly summarized below:

- Strip waveguide: This geometry relies on a full-etch step fabrication process, resulting in a high index contrast confinement in both vertical and horizontal directions. Such waveguide configuration allows tight bending radii, of around 5 μm [47], which make them very interesting for the implementation of ultra-compact devices. On the other hand, strip waveguides are very sensitive to sidewall roughness, resulting in comparatively high propagation loss, with typical values of dB/cm [98].

- Rib waveguide: A shallow- or deep-etch waveguide arrangement is used to reduce lateral index contrast, yielding a reduction of the propagation loss (down to sub-dB/cm [99]) and relaxing conditions for single-mode operation [100]. Rib waveguides are commonly used for opto-electronic devices, especially modulators and photodetectors, as the lateral Si slab allows putting doping regions apart from the guiding zone.
- Slot waveguide: Unlike conventional strip and rib geometries, slot waveguides exploit boundary conditions for light polarized in the chip plane, to funnel the light within the low-index region between the two silicon rails [101]. This particular guiding mechanism, with a remarkably strong confined evanescent field, make slot waveguides a very promising approach for the hybrid integration of active materials [102] or the implementation of evanescent-wave sensors [103]. Still, higher propagation loss may arise due to the strong interaction of light with sidewall roughness, requiring tight control of fabrication processes [103].
- Sub-wavelength waveguides: By periodically etching silicon with a pitch shorter than half of the wavelength, it is possible to suppress diffraction effects, implementing a metamaterial waveguide with engineered optical properties [104]. Sub-wavelength waveguides exhibit a propagation loss comparable to that of conventional strip counterparts [104], yet with flexible confinement and dispersion engineering that allowed the demonstration of low-loss crossings [105] and high-efficiency fiber-chip couplers [106]. However, trade-offs between the mode confinement engineering and the bending radius are typically required [107].

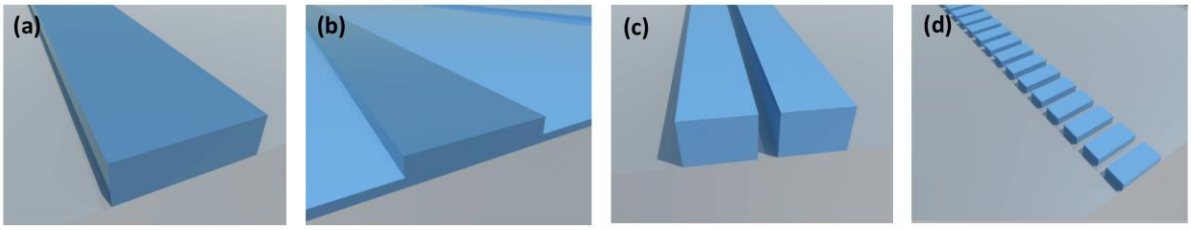

Fig. 3: Schematic representation of most commonly used waveguide geometries in Si photonics: (a) strip, (b) rib, (c) slot, (d) sub-wavelength.

From these waveguide geometries, numerous possibilities are offered by adjusting the height and width of the waveguides. Furthermore, in order to reduce the two photon absorption (TPA) in silicon at high optical power and the phase error due to the strong light coupling into Si waveguides, Silicon Nitride integration can also be considered as an alternative.

As silicon photonics applications require multi-interchip connections via optical fibers, efficient coupling interfaces are recognized as essential functional components in planar lightwave circuits. The light coupling is a non-trivial task, especially for high-index contrast platforms such as silicon-on-insulator, due to the large mode size disparity between modes of sub-micron waveguide cores and optical fibers, since dimensions of such waveguides are around two-orders of magnitude smaller than that of standard optical fibers (SMF-28).

The fiber-chip surface grating couplers (SGCs) have appeared as an elementary, yet recently popular approach to couple the light to or from integrated waveguide circuits, as demonstrated by seminal works of Dakss et al. [108] and Tamir et al. [109]. Over the years, the SGCs have shown marked maturity to afford efficient, robust, and scalable coupling functionality for off-chip optical fiber attachments [23-46]. The SGCs do not require additional post-manufacturing steps for a chip facet preparation such as dicing, polishing, and cleaving, while enabling flexible positioning on the chip with cost-effective wafer-scale accessories, as well as the compatibility with integration and packaging scenarios [25-29]. The SGCs are formed by a periodic diffraction grating in slab waveguide to allow a resonant light coupling between the planar circuit and a typically tilted optical fiber, positioned above the device, as schematically shown in Fig. 4(a).

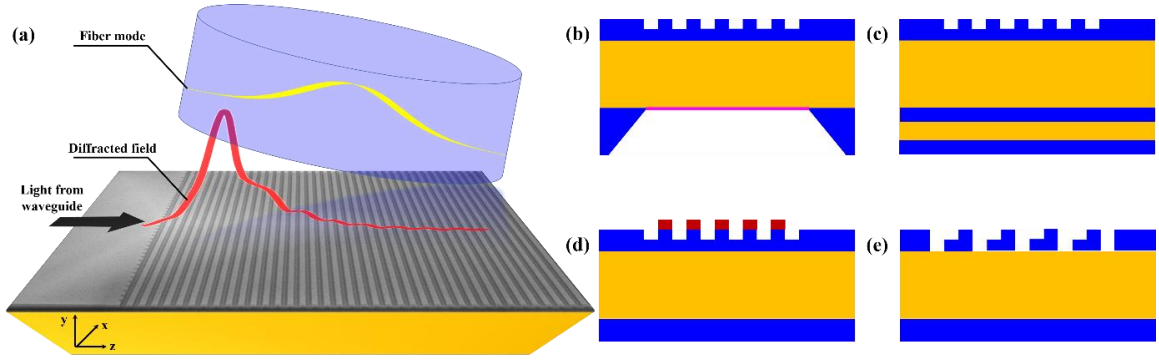

Fig. 4: (a) A fiber-chip surface grating coupler. The diffraction grating resonantly couples the light injected from the waveguide with an exponentially-decaying profile towards a Gaussian-like optical fiber mode. Schematic illustrations of the state-of-the-art approaches to achieve a high-efficiency coupling between optical fibers and integrated circuits. (b) SGC with a metal mirror implemented via backside processing [31, 33, 34]. (c) SGC with a Bragg mirror implemented via wafer-to-wafer bonding or by using a customized SOI wafers [25-27,35,36]. (d) SGC with an overlayer realized on top of device [37-39]. (e) Blazed SGC with an L-shaped geometry [33-36].

To date, an extensive set of SGC design strategies have been reported, with a steady progress in improving the fiber-chip coupling efficiency. Several decisive aspects *en bloc* contribute to the overall coupling performance, including the back-reflections at the waveguide-to-grating junction, the mode mismatch between the Gaussian-like optical fiber mode and the exponential profile of the grating beam, as well as the parasitic optical power that radiates towards the bottom substrate. The first two factors are typically addressed simultaneously by using the SGC apodization [24-26, 29-31], i.e. diffraction grating of a variable coupling strength that matches the near-field Gaussian mode profile. This encompasses approaches such as a duty cycle variation [24-26], etch depth optimization [29], or a sub-wavelength grating (SWG) refractive index engineering [30,31]. However, over the years, the SGC directionality, typically defined as the ratio of the power coupled towards the optical fiber and the total out-coupled optical power [31], has been identified as a main limiting factor for high-efficiency coupling [32].

The state-of-the-art solutions exclusively exploit the effect of thin-film interference by forming partial or full reflectors underneath the coupling device. This way, the light radiated downwards (into the substrate) is effectively re-utilized in order to assure in-phase diffraction with the preferential first-order radiation beam that is constructively coupled to the optical fiber mode. This may be realized through the etching depth optimization [24,26,29], BOX thinning [25,27,34], or radiation angle adjustment [31], typically combined with additional fabrication steps of backside wafer metallization [31,33,34] or flip-chip wafer-to-wafer bonding [25-27,35,36]. Experimentally, fiber-chip coupling efficiencies down to -0.5 dB have been demonstrated hitherto. Schematics of these concepts are illustrated in Figs. 4(b) and 4(c), respectively.

Alternatively, maximizing the intrinsic SGC directionality, i.e. breaking the vertical device symmetry, has also emerged in recent years as a profound design scenario to vastly improve the overall coupling efficiency [37-46]. In this concept, the optical power constructively diffracted to the upper cladding is maximized, while at the same time the parasitic power leaked into the substrate is conversely minimized. Efficient SGC designs have been theoretically elaborated and experimentally validated, primarily by using subsidiary low and high refractive index overlayers [37-39] or by exploiting the blazing effect in interleaved or in *L*-shaped device arrangements [40-46]. Those approaches are shown in Figs. 4(d) and 4(e), respectively, affording a tested coupling performance down to -1 dB up to date. Most recently, the later blazing concept has received a considerable amount of attention, particularly due to its inherent versatility [40-42], compatibility with processes and tools established in nanophotonics foundries [43], and waveguide platform portability [45,46], delivering high-efficiency and robust coupling reliance.

Today, the major challenge in light coupling in silicon photonics circuits resides in the limited spectral bandwidth of SGCs. Some solutions based on edge coupling are studied: inverted taper [110,111], subwavelength taper [112], and silicon nitride edge coupler [113]. These solutions

provide broadband light coupling and polarization insensitivity, however they are not suitable for large-scale wafer testing. Light coupling from/to optical fiber is still considered as an open and challenging task, which has to be solved in order to fully develop reliable multi-spectral photonic integrated circuits.

II.2 Optical modulation

Optical modulation is carried out by modifying the optical properties of the material (Si, Ge, III-V, Polymer, etc.) to change the behaviors of the light propagating through it. This modulation is mainly performed by an external electrical signal, which changes the real and/or imaginary parts of the refractive index of the particular material. The real part (n) is associated to the phase velocity and the imaginary part (α) is associated to the absorption. This allows classifying optical modulators in two main groups: (i) Electro-refraction modulators and (ii) Electro-absorption modulators, respectively. The most common physical effects exploited for optical modulation in photonics are Thermo-Optic (TO) [114], Pockels [115-117], Franz-Keldysh (FK) [118-119], Quantum confined Stark Effect (QCSE) [120-127], and Free-Carrier Plasma Dispersion effects [48-68].
The evaluation of the optical modulator performance is carried out through a typically wide set of parameters, so-called Figures-of-Merit (FoM). The most commonly used are the following:

- The Insertion Loss (IL): It is the total loss of the modulator section including in/out coupling and propagation losses. For a phase modulator, the insertion loss for L_π length (IL_π) is given. L_π is the modulator length to achieve π phase shift.
- The Electro-Optical Bandwidth (BW): This characteristic corresponds to the maximum speed of the modulator (analog signal). For most modulators, this bandwidth could be theoretically analyzed through the equivalent RC circuit of the electrical structures. Speed characteristics are also studied using digital signals (data rate). Then, eye diagram measurements are required as well as Bit-Error-Rate (BER) analysis to define the quality of the data transmission.
- The extinction ratio (ER): It characterizes the ratio of optical intensities in on/off states. ER is often reported at a given data rate, which is often lower than the ER given in DC.
- The modulation efficiency ($V_\pi L_\pi$): Only reported for an electro-refraction modulator inducing a variation of the effective index (Δn_{eff}) at a given wavelength λ. $V_\pi L_\pi$ is the product of the voltage (V_π) and the length (L_π) of the phase shifter needed to achieve π phase shift.

$$V_\pi L_\pi = \frac{V_\pi \lambda}{2.\Delta n_{eff}(V_\pi)} \quad (1)$$

- The power consumption (J/bit): Power consumption depends of the capacitance (C) of the electrical structure, the voltage swing (V), and the photogenerated current (I_{ph}) at a given data rate (B). The latter is mainly considered for an electro-absorption modulator. Power consumptions is driven by two equations:

$$E_1 = \frac{1}{4} C V^2 \quad (2)$$

$$E_2 = \frac{1}{B} I_{ph} V \quad (3)$$

We can notice that a comparison of published results on optical modulators is not often straightforward due to the variety of afore-described optical and electrical characteristics. In the following, an overview of the main physical effects typically elaborated to change the optical intensity is reported.

Thermo-Optic effect

The Thermo-Optic effect is a slow effect, which is mainly used to tune the operating point of photonic devices or as an actuator for switches. Indeed, under a temperature change (ΔT), the refractive index variation (Δn) of the material also changes following this expression in silicon: $\Delta n/\Delta T = 1.86 \times 10^{-4}\ K^{-1}$, denoted as the thermo-optic material coefficient (in this case coefficient of silicon). In some cases, when the electric power applied to the device is high, the temperature may rise, leading to a shift of the component behavior. In most of applications, the thermo-optic effect has to be addressed, either to compensate the thermal drift or to tune the operating wavelength.

Pockels effects

The Pockels effect is the dominant effect used in optical modulators based on Lithium Niobate ($LiNbO_3$) and Indium Phosphide (InP). However, silicon is a centro-symmetric crystal. An immediate consequence is the non-existence of the second-order optical susceptibility ($\chi^{(2)}$) in the material, the fundamental material property behind the origin of the Pockels effect. Nevertheless, it has been proposed and evaluated that the strain can be used to break the symmetry of the silicon crystal, as schematically represented in Fig. 5. This process is capable of generating the normally inhibited second-order susceptibility ($\chi(2) \neq 0$) and enables nonlinear phenomena like the Pockels effect [115-118]. The motivation is to develop strained silicon photonic devices for optical modulation: with a prospect for high-speed, low-loss, compact, low-power consumption, large optical bandwidth, and silicon compatible modulators.

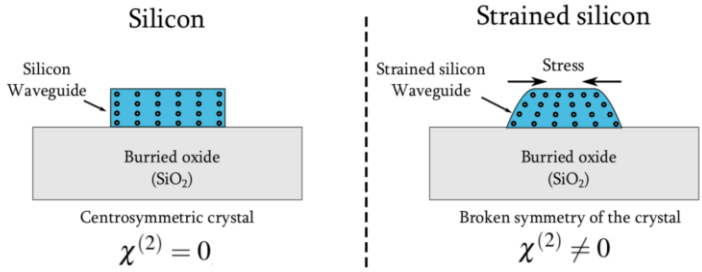

Fig. 5: The process of straining silicon to break the symmetry and induce χ(2) dependent phenomena.

A lot of efforts have been made in the recent years towards breaking the centro-symmetry of silicon and achieving the Pockels effect. Even though the results look promising, they are still far from the device point-of-view.

Electro-absorption effects

Electro-absorption (EA) modulators are a class of modulators that employ an electric field to induce a variation of the absorption coefficient (α) of the material, which directly changes the light intensity. Direct modulation of the optical intensity is obtained and the performance metrics depend on the absorption coefficient variation and the working spectral range. There are two main EA mechanisms in silicon photonics: the Franz-Keldysh effect and the (QCSE). Both of these effects have been demonstrated in Germanium and Germanium alloys [119-128], providing a platform for silicon-compatible materials for high speed, low power, and compact modulators.

In 2008, a MIT group demonstrated the first EA GeSi modulator based on the Franz-Keldysh effect (FKE), working around the C and L bands of telecommunication wavelengths [119,120]. From this demonstration, several groups developed Ge technology to achieve compact and low-power consumption modulators. A typical EA modulator based on FKE from bulk Ge has been reported to have around 8-10 dB extinction ratio at about 1600 nm wavelength using a reverse bias voltage between

0 and 4 V for a device with an active area of less than 45 μm^2, with a corresponding insertion loss of 5-10 dB and ~100 fJ/bit dynamic energy consumption. Adding a very small fraction of Si into Ge, 1550 nm operation has been reached [119-120].

The use of bulk Ge for light modulation based on FKE has shown two main limitations for datacom and low power consumption applications. First, the operating wavelength is limited to material band gap energy, i.e. 1550 nm. Secondly, swing bias voltages are still higher than 1 V, the maximum voltage delivered by CMOS circuits. These limitations can potentially be overcome by using the quantum-confined Stark effect (QCSE) in Ge multiple Quantum wells (MQWs). The benefits of quantum well structures result from its discrete energy levels thanks to the quantum confinement effect. Some recent demonstrations on high-speed optical modulation have been reported at wavelengths from 1300 nm to 1550 nm [121-128].

Free-Carrier Plasma Dispersion effect

The Free-Carrier Plasma Dispersion (FCPD) effect relates the changes in free carrier concentration in a semiconductor (electrons and holes) to a change in the complex refractive index. As the free carrier concentration increases, the imaginary part of the refractive index (absorption coefficient) increases, while the real part (phase) decreases. This effect was theoretically described by the Drude-Lorentz model [129-131]:

$$\Delta n = -\frac{e^2 \lambda^2}{8\pi^2 c^2 \varepsilon_0 n}\left(\frac{\Delta N_e}{m_e} + \frac{\Delta N_h}{m_h}\right) \quad (4)$$

$$\Delta \alpha = -\frac{e^3 \lambda^2}{4\pi^2 c^3 \varepsilon_0 n}\left(\frac{\Delta N_e}{m_e^2\, \mu_e} + \frac{\Delta N_h}{m_h^2\, \mu_h}\right) \quad (5)$$

where e is the charge of the electron, c is the speed of light, λ is the wavelength, n is the refractive index of the unperturbed material, ε_0 is the vacuum permittivity, ΔN_e and ΔN_h are the free carrier concentrations of electrons and holes, respectively, m_e and m_h are the electron and hole respective masses, μ_e and μ_h are the mobilities of electron and holes, respectively. From Eq. (3) and Eq. (4), it is possible to model the effect of free-carriers into the refractive index of any materials.

In silicon photonics, FCPD is still the main effect used to develop high-speed and efficient optical modulators. In the 1990's, visionary works from Soref and Bennet reported on experimental data on the variations of the refractive index as well as absorption of doped silicon wafers and defined a set of empirical equations for wavelengths around 1.3 μm and 1.55 μm [131]. As an example, for λ = 1.3 μm they take the form:

$$\Delta n = -6.2 \times 10^{-22}\, \Delta N_e - 6 \times 10^{-18}\, (\Delta N_h)^{0.8} \quad (6)$$

$$\Delta \alpha = 6 \times 10^{-18}\, \Delta N_e + 4 \times 10^{-18}\, \Delta N_h \quad (7)$$

As the electro-absorption generated by the FCPD effect is not strong enough for modulation, optical modulators based on this effect are mainly designed as electro-refraction modulators (i.e. phase shifters), minimizing absorption changes. Three main kinds of FCPD effect can be used to change carrier concentration variation into a waveguide: injection, accumulation, or depletion of carriers. The electronic structures to achieve such carrier variations are illustrated in Figure 6.

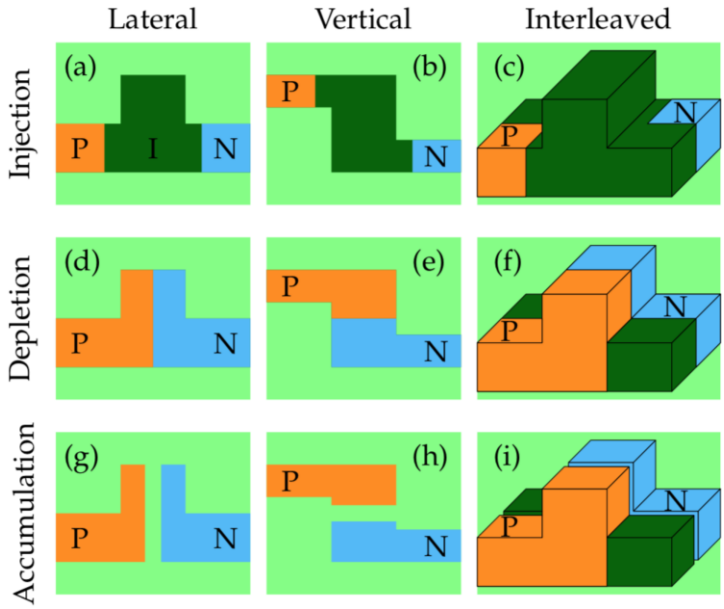

Fig. 6: Waveguide modulators based on the free carrier plasma dispersion effect: ***Carrier injection:*** *(a) lateral pin diode, (b) vertical pin diode, (c) interdigitated pin diode;* ***Carrier depletion:*** *(d) lateral pn diode, (e) vertical pn diode, (f) interdigitated pn diode;* ***Carrier accumulation:*** *(g) lateral capacitance, (h) vertical capacitance and (i) interdigitated capacitance.*

Carrier injection is based on PIN junctions, as reported in Fig. 6a, 6b, and 6c. Under a forward bias, a current flows through the junction, and the intrinsic zone (in green) is flooded with carriers (electrons and holes). A proper overlap between this zone and the optical mode introduces a change in the refractive index (i.e. phase change). This FCPD effect is the most efficient effect, but it is power hungry and limited in speed.

Carrier depletion is normally based on a PN junction (see Fig. 6d, 6e, and 6f). Under a reverse bias, a depletion (intrinsic) zone appears in the vicinity of the PN junction. The width of the depletion zone increases as a function of the reverse bias, removing carriers from both P and N doped regions. The widening of the depletion zone introduces a change in the refractive index and then a phase variation of the guided mode. As a unipolar effect (only one carrier), this effect is intrinsically high-speed. However, as the depletion zone is limited, the efficiency is lower than the carrier injection effect. In silicon photonics, carrier depletion is still the main effect used for optical modulation, because it combines high-speed, low insertion loss, and moderate power consumption with a simple technological process.

Carrier accumulation employs p-doped, oxide, n-doped (PON) capacitor structures (see Fig. 6g, 6h and, 6i). Under a bias voltage, electric charges accumulate apart the oxide interfaces, i.e. holes in the p-doped part and electrons in the n-doped part. This accumulation of carriers induces a change in the refractive index in the silicon close to the interface with the oxide. This effect combines a judicious mixture between carrier injection and depletion. The main drawback is still the complex processing and the limited bandwidth due to the large capacitance of the structure, however promising results have been already obtained [132-137].

Remarkable OOK (On-Off Keying) modulation characteristics have already been obtained with performance close to state-of-the-art lithium niobate modulators. Indeed, 40 Gbps, and even more, have been demonstrated with extinction ratios larger than 6 dB and insertion loss below 5 dB. The modulation efficiency $V_\pi L_\pi$ is 1-2 V.cm for carrier depletion effects, while it is below 1 V.cm for carrier accumulation modulators. From these characteristics, current trends are to first develop a reliable complex circuit that integrates lasers, Si modulators, and detectors, and secondly, to demonstrate

advanced multi-level modulation formats, including pulse amplitude modulation (M-PAM), phase shift keying (M-PSK), and quadrature amplitude modulation (M-QAM) based on FCPD.

Despite amazing characteristics, the requirements in terms of ultra-low power consumption are not reachable to date. Indeed, values of about one pJ/bit were obtained in optimized FCPD structures, which is quite far from the objective: a few fJ/bit. Then, some alternative solutions have to be developed and a promising trend may be the hybrid integration with other materials that are typically considered to be more efficient compared to the silicon-only approaches. This includes materials such as polymers, nano-materials like graphene, chalcogenide glasses, or carbon nanotubes functional oxides (BTO, BST, etc.), and of course III-V compounds. In section III, hybrid integration of III-V materials on a silicon photonics platform will be discussed and some demonstrations will be presented.

II.3 Optical receivers

Optical receivers are one of the main building blocks of the full Si photonics chain. Indeed, as it is positioned at the end of the optical link, it governs the whole power budget of the link, i.e. the delivered optical power of the lasers, the insertion loss of the modulators, and the loss of passive structures. A photodetector needs a minimum power to achieve the BER specifications at a given data rate.
In the silicon photonics platform, germanium (Ge) rapidly became the material of choice, because of its strong absorption coefficient in the near-infrared wavelength range (up to 1.6 µm) and its compatibility with CMOS processes, favoring monolithic integration. Despite the large lattice parameter mismatch between Ge and Si (4.2%), the epitaxial growth of high-quality and thick crystalline germanium layers on silicon has been successfully demonstrated with low dislocation concentration in Ge [138]. Today, the Ge photodetector is well identified as the most robust and mature device in the silicon photonics platform. Indeed, it offers cutting-edge performance directly comparable to its III-V counterparts.

Two strategies have been developed and reported for the integration of Ge photodetectors into silicon waveguides: (i) evanescent coupling and (ii) butt coupling (Fig. 7a and 7b, respectively) [69-84].

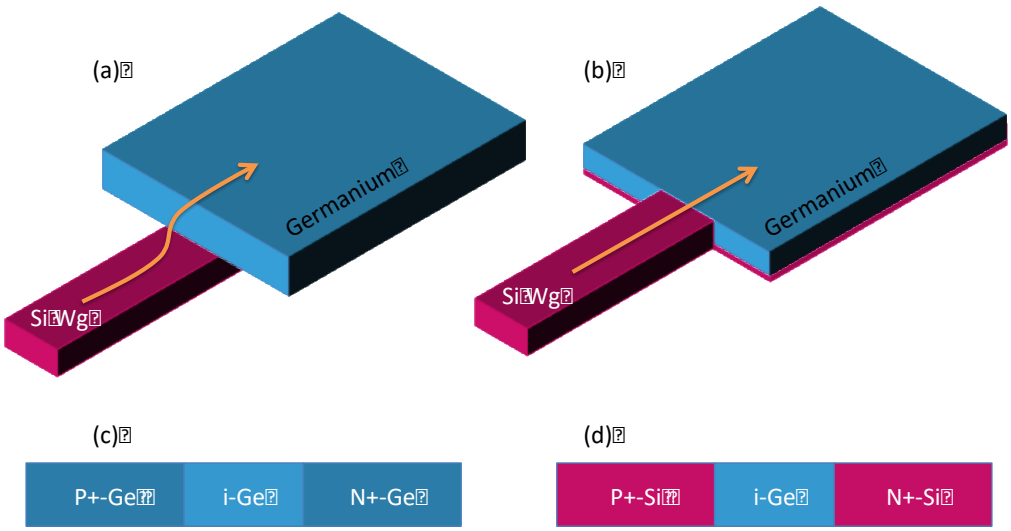

Fig. 7: Schematic view of (a) evanescent coupling and (b) butt coupling and the pin diode for photodetection: (c) pure Ge photodiode, (d) double Si/Ge/Si heterojunction photodiode.

Both Ge integration schemes have demonstrated similar photodetection performances in terms of speed and responsivity. However, even though there are no fundamental differences, there are some slight variations, which could be detrimental for a few applications. Indeed, the coupling efficiency is more robust for the butt-coupling configuration in terms of wavelength sensitivity and Ge thickness variation. Furthermore, such integration leads to an almost flat surface promoting hybrid integration. However, the detection linearity with input optical power in the evanescent coupling configuration is better than in the butt-coupling configuration as the light is continuously distributed along the germanium layer.

This avoids any kind of absorption screening due the strong Ge absorption. According to the target applications, these characteristics have to be taken into the account.

Two kinds of electrical configuration for the photodiodes have emerged, schematically shown in Fig. 7c and Fig. 7d: (i) a pure (homojunction) Ge photodiode with P+ and N+ Ge-doped contacts and (ii) a double Si/Ge/Si heterojunction photodiode where doped regions are formed in silicon [84]. Both approaches exhibit comparable detection characteristics. The advantages of a double Si/Ge/Si heterojunction photodiode are: (i) a reduction of the number of technological steps (e.g. a reduction of the fabrication cost and complexity), (ii) a decrease of the contact access resistance thanks to the use of a NiSi silicide, and (iii) an improvement of the optoelectronic device integration because identical silicide-based contacts are used for all optoelectronic Si devices including optical modulators and photodetectors. However, a challenging selective Ge epitaxial growth in a narrow Si trench has to be performed.

Numerous successful demonstrations have been obtained on Ge photodetectors integrated into Si waveguides. Most of these photodetectors reached very high performances in terms of speed (>40 GHz) and responsivity (>1 A/W) and dark current (below 100 nA). Even after a reduction of four orders of magnitude of the dark current from the first generation of Ge detectors, the dark current is still 1-2 orders of magnitude higher than the state–of-the-art III-V detectors. The key to solving this problem is the quality of the epitaxial growth of germanium on silicon in order to reduce the dislocation concentration and the traps at the interface between the Ge and Si.

As stated above, receivers in integrated circuits drive the minimum optical power needed to ensure error-free detection. Therefore, the more sensitivity of the detector, the lower required optical power from the source. The use of avalanche photodiodes (APD) have appeared as a promising way to push the responsivity beyond the limit imposed by external quantum efficiency. Avalanche operation in Germanium based photodiodes has been firstly demonstrated in Separate Absorption Charge Multiplication (SACM) [139] and Metal Semiconductor Metal (MSM) structures [140]. SACM avalanche photodiodes provide an optimized marriage between the strong germanium absorption and the low multiplication noise in silicon. However, a high bias is needed (>-10 V) to reach high multiplication gain, and the fabrication is complex due to the need to perfectly control the electric field into Ge and Si in order to reduce the electrical noise. Conversely, internal gain in MSM structures can be achieved at low bias (<-3 V); however, the dark current in MSM structures is well-known to be very high (typically of 50 µA for unity gain), thereby substantially degrading the sensitivity of the avalanche photo-receiver. Recently, a new approach has been developed based on a compact p-i-n Ge photodiode biased in avalanche mode with a thin multiplication Ge layer for dead space enhanced noise reduction [139,140]. This approach allows for simplified integration in silicon photonics technology. Moderate avalanche gain, about 10-20, and relatively low bias voltage of about 6 V have been demonstrated.

These preliminary results on Ge receivers are promising; however, they call for more research efforts in order to obtain efficient, low-voltage, low-noise and reliable avalanche photo-detectors directly integrated into Si waveguides.

II.4 Light Source

An integrated electrically pumped Si-based optical source has long been considered as a Holy Grail in silicon photonics as long as silicon is an indirect band gap semiconductor that exhibits light emission with poor efficiency. Numerous works have been performed on bulk Si, Si nano-crystals, and Rare-Earth Doped Silicon, to make this material a good candidate for on-chip lasing functionality. Although a lot of scientific breakthroughs have been accumulated over the years, no Si laser was demonstrated so far. However, from band engineering of highly doped Ge, promising demonstrations of germanium-on-silicon lasers have been achieved. Despite numerous efforts on the development of Ge lasers, the threshold is still too high to be considered in today's applications and the emitting wavelength is also limited to wavelengths above 1.55 µm. Therefore, integrating another material on Silicon seems to be unavoidable. A lot of materials have been considered to generate light into Si. This encompasses III-V compounds, carbon nanotubes, quantum dots, rare earth elements, etc. From all results published to date,

the most efficient lasers on Si have been developed from III-V semiconductors. Indeed, InP-based materials remain one of the best choices to fabricate efficient laser sources in the range of 1.3 - 1.55µm. However, in order to keep a low-cost, these devices must be integrated onto a Si substrate. Two different approaches are then possible: molecular layer bonding or direct epitaxy of III-V on Si. While the latter has been an exciting research topic for decades, the layer bonding is a pragmatic solution, which has allowed several demonstrations of III-V/Si hybrid devices, including light sources.

Furthermore, InP-based materials can also have several advantages for modulator integration. Indeed, Electroabsorption modulators can be achieved through absorption using the InGaAsP quantum well system via the quantum confined Stark effect. Such devices are classically used in electroabsorption modulated laser (EML) systems, and their integration has been demonstrated on Silicon [143]. But InP and InGaAsP also have interesting properties of refractive index variation with carrier concentration modulation, which is found to be much more efficient than that in Silicon [144,145]. This can be interesting to fabricate carrier-concentration-based modulators, with better efficiency than Si-only modulators.

III. III-V on Si photonics

III-V semiconductors are the materials of choice for the development of efficient optoelectronic devices for the next generations of photonic-electronic circuits. As a new material in the silicon photonics platform, some special attention has to be considered including material contamination and stability as well as the definition of new integration methodologies. In this section, the hybrid integration challenges are presented first, followed by the possible integration schemes of III-V materials on the silicon photonics platform.

III.1 Hybrid Integration Strategy

Place of III-V materials on Si photonics circuits

The schematic view shown in Figure 8 reports on a more exhaustive example of a typical PIC with patterned SOI, Si pn junctions for modulation, integrated Ge photodiodes, patterned SiN waveguides for alternative passive devices, a 4-level Cu BEOL (back end of line) for electrical routing, and Cu pillars for 3D bonding [146].

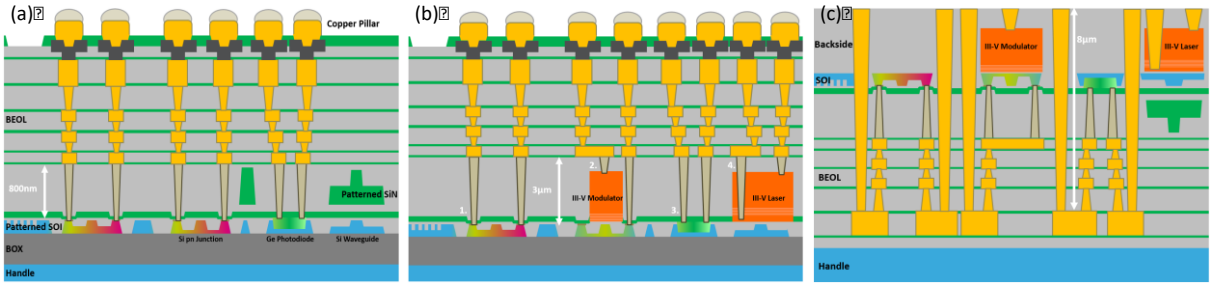

Figure 8: Schematic view of (a) a PIC showing the patterned SOI photonic devices and a second level of SiN photonic devices within the 4-level BEOL, (b) the co-integration challenge of having a 3µm high InP die to co-exist within the BEOL of the PIC. The contact level must open on silicon devices (1.), top III-V section (2.), germanium devices (3.) and bottom III-V devices (4.) and (c) Alternative integration strategy explored to overcome co-integration challenges between III-V and BEOL.

The rather complex PIC configuration shown in Figure 8a leaves little room for III-V integration without making some compromises. First, it is incompatible with a co-integration of SiN devices. Besides excluding the second photonic level, the challenge is to succeed in dealing with both the topology of the above-mentioned gain medium and the Si waveguide thickening. Moreover, in order to achieve large-

scale integration of the III-V material on silicon, one must avoid downsizing the wafer. In this case, the process steps following the die bonding must be done using CMOS foundry compatible process and material. Such integration has been demonstrated [147] on 200 mm wafer using localized waveguide thickening and CMOS compatible contact [148] and process, as demonstrated.
The other process to be adapted is the contact level, which must open on 4 different levels and 3 materials (Fig. 8b).
An alternative integration consists of flipping the wafer, bonding it to a new handle, etching the backside handle and bonding the III-V dies on the backside [149] In the proposed integration, the PIC is processed traditionally without any compromise, and the III-V is bonded subsequently on the other waveguide side (Fig. 8c), followed by an adapted second round of BEOL [150]
Other hybrid source integrations were proposed in the literature. For example, to overcome the challenges faced with thick gain regions, developments of thin III-V gain regions with lateral metallization were reported [151]. Another alternative is to suppress the Si waveguide cavity and patterning photonic crystals within the III-V to generate a resonant cavity [152-153]

III-V material integration on Si

State-of-the-art Si photonic platforms are nowadays fabricated on 200 and 300 mm wafers. However, III-V photonic platforms still use comparatively smaller wafers with sizes of 100 and 150 mm. Moreover, materials such as InP are very brittle compared to Si, which is more resistant mechanically. Pricewise, III-V wafers are more expensive than Si substrates irrespective of their size. Based on such assessment points, it appears that it makes more sense to import small III-V portions on Si rather than the other way around. There are two major ways to proceed, which have been widely reported: transfer bonding [154] and direct epitaxy [155,156]. The more matured integration method is transfer bonding and consists of preparing millimeter-size InP dies bonded on localized regions of a patterned and planarized SOI wafers (Figure 9).

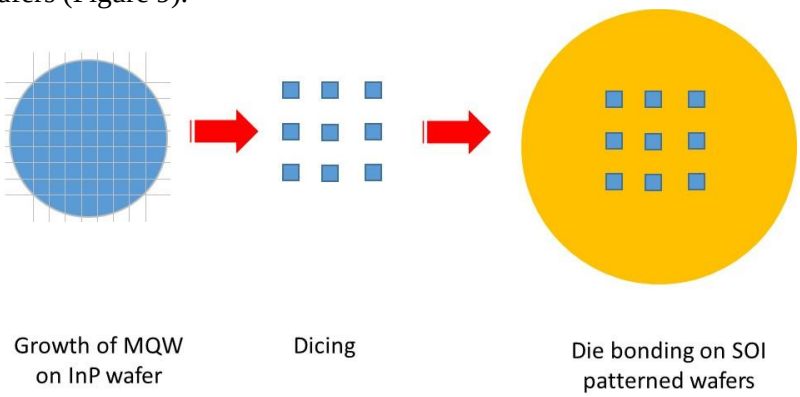

Figure 9: Hybrid integration strategy by die-to-wafer bonding of InP on SOI.

A faster and more efficient method than pick-and-place is to do a collective transfer of III-V dies using a die holder [157-158] . The technique consists of positioning the dies on an adapted surface and proceeding with the wafer bonding in a single step (Figure 10).

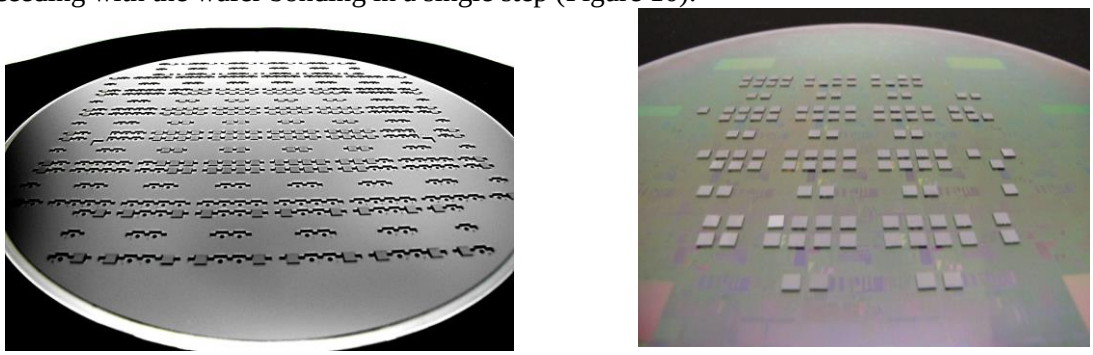

Figure 10: Experimental demonstration of collective die-to-wafer bonding on 200mm patterned SOI. Left picture is showing a silicon-based holder. Right picture presents III-V die bonder on patterned SOI wafer (in this case the Si-holder was not fully filled)

Transferring localized portions of III-V on a Si wafer corresponds to a major advancement. This crucial step enables the co-integration of Si devices, III-V devices, and hybrid devices within the same platform. In this case, alignment between the patterned Si and III-V device is managed with available lithography capabilities, which are definitely better than those of packaging level III-V device integration. Consequently, information transport (electrical or optical) is enhanced due to device proximity. Moreover, devices working within the same environmental conditions have almost the same operation shifts. Finally, the system footprint is reduced due to the redundant individual device packages. However, even if hybrid bonding opens the door to new possibilities, there are still other challenges to be met and satisfied. Typically, the difference in device aspect ratio between III-V and Si can result in both electrical and optical interconnection incompatibilities, depending on the integration scheme.
Hybrid laser integration is extensively explored and specific device architectures lead to tangible arguments about new challenges. A hybrid laser device usually consists of an InP gain medium pumped electrically using a Multiple Quantum Well (MQW) typically made up of stacks of InGaAsP (Figure). The MQW is designed such that the electrical band gap corresponds to the targeted optical bandwidth emission. It is addressed electrically within a p-doped and n-doped InP sandwich. Metal interconnections then connect the doped InP to the power supply. The other section of the laser consists of a Si waveguide cavity, which uses two cavity mirrors at both ends. The mode transition then occurs by favoring an interface between the gain medium and the cavity where adiabatic coupling can take place.

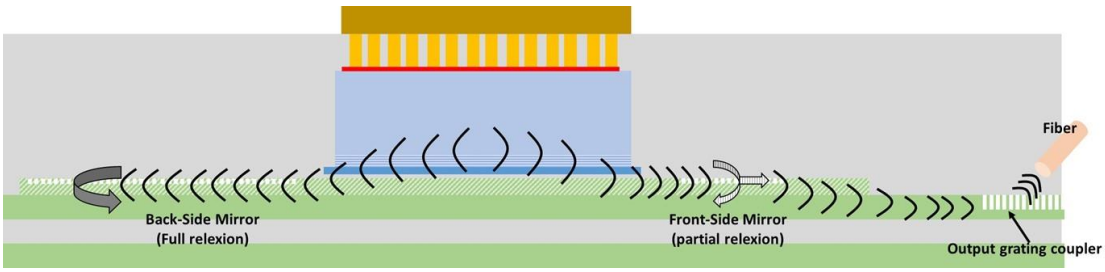

Figure 11: Schematics of integrated laser using InP dies as gain medium and SOI as resonant cavity.

In a proposed integration [159] the metal interconnection is done directly on top of the stacked p-doped InP (**Chyba! Nenašiel sa žiaden zdroj odkazov.**11). The p-doped region is thus limited to a minimum thickness of 2 µm to avoid absorption of the optical modes by the metal plate. Consequently, a device topology of about 3 µm and an optically active region of about 2 µm must be considered.
The thick optical region in the gain section has a direct impact on the adiabatic coupling with the underlying Si cavity. Lossless and low reflection coupling can only be achieved if a good effective index transition is performed around a matching point. Consequently, this implies that either very fine transition tips must be etched in InP (< 50 nm) or the Si waveguide has to be thicker. In the current integration, the SOI thickness is 500 nm, which is not compatible with conventional silicon photonics platforms mostly based on 220-nm- or 310-nm-thick SOI substrates.

Most of the demonstrations of integrated III-V laser on silicon photonics platform have been obtained by combining a silicon fabrication line and a conventional III-V device foundry to process the wafer with bonded III-V die. This solution implies to downsize the SOI wafer to a diameter supported by the III-V line, typically 4 inches. A preliminary version of a co-integrated Si modulator, together with a hybrid laser source and its associated BEOL was demonstrated [160] using this approach.
As the trend in silicon photonics is to go towards a complete integration of the photonic integrated circuit (PIC) and electronic IC (EIC), strategies have to be developed. One possible way, avoiding strong modifications of both photonics and electronics circuits, is to realize independent developments of the PIC with respect to the EIC. The two sub-systems are then combined using 3D integration by bonding one to another (Figure 12).

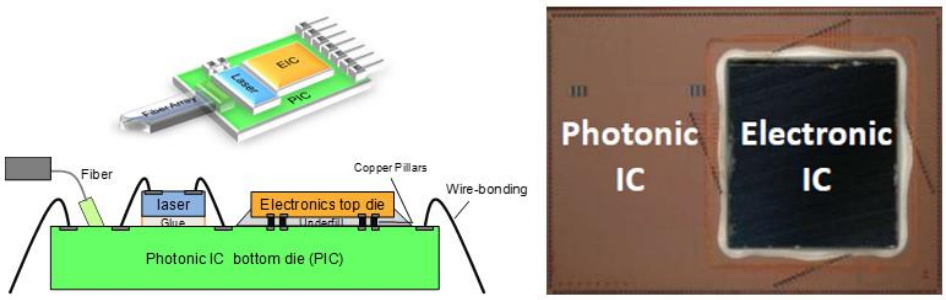

Figure 12: System level 3D assembly packaging strategy showing an EIC bonded on a PIC.

III.2 Hybrid optical Modulators

As described in section II.2, plasma-dispersion based phase-modulators are the most common way in silicon photonics to fabricate transmitters. The carrier concentration modulation is achieved using either a PN junction or a SIS (semiconductor-insulator-semiconductor) capacitor, and most of today's products are based on PN junction phase modulator working up to 56 Gbit/s [161]. As also pointed out, some challenges remain including efficiency and power consumption, which are too low to achieve with the current approaches. One possible way to overcome the limitation of optical modulators is to take the benefits of III-V materials in terms of **carrier**-induced property changes (Eq. 4 and 5). Especially, the effective mass of electrons and holes which are smaller in III-V materials compared to Si. For instance, a closer look to the refractive index variation with carrier concentration in InP reveals that the real part of the refractive index is improved with electrons in III-V materials, while the absorption and the hole mobility are degraded relative to silicon (For more information see ref 162).

The comparison and the evaluation of the performance of a modulator can be roughly governed by the β ratio of modulator's phase shift $\Delta\varphi$ and absorption α. Maximizing β, while keeping a good electrical bandwidth (e.g. low access resistance and low capacitance) is therefore a good criterion. Due to the low hole mobility and the higher free-hole absorption in III-Vs, fabricating a PN homojunction or a SIS in III-V materials would lead to non-optimal optical modulation amplitude (OMA) and may degrade RF performance. Therefore, using either Si or SiGe to fabricate the p-side while using III-V on the n-side has been proposed to integrate modulators. The comparison of β ratio for Si, SiGe and InGaAsP depletion based PN modulator is shown in Fig 13.

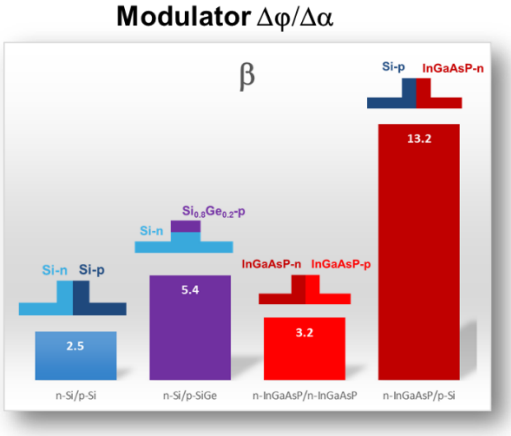

Fig 13: β ratio calculated for PN junction modulator configurations at the optimal OMA

Despite its theoretical interest, a hybrid III-V/Si PN junction phase shifter is difficult to integrate in practice due to the strong lattice mismatch between Si or SiGe and InP or InGaAsP. Nonetheless, SIS structure can be made using molecular bonding [162]. A typical example is shown in Fig 14.

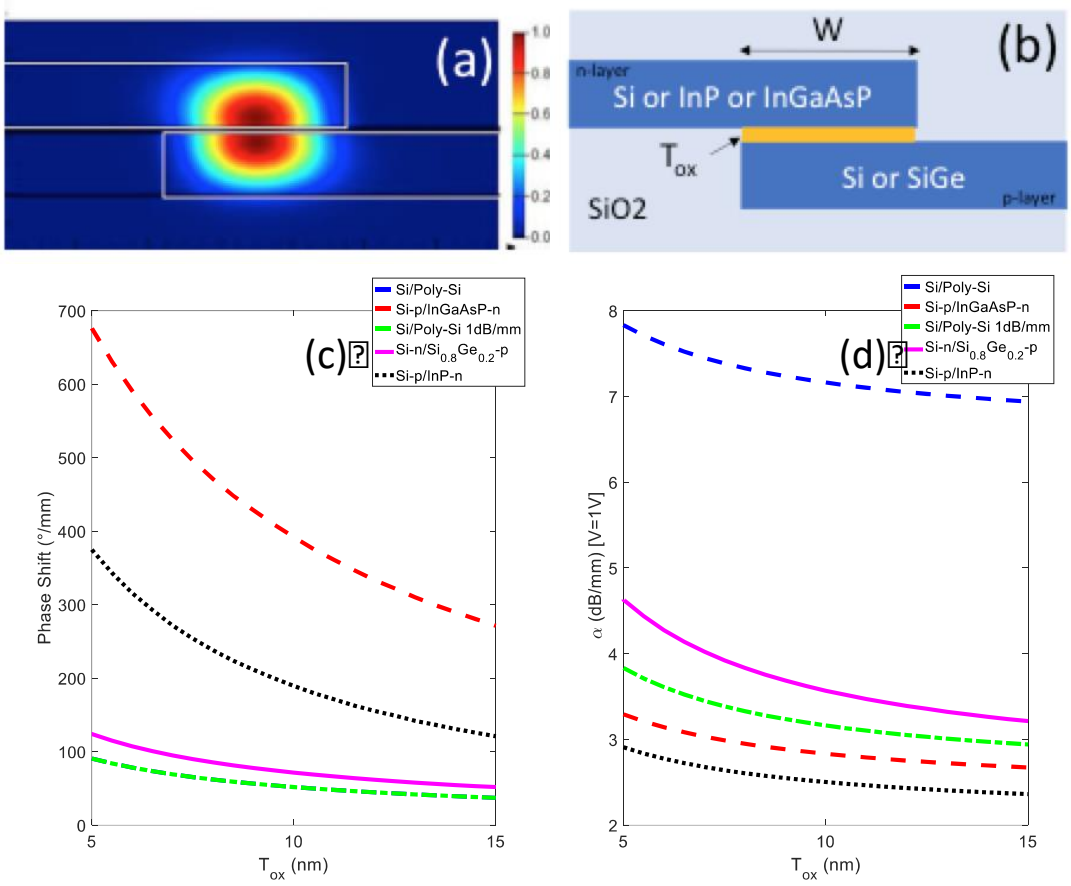

Fig 14: Example of SIS phase shifter structure: (a) optical mode profile and (b) schematic view. Simulated phase shift (c) and optical loss (d) as a function of the oxide gate thickness T_{ox} for several structure configurations.

The efficiency and loss of such hybrid SIS modulator have been evaluated [163] using a fixed structure (each of the layers are 120-nm-thick, waveguide width is W=0.45µm) for various configurations of materials, as a function of the oxide thickness T_{ox} (fig. 14). The hybrid InGaAsP/Si and InP/Si SIS modulators are showing the highest efficiency and the lowest losses, even for oxide thicknesses between 10 nm and 20 nm. Compared to a typical PN junction modulator, the $V\pi L\pi$ can be reduced by a factor of 10 to 50 at the optimal OMA point.
This first example is a perfect demonstration of the strong benefit to combine both III-V and Si properties.

III.3 Hybrid III-V/Si Transmitter

As reported in the introduction, monolithic integration of a transmitter including a hybrid laser together with a MZM based Si-modulator is a priority for the development of optical communication systems. For this purpose, a hybrid III-V/silicon laser was bonded on a silicon rib waveguide, with a 100-nm-thick SiO_2 gap between the III-V and Si layers. The III-V active region was 700-µm-long and 5-µm-wide. An intrinsic InGaAsP multiple quantum well (MQW), designed to exhibit maximum gain around 1.3 µm, surrounded by n- and p-doped InP layers is used as the gain medium. Light coupling in the silicon is realized by 100 µm long adiabatic tapers patterned in the silicon rib waveguide, located at each end of the III-V waveguide. Their simulated coupling efficiency is above 90%. Two shallowly etched Bragg gratings (10-nm etch depth, 3-µm-wide and 50% duty-cycle) are used for the to form the optical cavity. The Bragg gratings were 150-µm and 700-µm long with a grating strength $\kappa=78cm^{-1}$, giving reflectivity of 70% and 99%, respectively. The period of the gratings was 195 nm, to allow an

emission centered at 1302.6 nm.Optical modulation was performed by a silicon MZM modulator based on a *pn* junction in the depletion regime. Additionally, thermal shifters were used to control the static phase difference between the MZM arms and to shift the peak wavelength of the reflectors to tune the lasing wavelength. At a laser wavelength of 1303.5 nm, a 25 Gb/s transceiver was then demonstrated. The measured extinction ratio was 4.7 dB, and no signal distortion was observed after 10 km propagation. All these results are reported and detailed in ref. 164.

IV. Conclusion

Thanks to its transparency range and compatibility with CMOS processes, after 30 years of research silicon-based materials have emerged as an enabler of low-cost photonics systems. As optical transmission standard is becoming more and more complex, heading toward fully integrated chip-to-chip communications, and applications of integrated photonics are going beyond the Datacom realm, the development of efficient and versatile optical devices is needed. That includes low power modulators, efficient light sources, and athermal devices.

As it was mentioned, the optical properties of silicon itself do not address all requirements for all applications, especially for light sources. Consequently, the monolithic or hybrid integration of other materials into the silicon photonics structures is a promising approach that allows a judicious combination of efficient properties in a common Si platform. Among the numerous possibilities, the integration of III-V semiconductors on Si is very powerful and allows achieving efficient optoelectronic devices. Even so, there are still some open questions and challenges to address including the Si compatibility and the integration approach: bonding vs epitaxial growth and back-side vs back-end integration, the few demonstrations presented here of efficient laser and modulators on Si, already prove the benefit of such an approach.

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