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Metalorganic Chemical Vapor Phase Epitaxy Growth of Buffer Layers on 3C-SiC/Si(111) Templates for AlGa_N/Ga_N High Electron Mobility Transistors with Low RF Losses

Eric Frayssinet, Luan Nguyen, Marie Leseq, Nicolas Defrance, Maxime Garcia Barros, Rémi Comyn, Thi Huong Ngo, Marcin Zielinski, Marc Portail, Jean-Claude De Jaeger, and Yvon Cordier*

Herein, the interest of cubic silicon carbide as a template for the growth of AlGa_N/Ga_N high electron mobility transistor (HEMT) heterostructures on silicon substrates for high-frequency operation is shown. On the one hand, 0.6–0.8 μm-thick 3C-SiC grown by chemical vapor deposition on intrinsic silicon substrate having initial resistivity superior to 5 kΩ cm enables the metalorganic vapor phase epitaxy of Ga_N buffer layers with propagation losses below 0.4 dB mm⁻¹ at 40 GHz and 0.5 dB mm⁻¹ at 67 GHz. On the other hand, an HEMT heterostructure is grown on 1.5 μm-thick 3C-SiC on 4° off-axis silicon substrate having an initial resistivity superior to 200 Ω cm that allows to keep a sufficiently resistive epilayer stack limiting the loss up to 0.78 dB mm⁻¹ at 40 GHz. Device process developed on a piece of the 100 mm diameter wafer leads to the demonstration of DC transistor operation with low leakage currents. Compared with direct growth on silicon, these templates enable reduced radio frequency (RF) propagation losses that are very interesting for high-frequency transistors and circuits operation.

1. Introduction

A Ga_N-on-silicon high electron mobility transistor (HEMT) technology has been identified as a promising way to develop high-frequency telecommunication and power switching systems at large scale due to the availability of large diameter and low-cost substrates. Difficulties associated with the growth of high lattice-mismatched materials and large thermoelastic strain have been mainly overcome with Ga_N/Al(Ga)_N-based buffer layers grown on AlN nucleation layers. However, achieving high electrical resistivity layers remains a major concern especially for the production of low radio frequency (RF) loss epilayers for efficient high-frequency transistors and circuits for applications such as 5G.^[1]

Not only this necessitates the use of high-resistivity substrates^[2] but also requires the achievement of both sufficient crystal quality and electrical resistivity regarding AlN/silicon interface. The control of the electrical behavior of such structures is still challenging. The parasitic diffusion of dopant species into the silicon substrate,^[3,4] the formation of an inversion layer at AlN/Si interface,^[5–8] and degraded crystal quality have been reported as possible origins of parasitic conductivity and propagation losses.^[6,9] This point is highly critical for the growth with metalorganic chemical vapor phase epitaxy (MOVPE) whose competitive advantages for production are mitigated by the drawbacks associated with the difficult trade-off between crystal quality degradation at low growth temperature^[6,10] and possible diffusion of Ga or Al doping elements toward the substrate within high-temperature nucleation or growth process. To mitigate these drawbacks, various solutions were proposed to achieve good crystal quality layers and interfaces with high electrical resistivity, such as modification brought in the waveguides topology, inserting buried p–n junctions in the substrate,^[11] or using a lower growth temperature technique such as molecular beam epitaxy (MBE).^[12] In the present work, it is proposed to insert an additional layer made of cubic silicon carbide (3C-SiC) from which and through which the diffusion of dopants or its consequences is expected to be less likely due to its bandgap of 2.3 eV. Furthermore, when such

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a material is grown thick enough (several hundreds of nanometers in our case), it provides a template with reduced lattice mismatch strain with GaN (3% vs 17% for Si) and reduced thermoelastic strain after GaN-based structure regrowth, which can help for simplifying the design and the growth of the buffer layers.^[13] The thermoelastic strain is reduced due to a thermal coefficient of expansion of $4.5 \times 10^{-6} \text{ K}^{-1}$ intermediate between the ones of GaN ($5.6 \times 10^{-6} \text{ K}^{-1}$) and Si ($3.6 \times 10^{-6} \text{ K}^{-1}$). The availability of chemical vapor deposition (CVD) reactors for growth of SiC on large diameter substrates is an advantage for the rapid development of such technology. To the authors knowledge, the only reported data to date concern GaN-based HEMTs on 3C-SiC templates with conductive silicon^[14–16] impeding RF wave propagation performance. In the present work, it is demonstrated MOVPE grown HEMT with 3C-SiC on resistive silicon for transistor devices with low RF propagation losses.

2. Experimental Section

2.1. Buffer Layers Growth and Characterization

In the present study, 0.6–1.5 μm -thick 3C-SiC templates were grown around 1300 °C by chemical vapor deposition in a resistively heated hot wall reactor^[17] using a conventional two-step method.^[18] Propane and silane precursors were used with hydrogen as carrier gas. When grown on nominal Si(111) substrate, the 3C-SiC thickness was limited below 1 μm to avoid layer cracking, but the growth on 4° off-axis substrate induced a reduced tensile stress allowing to reach larger thicknesses.^[19] The GaN structures were grown in a Aixtron close-coupled showerhead system. For the purpose of comparison, buffer layers with the same layers stacks were grown on such templates as well as on classical Si(111) substrates with nominal orientation. The silicon substrates with nominal orientation were undoped with a resistivity superior to 5 k Ω cm. These 50 mm diameter substrates were 500 μm thick. The substrate with 4° offcut was n-type doped with phosphorus. The resulting resistivity was superior to 200 Ω cm. This 100 mm diameter substrate was 1 mm thick. In the studied samples, the buffer consisted of a 600 nm GaN/350 nm AlGa_xN/200 nm AlN stack (Figure 1). After oxide removal around 1000 °C (1200 °C thermocouple set point) under hydrogen flow, a thin (20 nm) AlN layer was nucleated at a set point fixed to 1100 °C. Then, the temperature was ramped up to 1200 °C set point for the remaining growth of 180 nm AlN and the rest of the structure. The resulting structures on 3C-SiC/Si(111) templates were free of cracks. However, the direct nucleation and growth of AlN on Si(111) using the same temperature set points resulted in poor and not reproducible crystalline quality with very rough layers. To mitigate this effect, the AlN nucleation and growth temperature set points had been increased by 50 and 150 °C, respectively. These changes resulted in more acceptable quality, and crack-free structures had been obtained without changing the growth parameters for AlGa_xN nor for GaN. The crystalline quality of the layers was assessed by X-ray diffraction (XRD). As shown in Table 1, the growth on the thicker 3C-SiC template (1.5 μm 3C-SiC) results in enhanced quality with smaller full width at half maximum (FWHM) of symmetric (002) and asymmetric (103) (302) peaks for AlN and GaN, respectively.

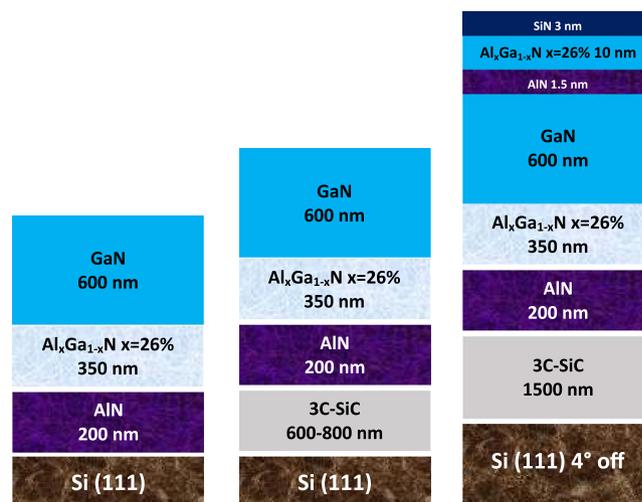


Figure 1. Cross-sectional view of the studied structures grown by MOVPE on Si(111) and 3C-SiC/Si(111) templates.

This was consistent with our previous observations^[13,14] and the enhancement of the 3C-SiC crystal quality, as the FWHM of SiC(111) peaks dropped down from 0.5° to 0.2° for the thicker film. Furthermore, it was noted that despite the higher temperature set points for AlN on Si(111), the crystalline quality was still less compared with the one of layers grown on the 3C-SiC templates. However, even on these templates, the FWHM values for GaN were still rather high due to the reduced thickness of the films (600 nm for GaN) chosen here to avoid cracks in a simple buffer layer stack with a single 350 nm AlGa_xN layer. The surface morphology of the as-grown 3C-SiC was assessed with atomic force microscopy (AFM). As shown in Figure 2a, compact and relatively smooth 3C-SiC is obtained on nominal silicon with a root mean square (RMS) roughness of 4 nm, which is reduced after the GaN epilayer growth, showing an RMS roughness between 0.5 and 1.5 nm as well as the presence of pits due to threading dislocations with densities in the range of low 10^9 cm^{-2} (Figure 2b). The surface morphology is quite similar to the one obtained after the direct growth on Si(111) (Figure 2c). In contrast, the 3C-SiC template on 4° off silicon was noticeably rougher and has been polished to reduce the RMS roughness below 1 nm prior to the GaN buffer regrowth followed by the HEMT active layers (see later). Figure 2d shows the AFM pictures of the surface morphology of such HEMT with $5 \times 5 \mu\text{m}^2$ and $2 \times 2 \mu\text{m}^2$ scans. Few pinholes were present and indicate that progress in polishing or regrowth remained to be done. Furthermore, unlike on previous GaN buffers, terraces were not visible due to the presence of the amorphous SiN layer in situ grown to protect the AlGa_xN barrier. According to our previous studies, the growth of the HEMT active layers did not drastically change the roughness of the buffer layer estimated around 1 nm in regions excluding the pinholes, which was not far from the roughness of GaN buffer on the on-axis template.

Figure 3 compares the XRD 2θ – Ω scan recorded on the structures having the buffer grown on the 0.8 and 1.5 μm 3C-SiC templates. Although the reflexion peaks for GaN, AlGa_xN, AlN, and 3C-SiC appeared at similar angles, which indicated similar strain state, the presence of well-defined Pendellösung fringes

Table 1. XRD peak full width at half maximum for AlN and GaN in the buffer stacks grown on Si(111) and 3C-SiC/Si(111) templates, AFM RMS roughness, and propagation loss at 40 GHz.

| Substrate/template | XRD FWHM | | | | AFM roughness | Loss at 40 GHz |
|-----------------------|---------------|---------------|---------------|---------------|---------------|------------------------|
| | AlN (002) | AlN (103) | GaN (002) | GaN (302) | rms [nm] | [dB mm ⁻¹] |
| Si(111) | 0.65° (2340") | 0.87° (3130") | 0.32° (1150") | 0.88° (3170") | 0.5 | 2.0 |
| 3C-SiC/Si(111) | 0.56° (2012") | 0.56° (2030") | 0.36° (1307") | 0.59° (2149") | 0.5–1.5 | 0.38 |
| 3C-SiC/Si(111) 4° off | 0.25° (900") | 0.42° (1512") | 0.30° (1080") | 0.43° (1548") | 0.8–1.2 | 0.78 |

for the structure on the thicker template attested its enhanced crystalline quality.

The samples had been cut into pieces to make further electrical characterizations and process step when required. The sheet resistances of the substrates and the regrown films were measured by a contactless setup based on eddy current measurement. 3C-SiC templates of 0.6–0.8 μm thick on nominal high-resistivity (>5 kΩ cm) intrinsic Si(111) exhibited resistances beyond the maximum range of contactless setup (20 kΩ sq⁻¹), attesting the high resistivity of the 3C-SiC film. Furthermore, Hg probe capacitance–voltage measurement indicated that the 3C-SiC layer was totally depleted from carriers by the surface potential and the residual donor concentration around 10¹³ cm⁻³ in the underlying silicon. Propagation losses were measured in the 0.25–67 GHz frequency range on coplanar wave guides fabricated on such templates. Losses increased with frequency from

about 0.3 dB mm⁻¹ at 10 GHz up to 0.45 dB mm⁻¹ at 50 GHz. The sheet resistance of samples grown for this study varied noticeably with the growth parameters, especially in absence of the 3C-SiC intercalated layer. With the previously described growth conditions permitting to obtain crack-free buffer layers, the sheet resistance increased beyond 20 kΩ sq⁻¹ on the 3C-SiC/Si(111) templates, whereas it dropped to about 2 kΩ sq⁻¹ on Si(111). The choice of the growth parameters on Si(111) was the result of a trade-off. Lower temperatures led to sheet resistances up to 5 kΩ sq⁻¹, but epilayers had shown asymmetric XRD peak FWHMs beyond 1°. In contrast, further increase in AlN nucleation and growth temperatures led to an enhancement of crystalline quality but to a drastic reduction of the sheet resistance below 1 kΩ sq⁻¹. A direct consequence of the improvement of the resistance was a drop of RF propagation losses from 2 dB mm⁻¹ on silicon down to 0.4 dB mm⁻¹ at 40 GHz on the

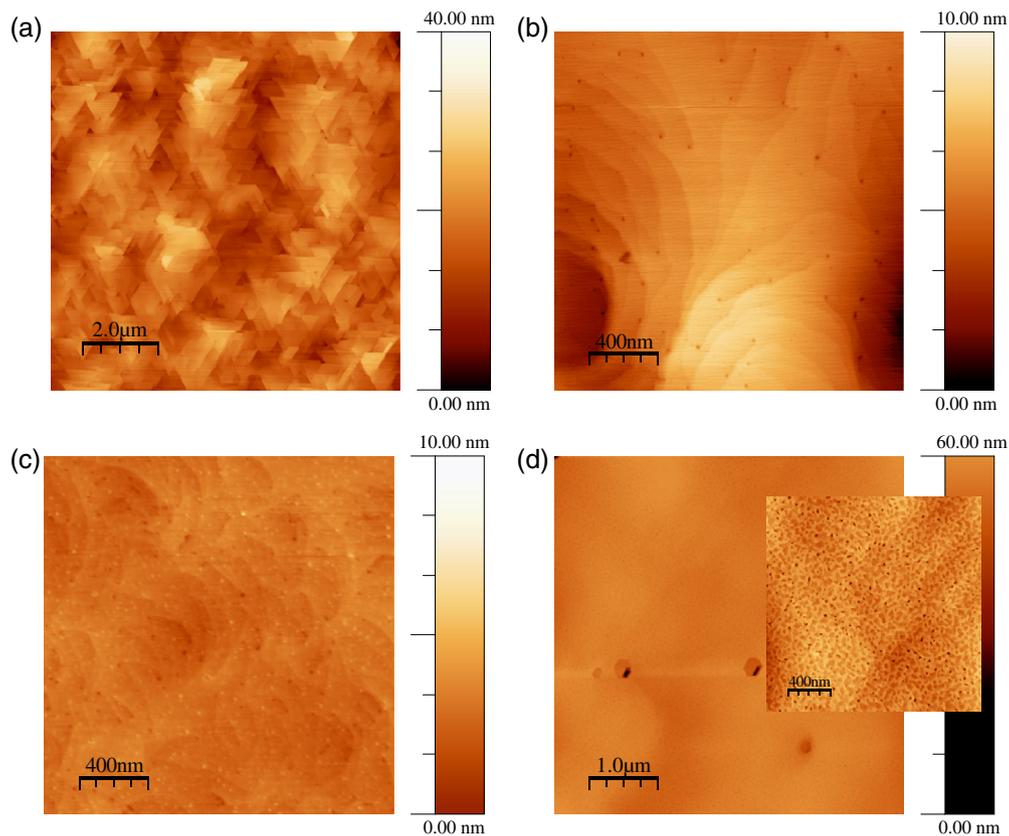


Figure 2. a) Tapping mode AFM view of the surface of a 0.8 μm-thick 3C-SiC template ; b) GaN buffer grown on such template and c) directly grown on Si(111). d) Views of the surface of the HEMT structure grown on the 1.5 μm-thick 3C-SiC template.

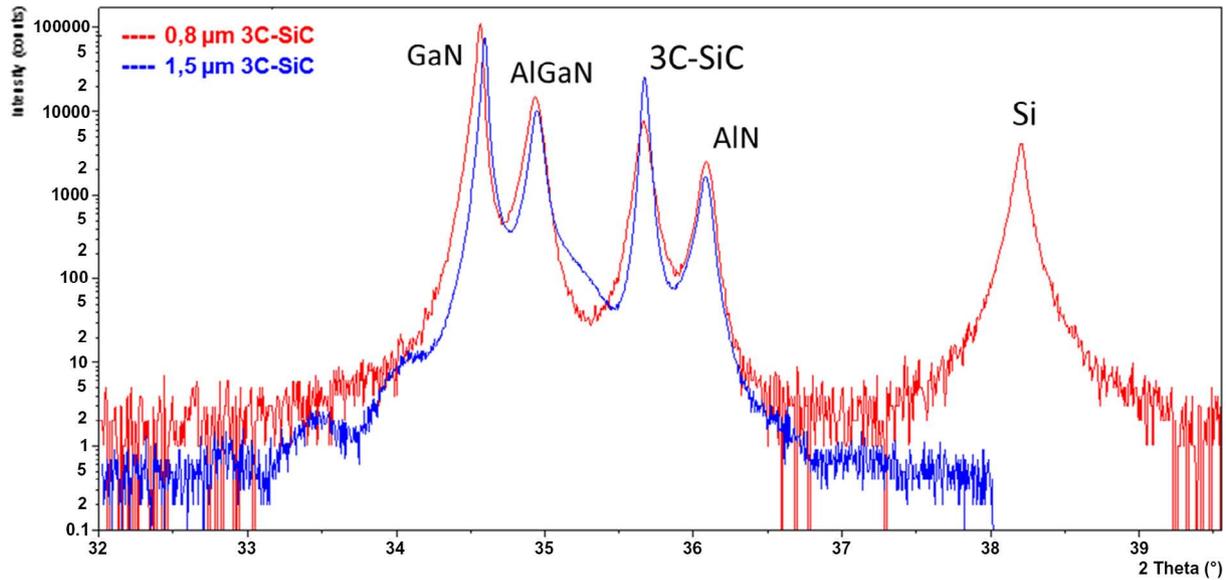


Figure 3. XRD 2θ - Ω scans showing the (0002) reflexion peaks of the AlGaIn/GaN HEMT structure grown on 1.5 μm thick 3C-SiC and the buffer layers grown on 0.8 μm 3C-SiC.

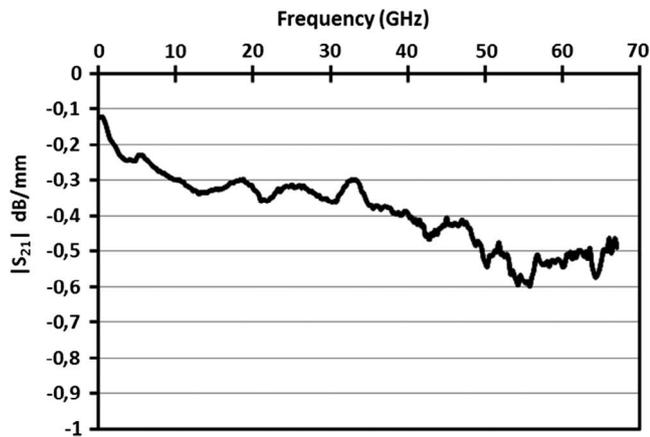


Figure 4. Propagation losses measured on coplanar wave guides fabricated on the GaN buffer layer on 0.8 μm -thick 3C-SiC on Si(111) with high resistivity.

3C-SiC template, as shown in **Figure 4**. Furthermore, losses remained of the order of 0.5 dB mm^{-1} up to 67 GHz, which was of high interest for the fabrication of efficient monolithic microwave integrated circuits (MMICs). Due to capacitive coupling with the substrate acting as a parasitic load, propagation losses and transistor performance were dependent with the effective resulting substrate resistivity and buffer layer thickness.^[2] But other parameters such as the crystalline quality and the thickness of AlN nucleation layer played a major role, for instance, with the possibility to generate an inversion layer at the AlN/Si interface or to generate high-frequency electrically active states in the epilayers.^[6,9] It is important to note that to limit losses to 1 dB mm^{-1} at 40 GHz with direct MOVPE growth on Si(111), Luong et al.^[6] used growth conditions resulting in a noticeably degraded AlN crystal quality with (002) XRD

FWHM of 1.9° . In the present study the FWHM is 0.25° – 0.56° on the 3C-SiC templates and 0.65° on the sample grown on silicon (Table 1). The reduced lattice parameter mismatch between 3C-SiC and AlN enabled a noticeably better crystal quality of the epilayer despite the low growth temperature.

2.2. Transistor Demonstration

The following step in the demonstration of the feasibility of high-resistivity crack-free buffer/substrate ensemble for RF devices and circuits was the assessment of a transistor epitaxy. For this purpose, the HEMT heterostructure grown on the 1.5 μm -thick 3C-SiC/Si(111) template had been evaluated. It was reminded that this template was grown on a $200 \Omega \text{ cm}$ resistivity silicon substrate with a resulting sheet resistance of

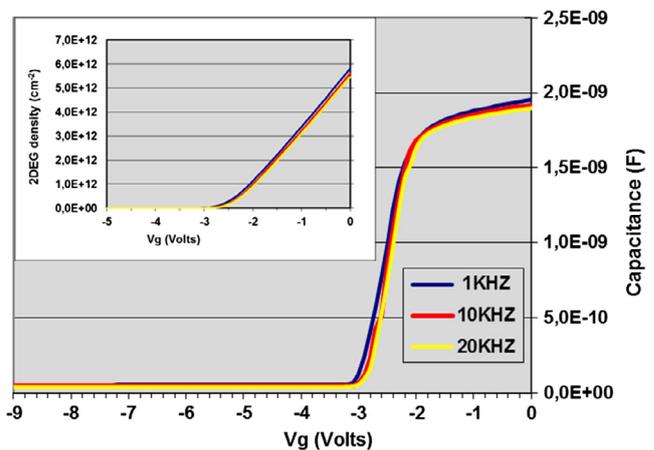


Figure 5. Mercury probe capacitance-voltage profile of the HEMT epilayer.

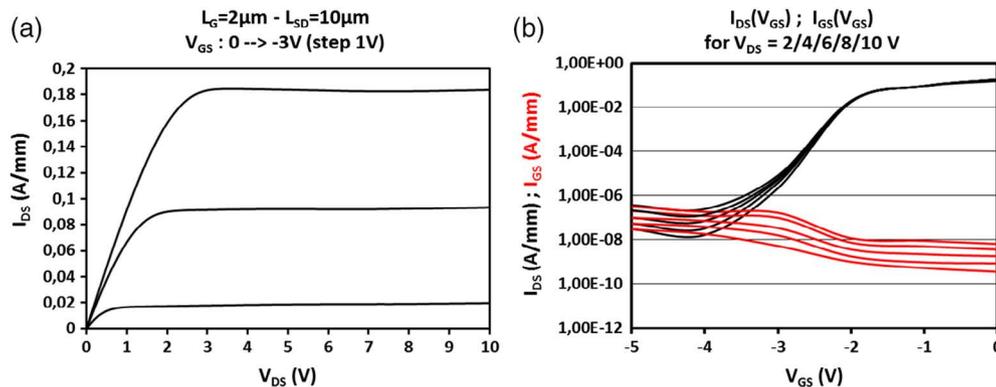


Figure 6. Transistor a) DC output and b) transfer characteristics showing low drain and gate leakage currents.

about $5000 \Omega \text{sq}^{-1}$. The high electrical resistance of the buffer layer had been checked with contactless setup after removal of the HEMT active layers from a part of the wafer using reactive ion etching. The growth of the GaN buffer stack on such a template did not induce any noticeable change in the sheet resistance, confirming the high electrical resistivity of the epilayers. On another piece of the wafer, coplanar wave guides fabricated on the HEMT structure after isolation by N^+ ion implantation indicated losses up to 0.78 dB mm^{-1} at 40 GHz, consistent with the contactless sheet resistance. As shown in Figure 1, the HEMT device structure consisted of the previously described buffer stack followed by a 1.5 nm AlN exclusion layer and a 10 nm $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier capped with a 3 nm in situ grown SiN passivation layer.

The electrical behavior of the heterostructure was first assessed by capacitance–voltage measurements in the 1–20 kHz range using a mercury probe with 800 μm diameter dot. The capacitance plateau related to the presence of a 2D electron gas (2DEG) at the AlN/GaN interface is shown in Figure 5, as well as a sharp pinch-off around -2.5 V attesting the low electrical defect or residual donor density in the layers estimated around $2 \times 10^{14} \text{ cm}^{-3}$ from the capacitance slope. The sheet resistance of the whole structure including the substrate was estimated at $570 \Omega \text{sq}^{-1}$ with the contactless setup. Subtracting the $5 \text{ k}\Omega \text{sq}^{-1}$ contribution of the buffer/substrate system led to $643 \Omega \text{sq}^{-1}$, which seemed reasonable for such an HEMT structure with a 2DEG density estimated around $5.5 \times 10^{12} \text{ cm}^{-2}$ after integration of the capacitance (inset of Figure 5).

Transistors with 2 μm length NiAu gates in 10 μm source to drain spacing and 100 μm development had been fabricated using UV photolithography. Device isolation was achieved by ion N^+ implantation. Ti/Al/Ni/Au ohmic contacts were deposited using electron-beam evaporation and annealed at 850 °C under nitrogen atmosphere. TLM measurement provided sheet resistances in the range of 484–551 Ωsq^{-1} , but the contact resistance was around 3 Ωmm and so annealing conditions needed to be further optimized to take into account the thermal behavior in presence of the thick 3C-SiC layer. Despite these limitations, transistors with a knee voltage of few volts and a clear saturation of the drain current and a good charge control had been obtained, as shown in Figure 6. At last, the leakage current measured between 100 μm width isolated

patterns separated by 5 μm spacing was below 10 μA at 50 V and at pinch-off, a $I_{\text{on}}/I_{\text{off}}$ ratio of about 10^6 and a gate leakage below $0.1 \mu\text{A mm}^{-1}$ were observed confirming the resistivity of the buffer layer and the quality of the Schottky gate contact.

3. Conclusion

In the present study, it is demonstrated that GaN/AlGaN/AlN highly resistive buffer layers are grown by MOVPE on high-resistivity 3C-SiC/Si(111) templates with high-frequency propagation losses ranging from 0.5 to 0.8 dB/mm up to 67 GHz depending on the initial silicon substrate resistivity. A clear benefit in terms of crystal quality of the AlN nucleation layer grown at low temperature arises from the insertion of a 3C-SiC layer. This study also shows that an HEMT heterostructure can be grown on such templates and transistors with good DC characteristics and low drain and gate leakage currents were fabricated. The development of these structures compatible with HEMT transistor fabrication is a first step in the demonstration of efficient high-frequency power HEMT transistors and MMICs.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

epitaxy, GaN on silicon, radio frequency, transistors

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