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# Digital Twin Real-Time FPGA implementation for light electric vehicle propulsion system using EMR organization

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**Abstract**—The paper focuses on implementation of several different concepts of wise analysis of light electric vehicle propulsion unit testing facility. Firstly, the concept of “digital twin” that represents a simulated replica of a complete testing facility is presented. More, instead of using an off-line simulation environment, the digital twin (DT) is programmed to run using two field programmable gate arrays (FPGA), hence it becomes an online real-time simulation. The second concept is the distribution of the digital twin. The actual unit controller is programed into one FPGA and the machine under test, its load and the power inverter are implemented into a second FPGA. The communication between the two is handled using analog and digital lines, just like the controller would be connected to the real test-bench. The third concept involves the organization of each of the two FPGA programs, based on Energetic Macroscopic Representation (EMR) that facilitates transparency, ease of implementation and minimizes the error in coding the actual test-bench replica and then its controller. Combining all the above mentioned concept into one single lucrative tool, experimentally validated by actual measurements, proves that the concept of using a DT implemented in real-time, without doubt can be used for testing prototypes and their controls regardless of the actual test-bench. Hence, on one hand it is eco-friendly, precise and save testing method and on the other hand, the same DT can be used by researchers and testers in facilities that do not have a test-bench at their disposal.

**Keywords**—Digital Twin, Real-Time, FPGA, EMR

## I. INTRODUCTION

The development of electric vehicles in the field of research in the last decade gained a lot of interest in nearly all directions of electrical engineering. Developing optimal designs both for controllers and electrical machines are daily challenges for many researchers. All the studies start from computer based simulations using dedicated environments specially designed for such studies. The second step is transitioning from simulation to real hardware building and testing [1-2]. Usually, test-benches are built to replicate the simulated solutions and comparative analysis between the results of the two environments are approached. After the test-bench is operational, usually, optimization of the control unit for lower power losses, several control strategies, faulty operations and different malfunctions are tested. In doing so, firstly, depending on the power of the machine under test, a lot of electrical energy is consumed with direct impact in the price of the development of the final product. On the other hand, testing for different control strategies, sometimes can

lead to faulting the inverter or the machine. Also, testing operation in several faulty scenarios, requires to intentionally fault some components of the test-bench.

The objective of the paper is to build a digital twin (DT) as a replica of a complete test-bench to help for the above-mentioned issues. The main difference between a DT and a signal HiL is that generally, the latter is built before the actual hardware is installed to test via powerful simulations a concept, while the DT is created after the actual testbench exists to have its digital replica usable independent of the actual hardware facility. Even more, when implementing the concept using real-time targets such as the FPGA, closes more the gap between simulation and actual testing. In the present paper these concept are detailed together with the EMR (Energetic Macroscopic Representation) of the entire system that proves to be the best solution for organizing such a complex system [3-4]. The DT of the actual test bench considered in the present study takes into account all its elements such as control unit, the machine under test with its electronics and the load machine with its attached programmable electronic load. The actual test-bench uses one FPGA as controller for all the devices used (electronic inverter, electronic load and electronic resolver) [5]. When designing the digital twin, the FPGA controller that normally was connected to the test-bench, remains programed with the same code, but instead of connecting it to the test-bench will be connected to another FPGA. The latter contains the complete model of the actual test-bench with all its assemblies.

The two FPGAs communicate using analog IOs for measuring the currents and voltages and digital IOs for sending the PWM signals and fetching the simulated resolver data [6-7]. Practically, replacing the test-bench with its digital twin becomes seamless from the controller’s point of view. Hence, the general scope of work is to prove the strategy of implementing a signal HiL unit that operates as digital twin of an actual testbench.

Another great advantage is that when transitioning from the digital twin to the test-bench (back and forth), requires only unplugging the FPGA that contains the DT and connecting the actual hardware and vice-versa, proving the benefit of such approach against simple software simulation. In the paper the results from the DT were compared only to actual measurements, the interest being to prove the similarity between the DT and the real hardware. Comparison to software simulators was out of the interest of the paper. In

order to be able to build a DT of such a test-bench, one requires to have correct and precise identified data of all the hardware assemblies. The data required to build the DT was identified using methods that are widely present in the common literature. However, for the sake of demonstration no saturation machine saturation or FET driver deadtime was considered, these being future investigations in this area of interest.

## II. METHODOLOGY OF IMPLEMENTATION

### A. The actual test-bench

In order to build a correct and complete digital twin of an existing test-bench, it is necessary to know all the assemblies composing it as well as all the data required to describe each of them using mathematical interpretations.

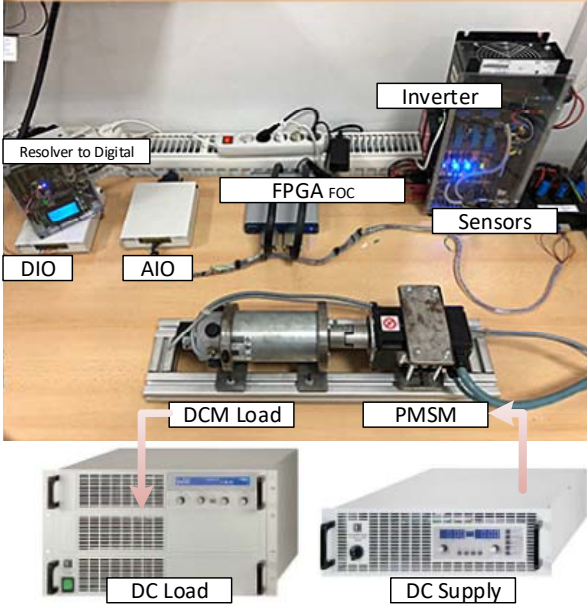


Fig. 1. The laboratory test bench

In fig. 1, the complete test-bench is depicted. This contains the FPGA as control unit, a 3 phase permanent magnet synchronous machine (PMSM) as machine under test together with its electronic inverter, the DC machine as load (DCM). The PMSM is supplied by a programmable DC supply while the DCM is controlled by a programmable DC load in order to obtain the desired load (torque and power) in the PMSM.

TABLE I. THE PMSM & DCM RATINGS

<b>PMSM Data</b>	
DC link voltage	$U_{DC}=50\text{ V}$
RMS current	$I=28\text{ A}$
Output power	$P_{2N}=0.3\text{ k W}$
Rated torque	$T=2\text{ Nm}$
Rated speed	$n_N=1500\text{ rpm}$
Number of poles	6
<b>DCM Data</b>	
DC link voltage	$U_{DC}=65\text{ V}$
RMS current	$I=4.6\text{ A}$
Output power	$P_{2N}=0.256\text{ k W}$
Rated torque	$T=1.4\text{ Nm}$
Rated speed	$n_N=1850\text{ rpm}$
Torque constant	$0.250\text{ Nm/A}$
Voltage constant	$29.5\text{ V/10}^3\text{ rpm}$

For the PMSM the identified parameters used in modeling and also used in the control unit are: stator resistance  $R_s=0.07\Omega$ , the inductances on the DQ axes are  $L_d=0.0002\text{ H}$  and  $L_q=0.0002\text{ H}$ . From the mechanical point of view, the inertia is  $J=0.00332\text{ kg}\cdot\text{m}^2$  and the friction coefficient is  $B=0.00122\text{ N}\cdot\text{m}\cdot\text{s}$ .

### B. EMR representation of the digital twin

Based on the information about all the assemblies of the test-bench its EMR representation can be designed. EMR is a graphical formalism to organize the models and the control of subsystems within a complete system. The concept of EMR organization and the rules attached to it are described in detail in [4]. In fig. 2, the entire EMR organization of the DT is depicted. It can be observed that the DT is divided onto the two FPGAs. One handles the model of the electrical machines mechanically coupled, the inverter and the load, while the second one contains the complete control unit. The communication between the two FPGAs is handled using analog and digital IO channels in order to mimic the actual test-bench. By this, the control unit does not have information if it is controlling the actual test-bench or its digital twin modelled on a FPGA.

The complete DT is monitored using a real-time GUI that in fact allows the user to impose different behavioral characteristics and to stream data from the models into data files.

Each block used in the model to represent actual assemblies from the test-bench or control unit was numbered in order to ease its relation to the following explanations and mathematical expressions.

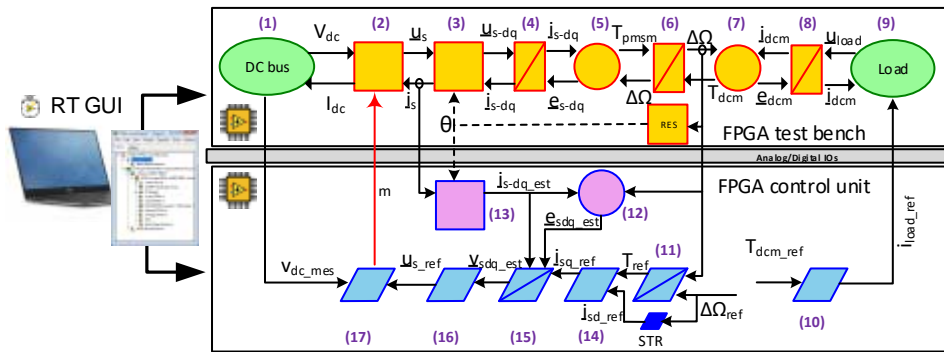


Fig. 2. The EMR representation of the DT

The DC bus block, (1) in fact is a constant that imposes the inverter's capacitor voltage at 50V. The second block (2) is in fact the replica of the inverter which based on the received 3 phase PWM signals (m) received from the controller to create the switched voltages. The  $PWM_{a,b,c}$  values are 0 or 1 as the (m) signal imposes it.

$$V_{DC} = 50 \quad (1)$$

$$\begin{aligned} V_{ab} &= V_{DC} \cdot (PWM_a - PWM_b) \\ V_{bc} &= V_{DC} \cdot (PWM_b - PWM_c) \\ V_{ca} &= V_{DC} \cdot (PWM_c - PWM_a) \end{aligned} \quad (2)$$

The third block (3) is the direct Park transformation from 3-phase DQ0 quantities. This is based on having the accurate rotor position ( $\theta$ ) at disposal.

$$\begin{aligned} U_\alpha &= U_{ab} \\ U_\beta &= (U_{ab} + 2 \cdot U_{bc}) / \sqrt{3} \\ U_D &= -U_\alpha \cdot \sin(\theta) + U_\beta \cdot \cos(\theta) \\ U_Q &= -U_\alpha \cdot \cos(\theta) + U_\beta \cdot \sin(\theta) \end{aligned} \quad (3)$$

The forth block (4) represents the model of the machine windings detailed directly in DQ form. For these calculations, it is mandatory to have correct information about the DQ inductances and the resistance of the phases of the machine.

$$U_{sDQ} - e_{sDQ} - (i_{sDQ} \cdot R_s) = L_{DQ} \frac{d}{dt} (i_{sDQ}) \quad (4)$$

The electromechanical conversion is the fifth block (5) that leads to the PMSM torque and the DQ components of the back emf computed from the stator currents, the machine parameters and the velocity of the rotor.

$$\begin{aligned} T_{PMSM} &= 3/2 \cdot p \cdot i_{sQ} (\psi_{PM} + (L_{sD} - L_{sQ}) \cdot i_{sD}) \\ e_{sD} &= -\psi_{sD} \cdot \omega \\ e_{sQ} &= \psi_{sQ} \cdot \omega \\ \psi_{sD} &= L_{sD} \cdot i_{sD} + \psi_{PM} \\ \psi_{sQ} &= L_{sQ} \cdot i_{sQ} \\ \omega &= \Omega \cdot p \end{aligned} \quad (5)$$

In eq.(5) p denotes the number of pole pairs,  $\psi_{PM}$  the permanent magnet flux and  $\omega$  the angular velocity of the machine.

The sixth block, corresponds to the mechanical conversion delineated from the torque produced by the PMSM, the load torque of the DCM, the friction coefficient B and the total inertia of the two machines, J.

$$J \frac{d\Omega}{dt} = T_{PMSM} - T_{DCM} - B \cdot \Omega \quad (6)$$

The seventh block (7) represents the torque and the back emf produced by the DCM, computed function of the machine current, the shaft velocity and the torque and voltage constants of the machine, detailed in table I.

$$\begin{aligned} T_{DCM} &= I_{DCM} \cdot kt_{DCM} \\ e_{DCM} &= \Omega \cdot ke_{DCM} \end{aligned} \quad (7)$$

The winding model of the DCM is described in block no. 8 and it is computed function of the machine parameters and the supply/load voltage of the machine.

$$U_{load} - e_{DCM} - (i_{DCM} \cdot R_{DCM}) = L_{DCM} \frac{d}{dt} i_{DCM} \quad (8)$$

In order to create a replica of the electronic load (block 9), that normally receives the imposed current and computes the voltage that needs to be supplied to the load to reach the desired current, a PI controller was implemented that outputs the desired voltage to reduce to null the error between the imposed and the actual DCM current.

$$U_{load} = k_p \cdot (i_{DCM\_ref} - i_{DCM}) + k_i \cdot (i_{DCM\_ref} - i_{DCM}) \quad (9)$$

All the blocks detailed till this moment (1-9) were implemented in the FPGA that models the best-bench.

The signals received or sent to the control unit by these blocks were handled via analog and digital ports available on the FPGA. One additional block, the resolver one (mentioned in fig.2 with RES) was created in order to mimic the response of the actual electronics attached to the resolver. It outputs the position of the shaft on digital channels that are then converted by the controller into actual angular position.

On the second FPGA, the control unit of the DT as well as of the actual test-bench, block no. 10 handles the calculation of the load machine's actual current from the reference torque.

$$i_{DCM\_ref} = \frac{T_{DCM\_ref}}{kt_{DCM}} \quad (10)$$

For the calculation of the reference torque for the PMSM function of the actual speed and the reference one, block no. 11 is engaged containing a PI controller that handles this issue.

$$\begin{aligned} T_{PMSM} &= k_p \cdot (n_{PMSM\_ref} - n_{PMSM}) + \\ &+ k_i \cdot (n_{PMSM\_ref} - n_{PMSM}) \end{aligned} \quad (11)$$

The electromechanical conversion is reused in block no. 12 to estimate the values for the DQ components of the back emf is computed.

$$\begin{aligned} e_{sD\_est} &= -(L_{sD} \cdot i_{sD} + \psi_{PM}) \cdot \omega \\ e_{sQ\_est} &= L_{sQ} \cdot i_{sQ} \cdot \omega \end{aligned} \quad (12)$$

The inverse Park transformation of the measured currents, handled in block no. 13 establishes the DQ values of those necessary for the entire control strategy.

$$\begin{aligned} I_{s\alpha} &= I_{As} \\ I_{s\beta} &= (I_{As} + 2 \cdot I_{Bs}) / \sqrt{3} \\ I_{sD} &= -I_{s\alpha} \cdot \sin(\theta) + I_{s\beta} \cdot \cos(\theta) \\ I_{sQ} &= -I_{s\alpha} \cdot \cos(\theta) + I_{s\beta} \cdot \sin(\theta) \end{aligned} \quad (13)$$

Block no. 14 is engaged on calculation of the reference Q current function of the reference torque while the reference D current coming from the strategy block. The latter was imposed to 0 as general control method of PMSMs.

$$i_{sQ\_ref} = \frac{T_{PMSM}}{\frac{3}{2} \cdot p \cdot [\psi_{PM} + (L_{sD} - L_{sQ}) \cdot i_{sD}]} \quad (14)$$

The actual reference values for the DQ voltages are computed in block no.15. Using the measured DQ currents, the estimated DQ back emf voltages and two PI regulators, the computation is accomplished.

$$\begin{aligned}\xi_{i_{QD}} &= i_{s_{QD\_ref}} - i_{s_{QD}} \\ u_{s_{QD}} &= k_{p\_i} \cdot (i_{s_{QD\_ref}} - i_{s_{QD}}) + k_{i\_i} \cdot (i_{s_{QD\_ref}} - i_{s_{QD}}) \quad (15) \\ u_{s_{QD\_est}} &= u_{s_{QD}} + e_{s_{QD\_est}}\end{aligned}$$

The DQ reference voltages need to be inverted using the reverse Park transformation into 3-phase quantities. This issue is handled in block no. 16. The last block, no.17 is in fact the PWM generator. Each of the 3-phase voltages is compared with the PWM carrier set for a certain frequency. The output of the comparison will be 0 or 1 and these values will represent in fact the states of the transistors. These states will be sent from the control unit FPGA to the test-bench simulator FPGA using the digital channels available.

### III. FPGA DESIGN AND TESTING

Generally, the EMR concept was detailed in several papers as being implemented usually in Matlab Simulink or LMS Amesim as offline simulations and in Typhoon HiL real-time environment [10]. To push a step forward, the authors implemented the entire model in 2 FPGAs, one handling the control unit and the other handling the complete test-bench model. The communication between the 2 FPGAs was handled using digital and analog IOs identically as the control unit would be connected to the real test-bench. One hand, by this a more realistic analysis is approached and on the other hand, the transition from controlling the digital twin to control the actual test bench is approached only by disconnecting the FPGA test-bench simulator and connecting the control to the real hardware.

All the mathematical equations that govern the models that were described in eq.1-15 were implemented in fixed point (FXP) representation, necessary for the FPGA compiler to generate the bit-files for each model.

In fig. 3-top, the EMR constructed for the actual test-bench as its digital twin is depicted. For each block created in the concept of the EMR a sub-VI was created. In order to create a more flexible environment, besides the normal input/output signals of each block, several additional ones were added ensuring to the mathematical models inside the blocks different quantities required, such as machine parameters, sampling time for integrators and gains for the regulators. Some connections between few block required feedback nodes, which are mandatory in FPGA programming when one signal is sent backwards, from the output to the input. However, these do not change the behavior of the system, only ensure that proper data is manipulated in the correct way inside the model. In fig. 3 both top and bottom, the digital output and input ports are visible in the control and test-bench simulator loops. However, the analog input/output ports are not visible in fig 2 as these were implemented in separate loops, but the 3-phase currents, the machine speed and position and the currents and voltages of the DCM were sent/received via those communication lines. The PMSM model (fig.3-top) triggers the clock of the control FPGA, as it can be seen in the lower part of fig.3-top. The FPGAs are operating at 5MHz and the data transmission is done at the same speed. However, the ADC IOs are operating at about 1MHz, variable function of how many are engaged in the project. While the data is not refreshed from the IOs, the FPGA, by nature, recycles the last data that was read on an input port.

The data of interest for the authors was gathered and inserted into a FIFO block (first in first out) that ensures loss-less data acquisition and in the same time ensures fast and reliable method of stream information into TDMS files, specific for LabVIEW environment.

When testing the digital twin versus the actual test-bench, the chosen method was to use a reference speed for the PMSM controller and a reference load torque for the DCM.

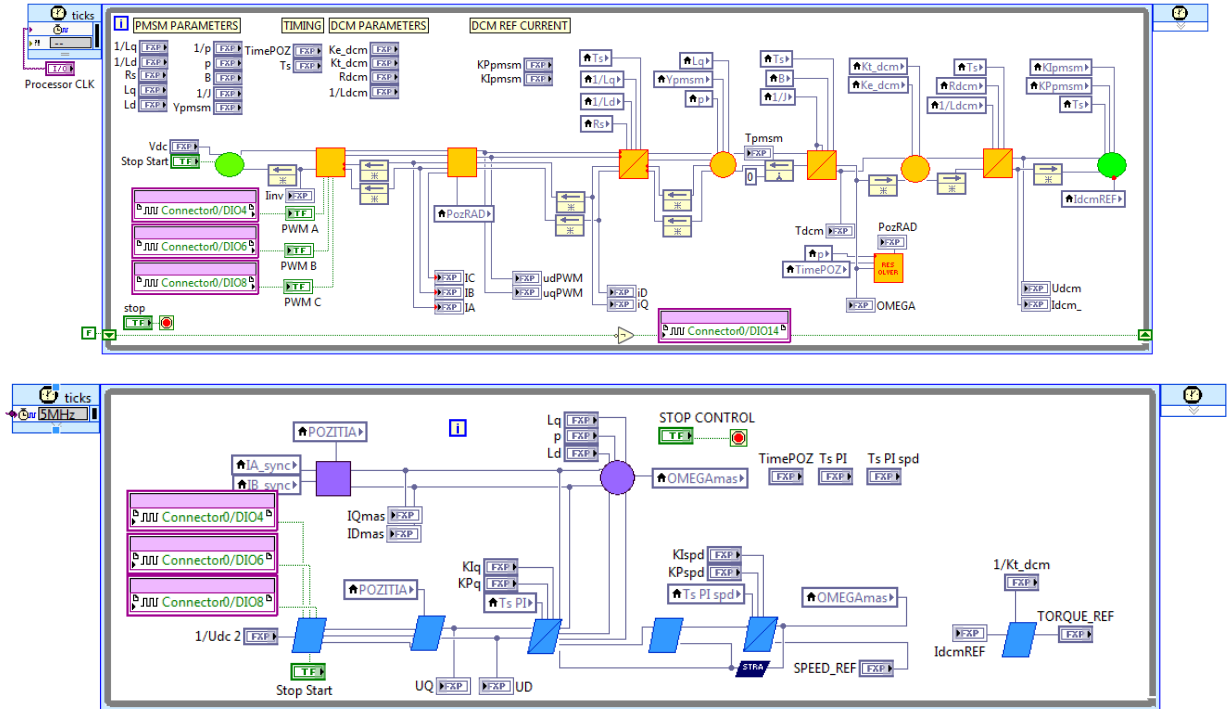


Fig. 3. The FPGA implementation of the EMR representation for the test-bench (top) and control unit (bottom)



The data used for this particular testing was in fact recorder from an actual vehicle for a 20 minutes ride in the urban environment. In order to reach for comparative results, both the digital twin and the actual test-bench were loaded for the same reference torque and speed.

The PMSM as propulsion machine ratings are given in table I. However, a simple calculation can be engaged to compute the gear box ratio in order to decrease the speed of the machine and increase the generated torque to meet the specification of a small scooter as light electric vehicle.

$$\begin{aligned}
 F_e &= c_{roll} \cdot M_{tot} \cdot g + 0.5 \cdot \rho \cdot c_{drag} \cdot (V_{veh})^2 + M_{tot} \cdot g \cdot \alpha \\
 T_{pmsm} &= F_e \cdot R_{whl} \\
 RPM_{whl} &= V_{veh} \cdot 1000 / 60 \cdot (2 \cdot \pi \cdot R_{whl}) \\
 GB &= RPM_{max} / RPM_{whl}
 \end{aligned} \quad (16)$$

In eq.(16) a simple calculation model for sizing the gearbox (GB) ratio is presented as function of the maximal shaft speed ( $RPM_{max}$ ) and actual speed of the wheel ( $RPM_{whl}$ ). The latter is computed by converting the rated vehicle speed ( $V_{veh}$ ) from km/h into rpm, function of the radius of its wheel ( $R_{whl}$ ). Function of the later and the resistive force of the environment ( $F_e$ ), one can compute the required torque of the PMSM. Using this method a GB ratio of 8 was reached.

TABLE II. THE PARAMETERS FOR SIZING THE GEARBOX

Parameter	Description	Value
$c_{roll}$	the rolling resistance coefficient	0.02
$g$	gravitational acceleration	9.81m/s <sup>2</sup>
$c_{drag}$	the drag coefficient	0.4
$M_{tot}$	the total mass	65kg
$\alpha$	the slope angle	0°
$V_{veh}$	the rated vehicle speed	15km/h
$RPM_{max}$	maximum PMSM speed	1500rpm
$R_{whl}$	radius of scooter wheel	0.2m

In all the above calculations the wind speed was neglected as being a variable quantity in such a system.

#### IV. EXPERIMENTAL TESTING AND COMPARATIVE ANALYSIS

As already mentioned, in order to have correct and comparative testing of the results of the actual measurements versus those obtained from the DT, the same speed reference was imposed to the PMSM and the same load torque was imposed to the DCM, in both analysis conditions. Even more, to ensure correct data acquisition, the sampling rate of the data and the sampling speed for its streaming into TDMS files was imposed identical for all the analysis. The main interest was to compare the DQ currents, the speed and the developed torque, the electrical and mechanical powers that finally returns the efficiency and the voltage and the current of the DCM in both cases. It has to be mentioned that with red curves are depicted the quantities related to the DT, with blue curves those measured on the test-bench and with green curves the reference values.

In fig. 4, the reference, the simulated and the measured velocity of the PMSM are depicted. The results are over the time period of 20 min. As can be observed, both the DT and the test-bench measurements agree closely to the imposed reference. In fig 5, the reference, the current's based estimate and the simulated torque characteristics are depicted. It is important to mention here firstly that the measured and simulated torque are in very good agreement, superimposing

quite closely. However, these values are a little larger than the reference value.

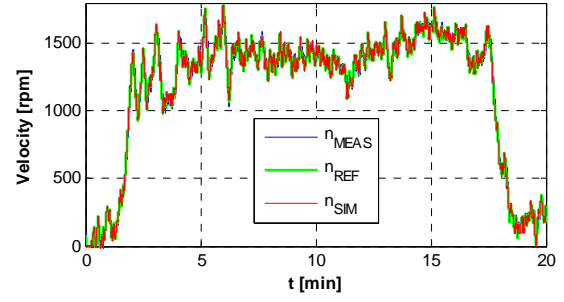


Fig. 4. The reference, simulated and measured velocity of the PMSM

This is normal because in order for the PMSM to ensure the production of torque to meet the reference, it has also to develop a larger quantity of torque to overcome the friction that is present in the bearings of the two machines.

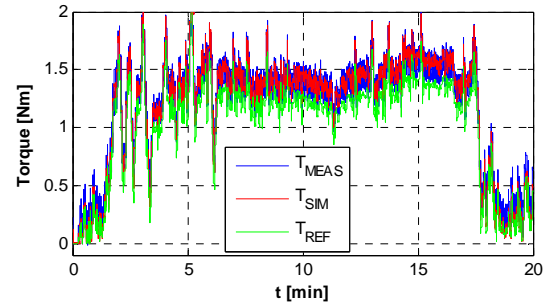


Fig. 5. The reference, simulated and estimated torque of the PMSM

Normally the currents in the machine are reflection of the torque variation. Knowing that the strategy of PMSM control was imposing the D current to 0 up to the rated speed, the torque is produced only by the Q current component. In fig.6 the DQ currents of the DT and those measured are superimposed, proving a very good agreement. The main difference is that the measured ones are polluted with more noise, however these can be minimized by more accurate PI controller tuning.

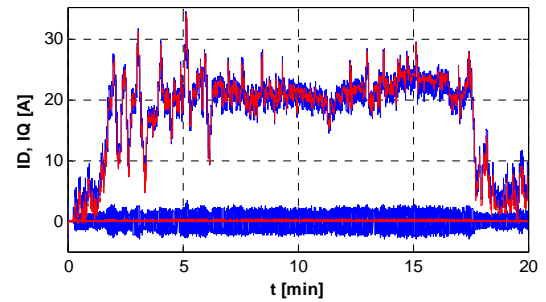


Fig. 6. The DQ currents of the PMSM

In fig. 7, the electrical and mechanical powers of the PMSM are depicted for the DT and those measured ones. The agreement between them is obvious. Larger quantity of measurement noise is present in the measured ones for the same reasons as earlier detailed. As it can be observed the efficiency of the machine is close to 0.8 while it operates close to the rated region. Spikes that go close to 1 are only due to noise in measurements. In order to test the complete behavior of the DT versus the actual test-bench, not only the results of

the PMSM must be valid, but as well as those of the DCM need to reach the same performances.

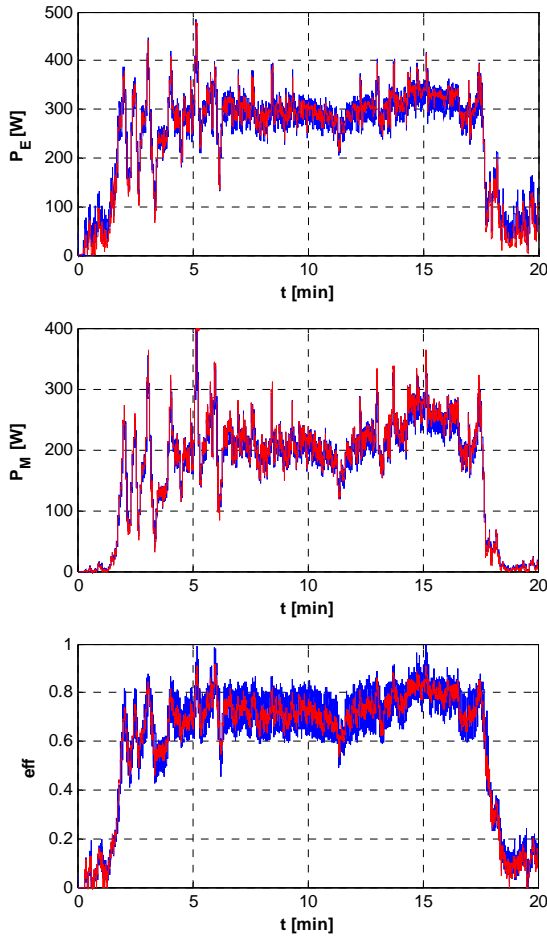


Fig. 7. The electrical (top) and mechanical (middle) powers and the efficiency (bottom) of the PMSM

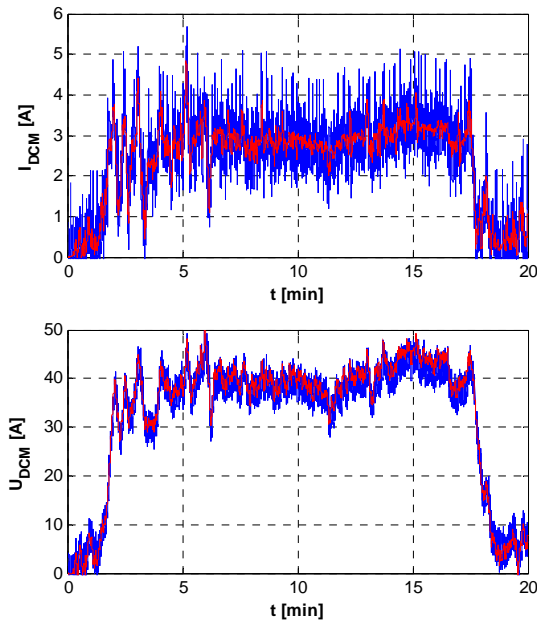


Fig. 8. The current (top) and voltage (bottom) of the DCM

In a comparative analysis observing fig. 8, it can be observed that the current and the voltage of the DCM of the DT and the measured ones are in very good agreement.

## V. CONCLUSIONS

Creating simulation environments that are able to replicate the behavior of the actual test facility is more than a lucrative tool for development engineers. Such tools can be transported anywhere, do not need space, power supply and other additional logistics and more, can safely return correct and reliable information about the future product testing it in any circumstance without damaging risk or other irreversible fault. The paper outlines such an approach, proving that with accurate parameter identification, using real-time processors, such performances can be reached with no doubt. In the same time, transitioning from simulation to actual measurement in such an approach, becomes straight forward and minimizes the time and effort of the researcher. Future investigations will take into consideration the machine core saturation and switch dead-time effect to be included in the simulation program.

## ACKNOWLEDGMENT

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