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# Behavioral Model of Gallium Nitride Normally ON Power HEMT Dedicated to Inverter Simulation and Test of Driving Strategies

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## Keywords

Wide band gap devices, GaN, Behavioral model, Voltage inverter

## Abstract

In this paper, the authors present a behavioral model of a GaN normally ON HEMT. Forward and reverse conductions are modelized. The modelling of both conduction modes is required to provide accurate diode-less synchronous switching-cell simulation. A dedicated transistor capacitance extraction procedure based on an analysis of turn-on and turn-off waveforms is also proposed and experimented.

## Introduction

### Context

Gallium Nitride (GaN) power High Electron Mobility Transistor (HEMT) are considered to replaced middle voltage IGBT in the electric vehicle (EV) and hybrid vehicle (HV). The added values of GaN transistors are mainly lower losses, higher operating temperatures and more compact systems [1], [2]. Because GaN HEMT devices are new power components, accurate models dedicated to power system simulation are strongly needed for designers. Models are also very useful for transient analysis ( $dv/dt$  and  $di/dt$ ), losses prediction, EMI impact evaluation, power topologies comparison or even for test of driving strategies.

A lot of models have been already proposed. In [3] and [4] theoretical studies of GaN-AlGaIn HEMT are proposed, providing complete solid-state analysis. The approach is not enough useful for power electric designer. More recently simple and accurate simulation models for EPC<sup>TM</sup> GaN HEMT have been presented [5], [6]. In both papers, the model parameters are extracted, in a conventional manner, from static  $I$ - $V$  and  $C$ - $V$  characteristics of a normally OFF transistor. Until now, no model has been established to represent the behavior of the transistor in both forward and reverse conduction modes. This type of model is essential for the study of diode-less synchronous switching-cell or inverter operation.

### Method

As explained in [7], the four most essentials waveform needed to model a power device are : 1) output characteristics ( $I_D$  vs  $V_{DS}$  @  $V_{GS}$ ). 2) Transfer characteristics ( $I_D$  vs  $V_{GS}$  @  $V_{DS}$ ). 3) Reverse drain – source characteristics ( $I_D$  vs  $V_{DS}$  @  $V_{GS}$ , 3<sup>rd</sup> quadrant characteristic). 4) Transistor capacitances versus bias voltage ( $C_{GD}$ ,  $C_{GS}$  and  $C_{DS}$ ). For the three static characteristics 1), 2) and 3), a classical parameter extraction procedure is used. Then a dedicated approach for the transistor capacitance parameters extraction obtained from an accurate analysis of turn-on and turn-off waveforms is detailed.

## Device under investigation

The device under investigation is the LETI-M30-200 Normally-ON GaN HEMT. Two identical transistors are involved in the same package to provide a half bridge module [8]. In table I, a summary of the main transistor characteristics is shown. Fig. 1 shows a picture of the die. 50  $\mu\text{m}$  diameter aluminium bondings are used for the power part (drain and source), and three 25  $\mu\text{m}$  diameter gold bondings (Kelvin source, Kelvin drain and gate) are used for the control part. Fig. 2 shows a typical stack for GaN based HEMTs developed at LETI.

**Table I: LETI GaN HEMT Characteristics**

$V_{DS\_MAX}$	$I_{D\_MAX}$	$V_{TH}$	$V_{GS\_MIN}$	$V_{GS\_MAX}$	Active die size	Thickness	Gate type
200V	30A	-3V	-7V	+7V	(1.7x7.3) mm <sup>2</sup>	0.6 mm	Metal Insulator Semiconductor

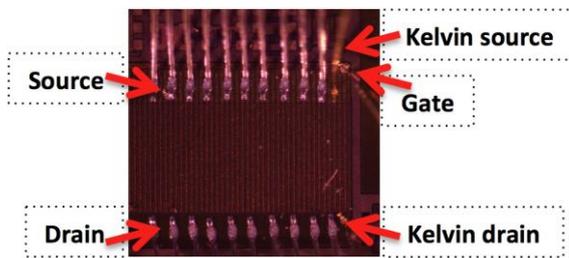


Fig. 1: LETI GaN HEMT photo

Source	Gate	SIN (PECVD) 300°C	Drain
Undoped GaN (3 nm)			
Undoped Al <sub>0.26</sub> GaN <sub>0.74</sub> (4 nm)			
Undoped GaN			
AlN nucleation layer (<50nm)			
Si (p) < 100 ohm.cm			

Fig. 2: Typical stack for GaN-based HEMTs developed at LETI

## Statics results and parameters extraction procedure

### Static characterizations and parameters extraction

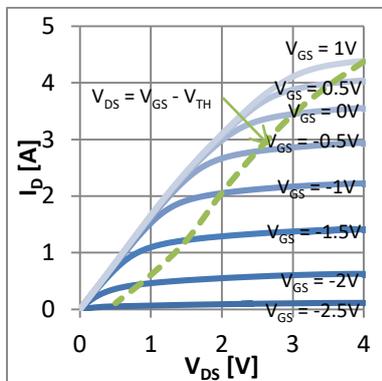


Fig. 3: Output characteristics @Tc = 25°C

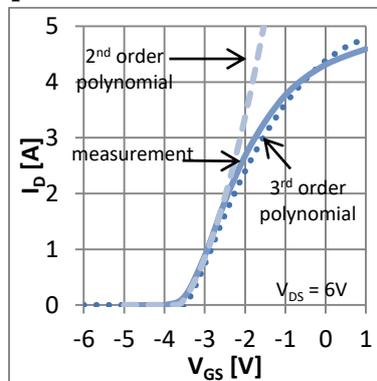


Fig. 4: Transfer characteristic @ $V_{DS}=6V$  and @Tc = 25°C

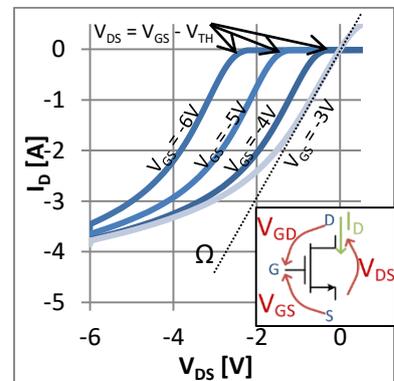


Fig. 5: Reverse drain – source characteristic @Tc = 25°C

Fig. 3 provides the output characteristic: ohmic region ( $V_{DS} < V_{GS} - V_{TH}$ ) and saturation region ( $V_{DS} > V_{GS} - V_{TH}$ ) can be easily identified. The green line marks the boundary between the two regions. Thanks to ohmic region, one can extract  $R_{DS(ON)}$  parameter:  $R_{DS(ON)} = 600m\Omega$  giving a specific resistance  $R_{DS(ON).S(ACTIVE)} = 54m\Omega.cm^2$ . One can note that, in this case, this relatively high value is due to high drain and source contact resistance due to poor metal-semiconductor quality of this first GaN generation.

Fig. 4 shows the transfer characteristic (solid line). One can notice that this curve is not linear. The behavior of the transistor transconductance changes when  $V_{GS} > -1V$ . This is due to the assumption  $V_{DS}$

$\gg V_{GS} - V_{TH}$  is no longer valid, and the transistor is no longer biased in the saturated region. Then, only the first part of the characteristic is representative of a transistor operating in the saturated region. The forward transconductance parameter  $g_{fs}$  can be extracted:  $g_{fs} = 1,43A/V$  in the first area ( $-3V < V_{GS} < -1.5V$ ). Another approach has been also tested: a 2<sup>nd</sup> order polynomial equation is used, because  $I_D$  is a function of  $(V_{GS}-V_{TH})^2$  as much  $V_{DS} > V_{GS} - V_{TH}$ , and its parameters are obtained by using mathematic fitting tools. Fig. 4 also shows the comparison between measurement and simulation results using the 2<sup>nd</sup> order polynomial equation. In order to be more accurate over the entire waveform, in the particular case  $V_{DS}=6V$ , a 3<sup>rd</sup> order polynomial equation may be used.

Finally, the voltage threshold parameter  $V_{TH}$  is extracted from the transfer characteristic. There, the value obtained is  $V_{TH} = -3.3V$ .

Fig. 5 is the reverse drain – source characteristic. One of the main singularities of the GaN HEMT is its reverse conduction capability. Because the GaN HEMT is a lateral and undoped device, no junction parasitic bipolar is present as in the case of MOSFETs [9]. If reverse conduction mode for MOSFET and GaN HEMT seems identical, actually a fundamental difference exists due to the fact that no body-diode is present in the HEMT device.

Whenever the gate-source voltage is lower than the threshold voltage, the MOSFET reverse conduction is due to minority carriers flowing through a body-diode. For the HEMT case, since the channel is in undoped crystal region, there is no minority carriers and so no reverse recovery losses [10]. For the forward conduction mode, the drain current is mainly controlled by  $V_{GS}$  voltage while in the reverse conduction mode this current is controlled by the  $V_{GD}$  voltage. This is a key-point for the HEMT model implementation. Equations (1) to (3) describe the reverse behavior of the GaN HEMT:

$$I_{D\_R} = g_{rs}(V_{GD} - V_{TH}) \quad (1)$$

$$I_{D\_R} = g_{rs}(V_{GS} - V_{DS} - V_{TH}) \quad (2)$$

$$I_{D\_R} = g_{rs}(V_{GS} - V_{TH}) - g_{rs} \cdot V_{DS} \quad (3)$$

$I_{D\_R}$  is the current that flow from the source to the drain (so  $I_{D\_R} > 0A$  in the reverse region) ;  $g_{rs}$  is the reverse transconductance. From the equation (3) one can easily identify two parts: an offset provided by  $g_{rs} \cdot (V_{GS} - V_{TH})$  with  $V_{GS}$  a constant voltage and a slope:  $g_{rs}$ .

On Fig. 5, one can notice 2 separate regions:

1.  $V_{GS} < V_{TH}$ : the load current goes through the source to the drain forcing a  $V_{DS} (< 0V)$  value to the transistor.  $V_{DS}$  will be such that  $V_{GD} > V_{TH}$ . In this region, “high-losses reverse-conduction” mechanisms exist based on the gate – drain transconductance control between  $I_D$  and  $V_{GD}$ . This leads to very important reverse voltage drop due to the offset  $(V_{GS} - V_{TH})$  and then high losses. One can notice also that in this region, each change of gate-source voltage has a direct effect on drain-source voltage.
2.  $V_{GS} > V_{TH}$ : in this region,  $V_{GD} > V_{TH}$  (since  $V_{DS} \leq 0V$ ), the transistor will be bias in the reverse ohmic region. The reverse conduction goes exactly like the forward conduction in the ohmic region. One can notice that a change of gate-source voltage has almost no effect on drain-source voltage.

One can also notice that a reverse saturation of the drain current appear at  $I_D = -3,5A$ . Until now, the authors have no physical explanations of this saturation phenomenon that is not observable with other GaN HEMT, neither on the CEA-LETI 2<sup>nd</sup> generations chips. Theoretically  $V_{GD}$  could increase indefinitely since  $V_{DS}$  is also free to increase indefinitely (under the physical limit of the chip).

## Static model and comparison between measurement and simulation results

**Table II: Static parameters**

$R_{DSON}$	$V_{TH}$	$g_{fs}$	$I_{D\_REVERSE\_SAT}$
600m $\Omega$	-3.3V	1.43A/V	-3.5A

Extracted static parameters are shown in table II. Fig. 6 shows the principle of the proposed GaN HEMT behavioral model. The model is divided in two symmetric modules joined from one side by the gate pin, and from the other side by  $R_{DSON}$  resistor that emulates the channel resistor. Note that this global resistance could be split in two access resistances,  $R_{ACCESS-DRAIN}$  drain side and  $R_{ACCESS-SOURCE}$  source side, in series with one effective channel resistance  $R_{DS-CHANNEL}$ .

One module manages the forward conduction, the other the reverse conduction. The main element of both modules is the ideal voltage-controlled current source. The transconductance of those sources are respectively  $g_{fs}$  and  $g_{rs}$ . Note that:

- If the access resistances are introduced, equivalent forward and reverse gains decrease and become respectively  $g_{fs}/(1+g_{fs}\cdot R_{ACCESS-SOURCE})$  and  $g_{rs}/(1+g_{rs}\cdot R_{ACCESS-DRAIN})$ .
- The turn-on threshold of those sources could also be differentiated in  $V_{THF}$ , for forward source, and  $V_{THR}$  for reverse source.
- All diodes are ideal diodes (for instance,  $V_{DF} = 0V$  when forward biased and no recovery charge). They are used to model the transition between ohmic – saturated region.

The model principle is detailed as following:

### Forward conduction:

If  $V_{GS} > V_{THF}$  and  $V_{GD} < V_{THR}$ , the voltage  $V_1$  is positive and  $V_2 = 0V$ . A current provided by the red-controlled-source flows from the drain to the source through  $D_R$  (blue diode) and  $R_{DSON}$  (the green resistor). So  $V_{DS}$  is given by the equation (4).

If the inequality (5) is true (the current flowing through  $R_{DSON}$  lower than the current supplied by the red source), then the extra current is flowing through  $D_F$  (red diode). So  $D_F$  is turned-on and the transistor works in its ohmic region ( $V_{DS} = V_{RDS}$ ).

Otherwise (current flowing through  $R_{DSON}$  equal to the current supplied by the red source),  $D_F$  is turned-off then  $V_{DS} > V_{RDS}$  and the transistor works in its saturation region.

$$V_{DS} = V_{RDS} + V_{DF} - V_{DR} \quad (4)$$

$$V_{RDS}/R_{DSON} < g_{fs} \cdot V_1 \quad (5)$$

### Reverse conduction:

If  $V_{GS} < V_{THF}$  and  $V_{GD} \geq V_{THR}$ , the voltage  $V_2$  is positive and  $V_1 = 0V$ . A current provided by the blue-controlled-source flows from the source to the drain through  $D_F$  (red diode) and  $R_{DSON}$  (the green resistor). The current is given by equation (3) (in this case,  $I_R = I_{D\_R}$  and  $V_{GTH} = V_{THR}$ ). The transistor is working in high-losses reverse-conduction mode.

Note that, in this mode, the voltage  $V_{GS} - V_{THR}$  is the voltage shift from the origin. This voltage is present across the  $D_R$  diode, which is turned-off. The reverse current flowing through the transistor is set by the blue source and equal to  $I_R$ . Precisely, from (3) and the internal relation of the proposed model (6):

$$V_{DR} = -V_{DS} - R_{DSON} \cdot I_{DR} \quad (6)$$

One can demonstrate that the voltage across  $D_R$  is given by the equation (7).

$$V_{DR} = I_R \left( \frac{1}{g_{rs}} - R_{DSON} \right) - (V_{GS} - V_{GTHR}) \quad (7)$$

Taking into account that in the proposed model:  $g_{rs} = g_{fs} = 1/R_{DSON}$ , the relation (6) can be simplified as follow :

$$V_{DR} = -(V_{GS} - V_{GTHR}) \quad (8)$$

Permitting to explain the two behaviours in reverse operation:

- Case 1:  $V_{GS} < V_{GTHR}$ ,  $V_{DR} > 0$ , giving a diode  $D_R$  off-state. In this case the reverse operation is governed by relation (3) that is physically an active reverse mode.
- Case 2:  $V_{GS} \geq V_{GTHR}$ ,  $V_{DR} = 0$ , giving a diode  $D_R$  on-state. In this case the reverse operation is governed by the relation:  $I_{DR} = -V_{DR}/R_{DSON}$ . That is physically a passive and ohmic mode.

In these two cases equation (9) gives the I-V slope.

$$\frac{dI_D}{dV_{DS}} = 1/R_{DSON} \quad (9)$$

### Ohmic region:

At last, if  $V_{GS} > V_{THF}$  and  $V_{GD} \geq V_{THR}$ , the two voltage-controlled current sources supply the currents,  $I_F$  (from the red source) and  $I_R$  (from the blue source). While the value of the drain current  $I_D$  is between both values  $I_F$  and  $I_R$ , such  $I_R < I_D < I_F$ , both diodes  $D_R$  and  $D_F$  are turned-on. Thus, the extra current is allowed to flowing through the diodes. That lead to  $V_{DS} = R_{DSON} \cdot I_D$ , corresponding to an ohmic region operating point. The transistor could work either in forward or reverse mode depending of  $V_{DS}$  ( $>0V$  or  $<0V$ ).

### Summary

- In forward conduction  $V_{GS} > V_{THF}$  and  $V_{DS} > 0V$  ( $D_R$  always turned-on):
  - For  $I_D < I_F$  (provide by the condition  $V_{RDS}/R_{DSON} < g_{fs} \cdot V_I$ ),  $D_F$  is turned-on and the transistor is working in its ohmic region ( $I_D = V_{DS}/R_{DSON}$ ).
  - For  $V_{DS}$  high enough to provide  $V_{RDS}/R_{DSON} > g_{fs} \cdot V_I$ ,  $D_F$  is turned-off and the transistor is working in the saturated region  $I_D = I_F$ .
- In reverse conduction  $V_{DS} < 0V$  ( $D_F$  always turned-on):
  - As long as  $V_{DR} > 0V$  (high reverse  $V_{DS}$  voltage),  $D_R$  is turned-off and  $I_D = -I_R = -I_{D,R}$  (provided by (3)).
  - When  $V_{DR} = 0V$  (that will be true according to (10)),  $D_R$  is turned-on and the transistor works in its reverse ohmic region ( $I_D = V_{DS}/R_{DSON}$ ). One can note that it is always true if  $V_{THF} \geq V_{THR}$ .

$$V_{GS} \geq V_{THR} \text{ for } \frac{1}{g_{rs}} = R_{DSON} \quad (10)$$

As shown on Fig. 7, measurement points and simulation results are placed on the same graph. As a conclusion, a good modeling of the LETI GaN HEMT static behavior in all bias regions (forward, reverse and ohmic) is obtained.

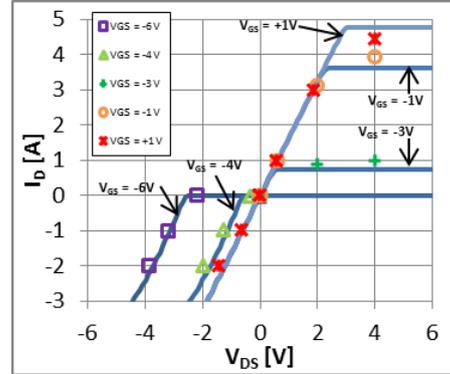
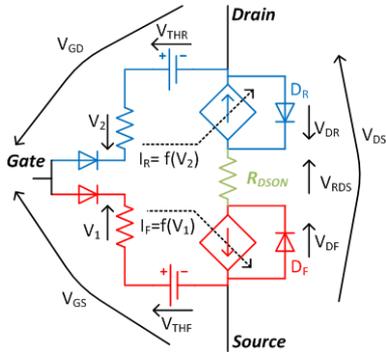


Fig. 6: Proposed circuit model for GaN HEMT

Fig. 7:  $I_D - V_{DS}$  forward and reverse characteristics comparison (blue lines: simulation, points: measurement)

## Dynamics results and extraction procedure

### Instrumentation and methodology

The test circuit is an inverter leg (Fig. 8) where the device under test (DUT) is the low-side. Methodology and instrumentation are the same as reported in [11]. The load is a simple air inductor based on Litz wire used in the well-known double short pulse method that leads to insignificant self-heating of the die. Very important care has been taken in the design of the double layer PCB to obtain a low area for the switching loop and then a low stray inductance on the layout (20nH), for the filtering and decoupling of the switching-cell (film capacitors) and finally by using a low-inductive coaxial shunt (2 GHz bandwidth, 2nH) used to sense the transistor current. Fig. 9 shows a picture of the test bench.

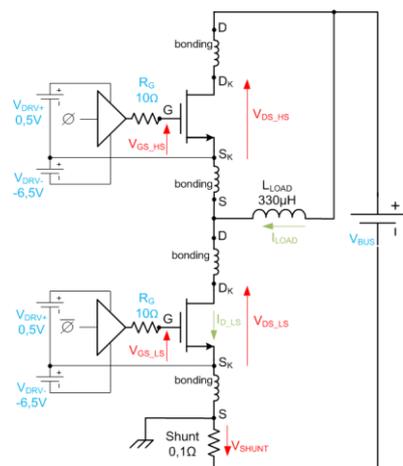


Fig. 8: Test circuit : DUT in an inverter leg topology

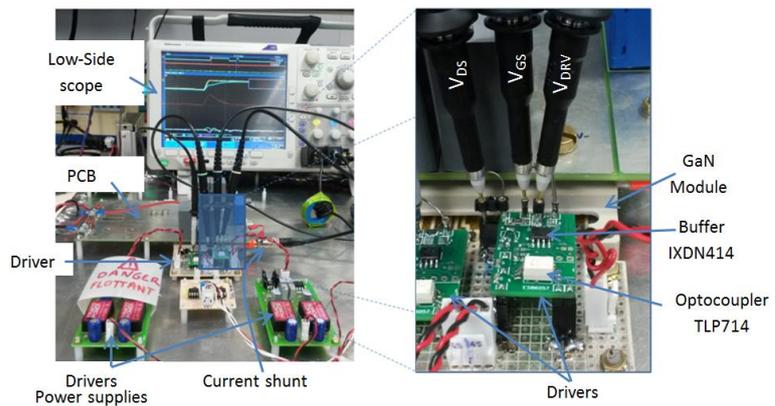


Fig. 9: a) Test bench, b) zoom on the low-side driver

## Transistor capacitances identification process

As it is developed in [9] and [12],  $C_{GD}$  is a low-value and non-linear voltage-dependant capacitance. It is the most significant in HEMT GaN device switching in term of  $dv/dt$  and EMI effect. The model previously described has to be accurate during transient in order to provide to designers a useful simulation component for the analysis of the switchings. Consequently the model has to be as accurate as possible for  $C_{GS}$  and  $C_{GD}$  behavior modeling. At last, a fixed value for  $C_{DS}$  is implemented. This modelling is good enough to provide a very good matching between measurement and simulation.

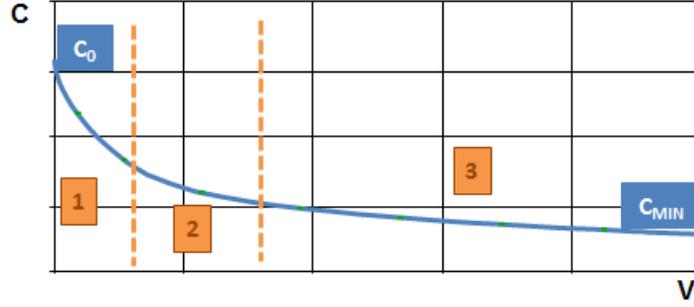


Fig. 10: C-V profile of  $C_{GS}$  and  $C_{GD}$

$$C(V) = C_0 \times \frac{1}{\sqrt{(1+V) \times \left(1 + \frac{k_a [1 + \tanh(k_b \times V - k_c)]}{2}\right)}} \quad (11)$$

In order to model the C-V profile of  $C_{GS}$  and  $C_{GD}$  (Fig. 10), the equation (11) is used (coming from CREE MOSFET SiC CMF20120D PSpice™ model). Fig. 11 is a turn-on oscillogram at  $V_{BUS}=40V$  /  $I_{LOAD}=1.6A$  ; Five steps are identified to extract the C-V values in the three main areas:

- Area 1:  $C_{MAX} - V_{MIN}$
- Area 2:  $C_{INT} - V_{INT}$
- Area 3:  $C_{MIN} - V_{MAX}$

- 1)  $V_{GS}$  increases from  $V_{DRV}$ . (negative driver power supply) to  $V_{TH}$ . In this step,  $V_{DS}$  remains stable ( $\Delta V_{DS} \approx 0V$ ), so  $\Delta V_{GS} = \Delta V_{GD}$ . Equations (12) and (13) provide the link between the capacitor value, the amount of charges and the voltage variations observed in the step 1. From these equations, the extraction of the  $C_{IESS\_1}$  value is possible.  $C_{IESS\_1}$  is the value of the input gate capacitor for  $V_{DRV} < V_{GS} < V_{TH}$  (14).

$$Q_1(t) = \int_0^{t_1} I_G dt \quad (12)$$

$$C_{IESS\_1} = Q_1 / \Delta V_{GS} \quad (13)$$

$$C_{IESS\_1} = C_{GS\_MIN} + C_{GD\_MIN} \quad (14)$$

- 2)  $V_{DS}$  decreases due to  $dI_D/dt$  transient through the bondings. No information on the capacitance values are extracted from this region.
- 3) Steps 3 and 4 are the plateau region due to Miller effect. In these steps,  $V_{GS}$  remains stable ( $\Delta V_{GS} \approx 0V$ ) so only  $V_{DS}$  variations have an effect on  $C_{IESS}$ . From (15) and (16) one can easily

extract  $C_{GD\_MIN}$ . Then, by substituting  $C_{GD\_MIN}$  by its value in equation (14), the value of  $C_{GS\_MIN}$  is deduced.

$$Q_3(t) = \int_{t_2}^{t_3} I_G dt \quad (15)$$

$$C_{GD\_MILLER} = Q_3/\Delta V_{GD} \approx C_{GD\_MIN} \quad (16)$$

4) The step 4 is the end of the plateau region. In this region, one can note the slow decrease of  $V_{DS}$  due to  $C_{GD}$  increasing. From equations (17) and (18), the value of  $C_{GD\_MAX}$  is deduced.

$$Q_4(t) = \int_{t_3}^{t_4} I_G dt \quad (17)$$

$$C_{GD\_MAX} = Q_4/\Delta V_{GD} \quad (18)$$

5) In this final step,  $V_{DS}$  remains constant ( $\Delta V_{DS} \approx 0V$ ) and  $V_{GS}$  increase up to its final value:  $V_{DRV+}$  (positive driver power supply). From equations (19) and (20), one can extract  $C_{IESS\_2}$ .  $C_{IESS\_2}$  is the input gate capacitor value when  $V_{GS}=V_{DRV+}$ . From equation (21) one can deduct  $C_{GS\_MAX}$ .

$$Q_5(t) = \int_{t_4}^{t_5} I_G dt \quad (19)$$

$$C_{IESS\_2} = Q_5/\Delta V_{GS} \quad (20)$$

$$C_{IESS\_2} = C_{GS\_MAX} + C_{GD\_MAX} \quad (21)$$

Finally, the capacitor values in area 2 ( $C_{INT} - V_{INT}$ ) are obtained at  $t_4$  for  $C_{GS}$  and at  $t_3$  for  $C_{GD}$ .

Fig. 12 is a turn-off oscillogram with  $V_{BUS}=40V / I_{LOAD}=1.6A$ . Because  $I_{LOAD}$  value is small enough (less than  $I_{LOAD\_LIMIT}$ ), the turn-off waveforms shown the behaviour of a switching with a transistor in its cuff region. (the channel turned-off when  $V_{GS}<V_{TH}$ ). The  $I_{LOAD\_LIMIT}$  current is the load current value that defines the boundary between turn-off events with or without active channel. It was define by the authors in previous work [11]. Note that capacitances  $C_{OSS\_HIGH-SIDE}$  and  $C_{OSS\_LOW-SIDE}$  can be seen placed dynamically in parallel because  $dV_{COSS\_HIGH-SIDE}/dt = -dV_{COSS\_LOW-SIDE}/dt$ . For this reason, at low load current, the drain current waveform shows a step at  $I_{LOAD}/2$ . Thanks to this analysis, one can extract  $C_{OSS}$ , and so  $C_{DS}$ , taking into account the extraction of  $C_{GD\_MIN}$  (equations (22) and (23)).

$$\left. \frac{dV_{DS}}{dt} \right|_{turn-off\_@\_turned-off\_channel} = \frac{I_{LOAD}}{2 \cdot C_{OSS}} \quad (22)$$

$$C_{OSS} = \frac{I_{LOAD}}{2 \cdot dV_{DS}/dt} = 350pF \quad (23)$$

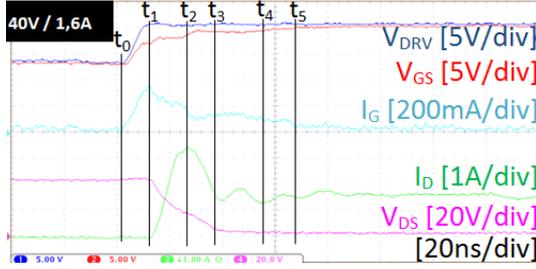


Fig. 11: turn-on transient with  $V_{BUS} = 40V$ ,  $I_{LOAD} = 1.6A$  and  $R_G = 10\Omega$  @  $T_{case} = 25^\circ C$

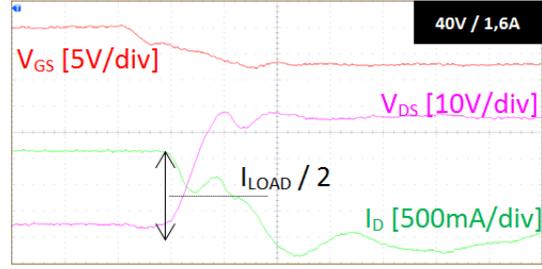


Fig. 12: turn-off transient with a cut-off channel.  $V_{BUS} = 40V$ ,  $I_{LOAD} = 1.6A$  and  $R_G = 10\Omega$  @  $T_{case} = 25^\circ C$ .

### Measurement and simulations results comparison for transient waveforms

The circuit of the Fig. 8 is implemented in a simulation environment using PSpice™ simulator in order to evaluate the dynamic behavior of the model. In table III the most important collected data are listed for three operating points: a)  $V_{BUS} = 40V / I_{LOAD} = 2.4A / R_G = 10\Omega$ ; b)  $V_{BUS} = 30V / I_{LOAD} = 1.6A / R_G = 10\Omega$ ; c)  $V_{BUS} = 40V / I_{LOAD} = 2.4A / R_G = 22\Omega$ . Fig. 13 shows the comparison of the simulation results and the measurements for turn-on and turn-off transients in a) case.

A very good matching between the simulated circuit and measurements is obtained for switching analysis. Indeed, both goals in term of behavior are completed:

1. “the circuit point of view”. The simulation of the current and voltage switching ( $di/dt$  and  $dv/dt$ ) are matching with the measure.  $di/dt$  average error: 16%;  $dv/dt$  average error: 12%.
2. “the driver point of view”. The simulation and the measurement of the gate charge are also matching ( $Q_G$  average error: 7.7%).

Finally, a large error (a factor from 1.5 to 2) on the turned-off energy estimation is obtained. This issue has two origins: in one hand, the fixed implemented  $C_{DS}$  value introduces a time shift; and in the other hand, the negative oscillations of the load current strongly impact the estimation of the switching energy. One can note that, for a greater value of  $I_{LOAD}$ , this issue should be considerably limited.

**Table III: simulation and experimental results comparison for robustness assessment of the proposed model**

	Turn-on			Turn-off	
a) 40V / 2.4A / $R_G = 10\Omega$					
	$dI_D/dt$	$Q_G$	$E_{COM}$	$dV_{DS}/dt$	$E_{COM}$
Measures	0.32 A/ns	7.4 nC	1.6 $\mu J$	3.3 V/ns	1.1 $\mu J$
Simulations	0.31 A/ns	7.2 nC	1.6 $\mu J$	3.2 V/ns	0.6 $\mu J$
b) 30V / 1.6A / $R_G = 10\Omega$					
Measures	0.34 A/ns	7.8 nC	0.6 $\mu J$	2.8 V/ns	0.7 $\mu J$
Simulations	0.29 A/ns	6,8 nC	0.6 $\mu J$	3.1 V/ns	0.3 $\mu J$
c) 40V / 2.4A / $R_G = 22\Omega$					
Measures	0.26A/ns	7.8 nC	2.2 $\mu J$	1.8 V/ns	1.52 $\mu J$
Simulations	0.18 A/ns	7.2 nC	2.6 $\mu J$	2.2 V/ns	1 $\mu J$

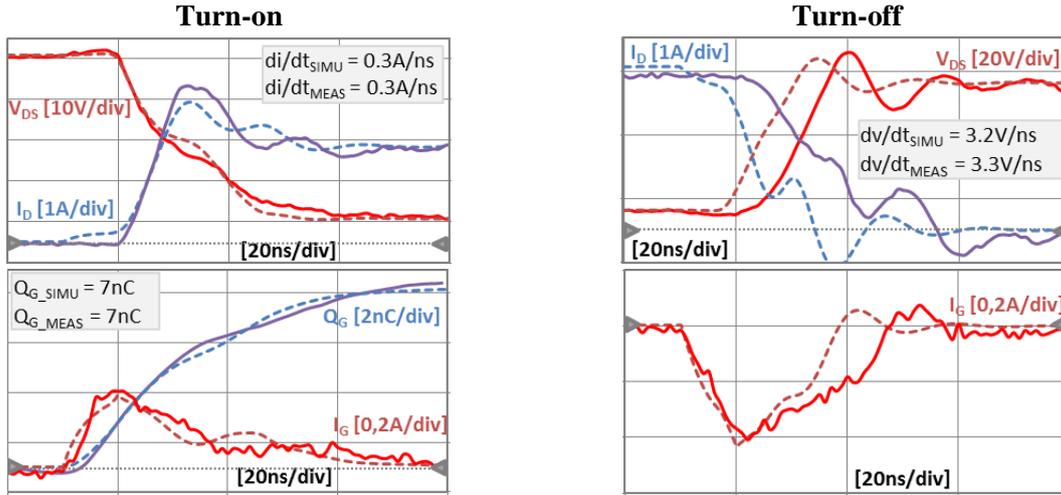


Fig. 13: turn-on and turn off transient comparison between simulation (dashed lines) and measurement (solid lines) at  $V_{BUS} = 40V$  and  $I_{LOAD} = 2.4A$ .

## Conclusion

In this paper, a static and dynamic behavioral model of a power GaN HEMT dedicated to power system simulation is presented. A good understanding of the physical operations of the transistor allows achieving a straightforward behavioral model. Indeed, this model implements few components (two dependant current sources and some diodes, resistors and capacitors). It provides accurate results and requires the extraction of only few parameters. The analysis of  $I$ - $V$  static diagram in forward and reverse conduction modes allows obtaining the statics parameters of the transistor. A good matching between simulation and measurement is obtained both in ohmic and in transconductance controlled mode with  $I_D > 0A$  (quadrant 1) and with  $I_D < 0A$  (quadrant 3). The capacitances ( $C_{GS}$ ,  $C_{GD}$  and  $C_{DS}$ ) are added to the model in order to provide a good dynamic behavior. For accuracy purpose during transients, the implementation of voltage dependent capacitors is needed. An appropriate equation is provided to describe the voltage dependence of the gate–drain capacitor (Miller effect and  $dV_{DS}/dt$  behavior) and the gate–source capacitor (gate charge model and useful for driver design strategy evaluation). At last, a simple voltage-constant capacitor, good enough for the drain–source capacitance representation, is implemented in the model. Then, an accurate analysis of turn-on and turn-off waveforms allows the extraction of capacitor values.

The static elements and voltage-dependant capacitances provide a simple and efficient behavioral model. Thanks to turn-on and turn-off measurements, a comparison between simulations and tests for  $dV_{DS}/dt$ ,  $dI_D/dt$ ,  $Q_G$  (gate charge) and the switching energy is provided. The results obtained validate the relevance of the model.

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