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# *CMOS Gate Driver with fast short circuit protection for SiC MOSFETs*

Yazan Barazi, Nicolas Rouger, Frédéric Richardeau,  
Laplace, University of Toulouse, CNRS, INPT, UPS, Toulouse, France  
2 rue Charles Camichel Toulouse, BP7122 – 31071 Toulouse Cedex 07, France  
barazi@laplace.univ-tlse.fr; rouger@laplace.univ-tlse.fr; frederic.richardeau@laplace.univ-tlse.fr

**Abstract**— This article presents an alternative solution to the short circuit challenges commonly faced by SiC MOSFETs power transistors. In response to this issue, a dedicated fast CMOS active gate driver AGD is designed to detect the short circuits and to protect SiC MOSFETs, using only low voltage analog functions (5V and 40V transistors). The external high voltage diode used in the desaturation monitoring technique is no longer required and the short circuit detection can be much faster based only on signals observed by the gate driver. The IC prototype is based on XFAB XT018 0.18 $\mu$ m CMOS SOI technology. The novel detection circuit is based on a 2D diagnosis, without any time dependency, fully integrated, with a low monitoring voltage. Detection of SC events is between 35ns and 130ns depending on the input capacitance of the power transistor, the internal/external resistors, detection threshold levels and other parameters.

**Keywords**—SiC MOSFET; Active Gate Driver; CMOS; Short-Circuit; Detection and Protection

## I. INTRODUCTION

Silicon Carbide MOSFETs have been used in power converters to improve the efficiency and power density. SiC MOSFETs compared to Silicon IGBTs have better figures of merit, where SiC MOSFETs can have similar conduction losses with much improved switching losses. As the SiC MOSFETs gain maturity and their cost reduces with time, SiC MOSFETs are expected to be adapted and used in more and more applications [1].

The SiC MOSFETs allows higher voltage operations with lower conduction loss, higher switching speed operations with lower switching losses and higher temperature operation capability. In order to ensure these operations, the gate driver should adapt to the specificities of SiC MOSFETs. Essentially, the driving peak current, small propagation delay, high frequency operation, and small power consumption [2]. Another performance feature to be taken into account by the gate driver is the reliability of detection and protection against short circuit (SC) events. Moreover, this detection and protection should be fast since SiC MOSFET short-circuit withstand capability is within  $t_{sc}=2\mu s$  [3], [4] instead of  $t_{sc}=10\mu s$  for Si IGBTs. ( $t_{sc}$  = Short-Circuit Time capability). In addition, the SiC Mosfet has a much lower endurance for repeated short-circuit events than a silicon device. This endurance capability is lower, the longer the short-circuit application time, typically for  $t_{Faulted\_pulse} > T_{sc}/2$ . This is therefore clearly an additional reason to detect and turn-off softly the device with the shortest delay while providing robust detection to switching noise (typically  $t_{detec. delay} \ll t_{sc}/2$ ). Therefore, the SiC MOSFETs gate driver compared to the Si IGBT ones have lesser time to detect the SC and protect the power device and to avoid ageing of the chip.

Recent trends for integrated gate drivers are to integrate a variety of complex functions to address the challenges and to further improve the device performance. One of the main addressed functions, is the SC detection [5]. In the literature, several detection

methods were discussed [6]. The  $v_{ds}$  desaturation monitoring method is classically used for SiC MOSFETs and Si IGBTs [7]. However, this method requires a long blanking time, a high voltage diode, cross talk between power circuit and gate driver, and therefore impossible to integrate within a low voltage CMOS technology. Moreover, this monitoring strategy is not well suited, with MOSFET device, under high current overload operations because of its ohmic on-state greatly dependent of the junction temperature.

In this article, an active gate driver (AGD) is designed to detect the SC and to protect SiC MOSFETs. In order to do so, two original detection approaches are integrated: the occurrence (or not) of the Miller plateau, and the slope differences at the gate voltage, between normal operation and SC events, which offer different solutions and better performances than the prior art. These SC detection techniques are based on low voltage signals available in the gate driver.

## II. SHORT CIRCUIT BEHAVIOR AND TESTBENCH

### A. Studied Short Circuit

First and foremost, it is mandatory to understand the behavior of the power semiconductor device under short circuit, before designing its associated active gate driver. There are two main types of SC, Hard switch fault (HSF) (type I), which is the investigated fault and Fault Under load (type II, not discussed in this article). HSF occurs when the switch turns on with a permanent full bus voltage across itself typically caused by faulted control signals. FUL occurs when the device is already in on-state and an external short-circuit occurs [8]. Here, the fault event will be detected at the low side of a switching cell to further protect the low side power MOSFET during its turn ON.

Fig.1 presents the qualitative switching waveforms of a SiC MOSFET under Normal turn-on (NTO) and Hard Switch Fault (HSF). Briefly, the absence of the Miller plateau, changes on the slopes at the gate-source voltage, changes in the  $dv_{ds}/dt$  and the over-current at the drain are observed under HSF-SC. As it will be presented hereinafter, this distinctive behavior is used to detect and further protect the SiC MOSFET in case of HSF.

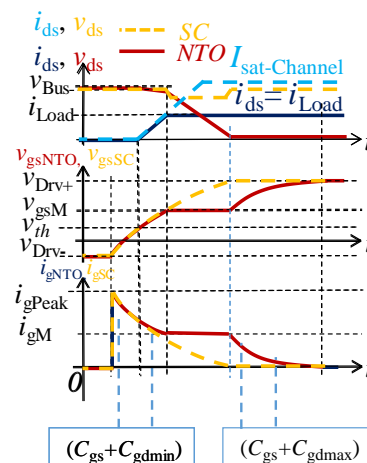


Fig. 1. Characteristics switching waveforms of SiC MOSFET under NTO and SC conditions.

### B. Testbench and pre-study

Real Gate and Drain waveforms are measured (fig.2.) with Wolfspeed’s evaluation-board and are further implemented to design the CMOS analog functions. The CREE evaluation-board includes a half bridge converter, with two C3M 1.2kV SiC MOSFETs, and their respective discrete gate drivers.

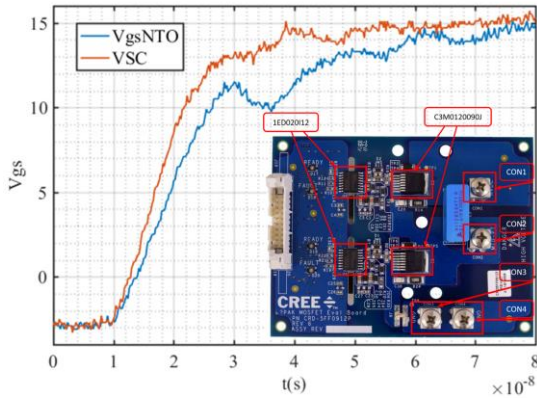


Fig. 2. Experimental waveforms for C3M0120090J device under NTO and SC conditions. Top view of the used evaluation board.

The SiC MOSFETs are driven by  $v_{gs}=-4V/+15V$  and typically operate under  $v_{ds}=900V$   $i_d=22A$  with a  $R_{ds(on)}=120m\Omega$  ( $25^\circ C$ ) and a  $R_{gExt}=8\Omega$ . These SiC MOSFETs are of the highest interest due to their small input capacitances  $C_{iss}=350$  pF. As one can see on fig.2, detecting such SC events only from gate signals is not straight forward. Indeed, the difference between NTO and HSF with SiC MOSFET is small while considering only signals available from the gate driver.

To further design an integrated and fast SC detection, other real Gate and Drain waveforms have been measured as well, using the labs test-bench. The waveforms are WolfSpeed’s second generation SiC MOSFETs, C2M0080120 under  $v_{ds}=600V$ . The device is driven by  $v_{gs}=-5V/20V$  and typically operates under  $v_{ds}=900V$   $i_d=36A$  with a  $R_{ds(on)}=80m\Omega$  and a  $R_{gExt}=10\Omega$ . Contrary to the other device, this power device has a bigger input capacitance  $C_{iss}=1.13$  nF.

## III. THE INTEGRATED CIRCUIT: DESIGN AND LAYOUT

### A. Gate driver

Although the focus of this work is to propose new SC detection techniques, it is important to offer simple solutions to study robustness of the detection techniques with variable parameters. Among the parameters which affect the power switching speed and turn-ON of SiC MOSFET, the main parameters are the input capacitance of the power device, the internal/external resistor [9] or the gate current [10]. In this work, the AGD was adapted to provide variable gate currents, and selectable gate resistors, to further assess the robustness of the detection methods. The CMOS IC is designed using X-Fab XT0.18 SOI technology, which combines the benefit of SOI wafers with Deep Trench Isolation (DTI) and six metal layers 0.18  $\mu m$  process. as well as high voltage transistors up to 200V and high temperature operation. These properties facilitate the design of this IC circuit, to source high current and drive the power transistor with the required gate voltage [11]. fig.3 presents the CMOS IC, which includes several functions.

- A segmented output buffer using 40V-range transistors proposed by the technology, with 10ns and 2ns the respective propagation and propagation mismatch delay. This segmented output buffer allows three source/sink current configurations

(e.g. +/-1.5 A, +/- 3A, +/-4.5A, 25°C), with split PMOS outputs which complementary offers other selectable current values through discrete gate resistors and enable bits (labelled EnP1, EnP2 in fig.3).

- An active Miller Clamp AMC with  $R_{Dson} < 1$  ohm, effectively protecting the device from high  $dv/dt$  changes and safely shut down the power transistor in the case of negative power supply is removed.
- Last and not least, two short circuit detection approaches and protection functions. These functions will be developed in the section below.

### B. Detection and Protection Circuit

The two SC detection approaches that are included in the IC circuit are based on the derivation method. The first approach is the dip approach, where the presence or non-presence of the Miller plateau is detected. The second one is the slope approach, based on the differences between the slope before and after the Miller plateau under NTO; or the unchanged slope under SC.

Once the SC has been detected, the protection circuit is similar to the literature (Soft Shut Down – SSD), where a larger resistance is used to discharge smoothly the gate of the power device. The  $R_{ds(on)}$  of the integrated SSD is around 100 ohms, assuring a soft shut down (small size transistor within the IC). Once the SC has been detected, the segmented buffer goes to a high impedance state HZ (HZ+ signal in fig 3.), where the gate of the power device becomes floating (PMOS and NMOS in output buffer are in OFF state).

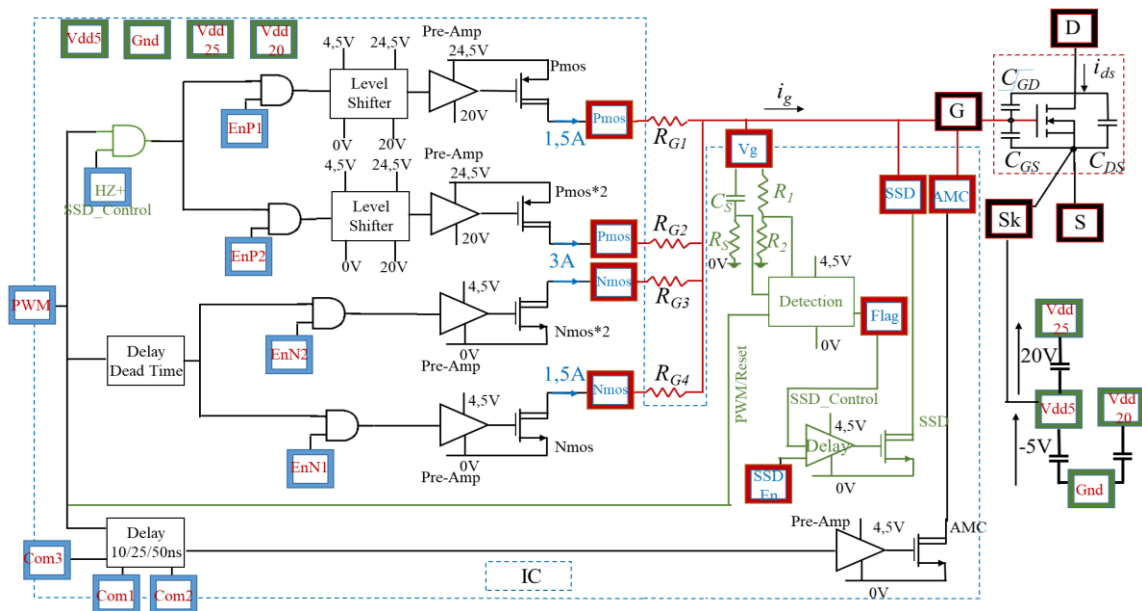


Fig. 3. IC schematic including all the integrated functions

This additional state is typically not available in standard output buffers and gate drivers. However, it is required to turn off the output PMOS in the gate driver, to bypass the incoming PWM signal, and to prevent a short circuit flowing through the output PMOS and the SSD NMOS transistor. After a short delay time to confirm the turn OFF of the PMOS in the output buffer, the SSD is activated. In our IC prototype, the detection FLAG is sent to the centralized control to take further actions, and the SC detection+protection is done at each PWM pulse. In other words, the HZ+ is reset once the next PWM pulse is sent.

### C. View of the IC

The layout of the whole ASIC is divided in two main parts. The Active Gate Driver is  $2414\mu\text{m} \times 1559\mu\text{m}$ , including decoupling capacitors. The detection block for both detection techniques has a surface of  $200\mu\text{m} \times 150\mu\text{m}$ , and the SSD has a surface of  $80\mu\text{m} \times 30\mu\text{m}$ . Fig.4 presents a microscopic zoom view of the chip. The IC is packaged in a QFN40 6mmx6mm.

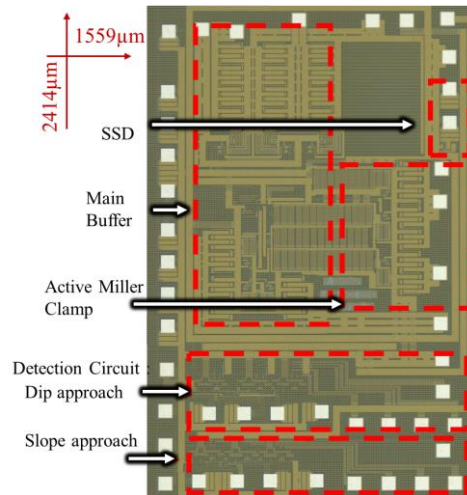


Fig. 4. Microscopic view of the IC.

### IV. VALIDATION OF THE PROPOSED DETECTION CIRCUIT

The derivation monitoring method is based on a sensing capacitor and a resistor. The dip detection schematic is proposed in Fig.5. Experimental waveforms, for both power transistors, were imported in Cadence to design and validate this method, associated with models provided by the CMOS foundry (XFAB XT018 180nm). Fig.6 presents the proposed derivation method with C3M power devices, based on the presence or non-presence of the Miller plateau. This plateau is translated as a dip as shown in the  $dv_{gs}/dt$  signal under NTO. The detection occurs at the arrival of this dip, distinguished by the  $dv_{ref}/dt$ , and activated when  $v_{gs}$  rises above  $v_{gsRef}$ . In the same figure, a visible difference at the projection of the slopes from  $v_{gs}$  to  $dv_{gs}/dt$ .

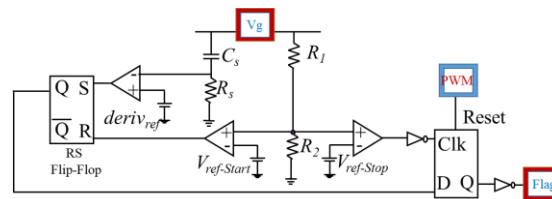


Fig. 5. Detection schematic based on the dip approach.

Fig.7-8 shows the AGD under simulation. Note that the experimental  $dv_{gs}/dt$  is presented in the figures to illustrate the behavior and used as input signal into Cadence.  $v_{gs}$  and the flags are simulated waveforms. The protection time is 50ns and 100ns respective to C3M and C2M.

Fig.7 shows a detection time of 20ns, and a delay time behavior for the C3M power device of 30ns. For fast detection and original methods reference [12], [13] are proposed. Yet for the C2M power device under different condition ( $R_{gExt}=10\Omega$ ,  $v_{gs}=-5V/20V$ ), shows a detection time longer than the previous figure 75ns plus the delay time behavior of 25ns, Fig.8. The difference is

due to several parameters: the applied gate to source voltages  $v_{gs}$  and the input capacitance of the devices  $C_{iss-C3M} = 350 \text{ pF} < C_{iss-C2M} = 1130 \text{ pF}$ . The detection circuit has a surface of  $150\mu\text{m} \times 200\mu\text{m}$ , with a typical DC consumption of  $1.52 \text{ mW}$  (or  $0.34 \text{ mA}$  at  $4.5\text{V}$ ,  $25^\circ\text{C}$ ).

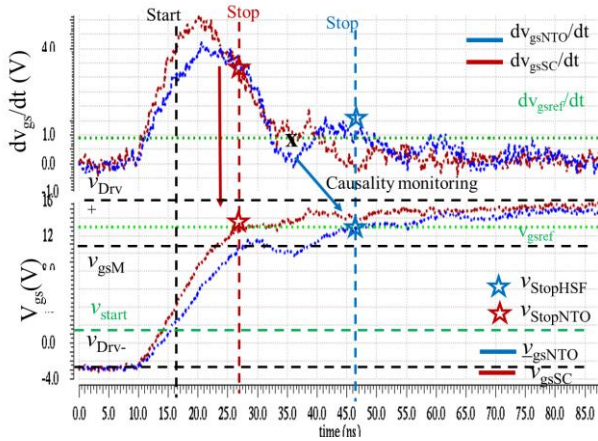


Fig. 6.  $dv_{gs}/dt$  characteristics under NTO and SC HSF, dip detection approach. Experimental waveforms further implemented in Cadence.

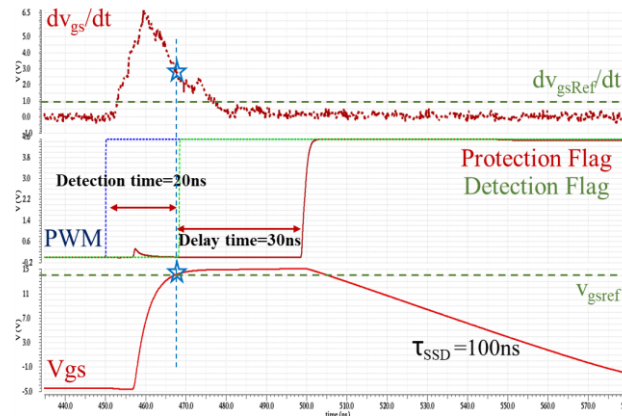


Fig. 7. Simulated waveforms on Cadence of the device under soft protection using experimental C3M0120090  $V_{GS}$  &  $V_{DS}$  waveforms .

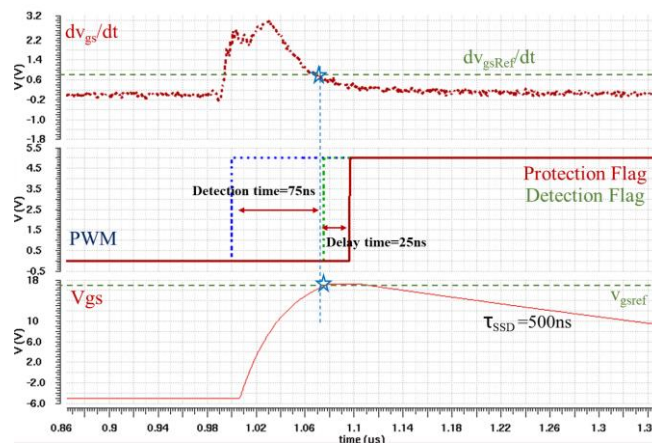


Fig. 8. Simulated waveforms on Cadence of the device under soft protection using experimental C2M0080120  $V_{GS}$  &  $V_{DS}$  waveforms.

The detection time presented in fig.7-8 is the time for  $v_{gs}$  to reach  $v_{gs-Ref}$  and to detect if  $dv_{gs}/dt$  is above or below the reference level. C3M and C2M have different input capacitances therefore different slope speed. The delay time presented in the figures is the time to process the detection flag, to activate the high impedance state of the output buffer, plus an additional delay before activating the SSD.

#### CONCLUSION

A fast and fully integrated method was proposed to detect and protect Hard Switch Fault type short circuit events for SiC MOSFETs. With our techniques, the detection times are reduced to less than 100ns, and external components such as high voltage diodes are no longer required. Experiments are ongoing to assess the robustness of our active gate driver and the integrated protection techniques. High safety and improved endurance short-mode capability could thus be achieved with these two proposed ultra-fast detection concepts.

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