Modeling and Design of High Bandwidth Feedback Loop for dv/dt Control in CMOS AGD for GaN

Plinio Bau, Marc Cousineau, Bernardo Cougo, Frédéric Richardeau, Nicolas C. Rouger

Modelling and Design of High Bandwidth Feedback Loop of CMOS for GaN HEMT dv/dt Control

Plinio Bau[1,2], Marc Cousineau[1], Bernardo Cougo[2], Frederic Richardeau[1], Nicolas Rouger[1]
[1]LAPLACE, Université de Toulouse, CNRS, Toulouse, France
[2]Institute of Technology Antoine de Saint Exupéry
Email: plinio.bau@irt-saintexupery.com nicolas.rouger@laplace.univ-tlse.fr

***Abstract*—The objective of this work is to show the intrinsic limitations of a CMOS technology for the realization of an Active Gate Driver (AGD) with active *dv/dt* control loop. Due to a theoretical study using first order models of CMOS submicron transistors, the main equations providing the link between feedback loop bandwidth and specific technology parameters are obtained. This optimization study allows us to determine the theoretical limits in terms of bandwidth and silicon area. Then, it becomes possible to determine the most appropriate switching control method to implement depending on the application requirements (high efficiency, low EMI), i.e. active feedback with adjustable gain, while ensuring suitable time delays. A feedback loop bandwidth of 1.59 GHz using an 1pF integrated capacitor to address a switching speed of 175 V/ns is demonstrated. Experimental results and simulations using accurate technology models confirms the theory.**

Keywords—Active gate driver, GaN, switching analysis, dv/dt, EMI, power electronics, ASIC for power IC.

I. INTRODUCTION

Switching times of wide bandgap power transistors are extremely high (hundreds of V/ns for 600V GaN or 1.2kV SiC MOSFET) [1]. Therefore, practical useful guidelines are provided to the designer to determine the best trade-off in terms of integrated high voltage capacitive *dv/dt* sensor (C_S), current mirror gain and PMOS/NMOS transistors sizes in order to design an integrated *dv/dt* control system [2]-[4]. Systematic comparison between theoretical predictions and CADENCE™ simulation/layout use-case designs are investigated to demonstrate the validity of the approach. Experimental results confirm the theoretical study allowing the design of sub nanosecond response systems. At last, it becomes possible to determine the most appropriate technology to implement the AGD controlling high *dv/dt* of wide-bandgap transistors.

II. DV/DT CONTROL FEEDBACK LOOP

Fig. 1 shows the transistor level schematics of the proposed CMOS AGD. As already demonstrated in [2] from the same authors, the *dv/dt* can be controlled by changing the value of the gain. The gain is made by the width ratios of transistors involved in a PMOS and a NMOS current mirrors. By increasing this gain, the *dv/dt* of a power device can be reduced independently from the *di/dt*.

The main idea of this method is to sink a current from the gate node during the turn-on event. Therefore, a virtual capacitor is emulated, only during the *dv/dt* phase, between the gate and drain nodes of the WBG power device. One should note that this gain *G* results from the association of a first and second current mirror stages, respectively made of PMOS and NMOS transistors, obtaining $G = G_P \times G_N$. Neglecting the load current effect and some other second order physical phenomena, the *dv/dt* can be expressed by (1):

$$\frac{dv_{DS}}{dt} = -\frac{v_{DRV} - v_M}{R_G C_{rss}} + \frac{i_{FB}}{C_{rss}} = -\frac{v_{DRV} - v_M}{R_G (C_{rss} + G C_S)} \qquad (1)$$

where v_{DRV} is the power supply voltage of the driver and v_M is the Miller plateau voltage.

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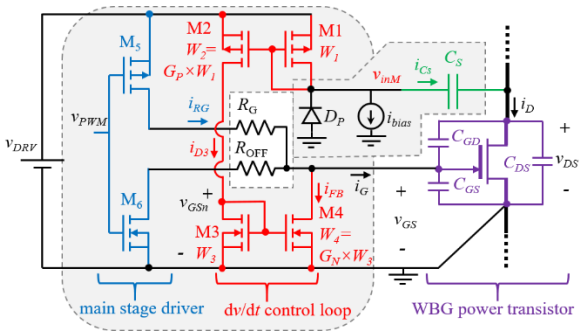

Fig. 1. Schematic of the AGD to control turn-on dv/dt values.

This work shows a step-by-step analytical analysis aimed to optimize the parameters of the circuit shown in Fig. 1, circuit previously presented in details in [2].

TABLE I

THEORETICAL EXPECTED *DV/DT* ATTENUATION

Attenuation factor (A_{tt})	***dv/dt* attenuation**	***GCS/ Crss***	***GCS*** (C_{rss}=2pF)	***G*** (C_S=1pF)
1	0%	0	0	0
4/3	*25%*	*1/3*	*0.6pF*	*0.3*
2	*50%*	*1*	*2pF*	*2*
4	*75%*	*3*	*6pF*	*3*

$$A_{tt} = \frac{dv_{DS}}{dt}\bigg|_{OL} \Big/ \frac{dv_{DS}}{dt}\bigg|_{CL} = 1 + \frac{GC_S}{C_{rss}} \qquad (2)$$

where $dv_{DS}/dt|_{OL}$ and $dv_{DS}/dt|_{CL}$ and are respectively the open-loop and closed-loop v_{DS} variations and C_{rss} represents the gate-to-drain capacitor during the Miller plateau.

Table I shows the value of the product *GCs* to consider for a given expected *dv/dt* attenuation A_{tt} for the GaN power device GS66508T (C_{rss}=2pF). Choosing an attenuation A_{tt} (for example 50% from 175V/ns to 87.5V/ns) the best distribution between the values of G and C_S has to be determined, both in terms of feedback loop bandwidth and silicon area. Next chapters present optimization studies for a given constant GC_S, related to a specific application (GC_S=10pF, $dv_{DS}/dt|_{CL}$ =80V/ns).

A. Feedback loop circuit model

Fig. 2(a) shows the feedback loop circuit used to control dv_{DS}/dt considering the intrinsic capacitances C_{GSp} and C_{GSn} of the PMOS and NMOS transistors. Fig. 2(b) provides a representation of the circuit layout showing the silicon area required for the transistors M1 to M4. The case with G_P=2 and G_N=2 for the gains of the two current mirrors M1-M2 and M3-M4 is illustrated.

An elementary size for the transistor M1 has to be chosen. This size depends both on the input current i_{Cs} provides by the sensing capacitor C_S and the minimum value of v_{inM} that can be tolerated. It can be noticed that M2, M3 and M4 sizes depends on M1. A minimum size for M1 has to be computed in order to reduce the overall surface of the circuit.

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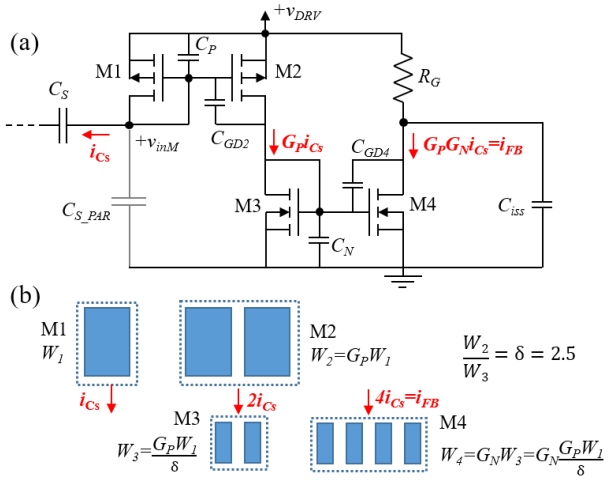

Fig. 2. (a) Two-stage current mirror with its parasitic capacitances, (b) Circuit layout assuming a area factor of 2.5 between NMOS and PMOS transistors (G_P=2 and G_N=2).

B. Sizing M1

Fig. 3 shows the characteristics of a diode-connected PMOS transistor. Due to short channel effect observed in submicron CMOS technologies, two different operating zones may be distinguished, a low current and a high current zones. Therefore, the classic square law has to be linearized for using the transistor at high current level, the well-known square law is no longer valid and a direct proportionality between drain current and gate-to-source voltage has to be considered. With parametric simulations, at v_{GS} constant, it is observed a constant current per width ratio in a wide range of values for W1. Considering the length L of the transistor channel minimum, this constant i_D/W ratio is very useful to make the link between the size of the capacitor Cs in one hand, and in the other hand the resulting size of the mirrors.

The transistor M1 will operate at the operating points 1, 2 and 3 indicated in Fig. 3. At the beginning, when no switching event occurs, i_D=0. At first, slightly before a turn-on order, a pre-biasing current i_{bias} (see Fig. 1) of about 50 µA is generated biasing M1 at the point 1. Then, when a switching event occurs, the transistor M1 reaches the point 2 during a short transient less than 1ns. Just after a short delay, the feedback loop acts to reduce dv_{DS}/dt, the current i_{Cs} decreases and M1 reaches the point 3. Then, it remains on this biasing point 3 for the rest of the switching, assuming a perfect trapezoidal v_{DS} waveform. If v_{DS} is not perfectly trapezoidal, W1 will still operate between points 1 and 3.

Fig. 3 also shows that the temporary operating point 2 should not exceed the maximum voltage v_{DVR}+0,6V otherwise the protection diode D_P may conduct and clamp the voltage to -0,6V. The minimum width of M1 is calculated to place point 3 at $v_{GS\_CL}=v_{DRV}/2$ and it is verified that point 2 will operate under safe operation area. Finally, the expression W1, the width of M1 is:

$$W_{1MIN} = \frac{i_{D\_CL} L_{MIN}}{g_{mP}(v_{GS\_CL} - v'_{TH})} \qquad (3)$$

where L_{MIN} is the minimum transistor length possible of the technology to withstand 5V, 500 nm in our case, and v'_{TH} is the effective threshold voltage of the linear model shown in Fig. 3 around 1.5V. μ_{Peff} is the effective mobility of the PMOS transistor at high current (in the linear zone).

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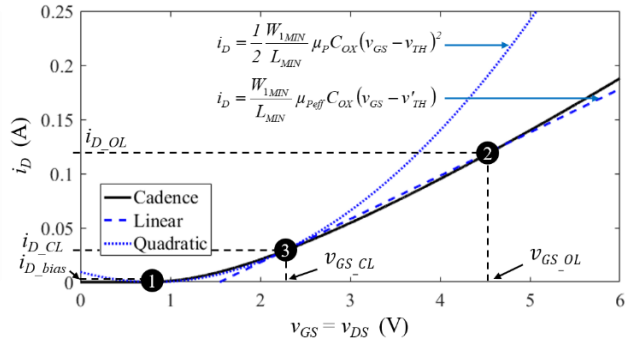

Fig. 3. Diode-connected transistor PMOS characteristic and 1st order model parameter extraction.

C. Sizing W_3 as a function of W_2

The transistor M2 is a multiple of M1 depending the gain G_P of the 1st-stage current mirror. Now, sizing M3 to operate at $v_{DS3}=V_{DRV}/2$ will make M2 always operate in its saturation region. Then, to guarantee the appropriate biasing of M3, the ratio between W2 and W3 has to be equal to the ratio δ of the effective mobility of the PMOS and NMOS transistors. In our case, a ratio equal to 2.5 is obtained.

$$W_3 = \frac{W_2}{\delta} \text{ with } \delta = \frac{\mu_{effN}}{\mu_{effP}} \qquad (4)$$

III. Bandwidth Analysis

One expression for bandwidth as a function of gain or C_S in order to address very fast transient response, with a constant factor GC_S imposed by the application, the bandwidth of the feedback loop has to be determined. Its value may depend on the gains G_P and G_N and on the value of the capacitor C_S. The total intrinsic capacitances at the gate of the PMOS and NMOS current mirrors are respectively given by (5) and (6).

$$\begin{aligned} C_P &= (1+G_P)C_{GSp} + G_P C_{GDp}(1-a_{v\_p}) + C_{DSp} + C_{S\_PAR} \\ C_P &\cong (1+G_P)C_{GSp} + C_{S\_PAR} \end{aligned} \qquad (5)$$

$$\begin{aligned} C_N &= (1+G_N)G_P C_{GSn} + G_N G_P C_{GDn}(1-a_{v\_n}) + G_P C_{DSn} + G_P C_{DSp} \\ C_N &\cong (1+G_N)G_P C_{GSn} + G_P C_{DSp} \end{aligned} \qquad (6)$$

where a_{v_p} and a_{v_n} are the small signal voltage gains of the common-source stage made by M2 and M4 respectively, both close to one, and C_{GS}, C_{GD} and C_{DS}, are the intrinsic capacitors of the transistors.

The expressions of the total capacitances C_P and C_N shown by the gate nodes of the PMOS and NMOS transistors can be drastically simplified.

To calculate the bandwidth, knowing the capacitances of the circuit, the associated dynamic impedances have to be computed. Mainly, the impedances seen at the gate nodes are provided by the diode-connected transistors M1 and M3. Their values are related to the transconductances g_m. The time constants τ can be written as follow:

$$\tau_P = \frac{C_P}{g_{m1}}; \tau_N = \frac{C_N}{g_{DS2} + g_{m3}} \qquad (7)$$

where g_{m1} and g_{m3} are M1 and M3 transconductances and g_{DS2} is the drain-to-source admittance of M2.

Then, the cutoff frequency for the PMOS and NMOS current mirrors respectively are expressed by:

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$$f_{cP} = \frac{1}{2\pi\tau_P}; f_{cN} = \frac{1}{2\pi\tau_N} \qquad (8)$$

The expression of the transition frequency f_T for the NMOS transistors, which indicates the maximum bandwidth that can be reached with a given technology, is provided below:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \qquad (9)$$

Indeed, increasing W increases both g_m and the intrinsic capacitor values. Then, the cutoff frequency of the current mirrors can be related to this transition frequency. Because M1 and M3 are diode-connected transistors, they always work in their saturation region where C_{GD} can be neglected comparing to C_{GS}. Now, neglecting the contributions of C_{S_PAR} and C_{DSp} in Eq. (5) and (6), one can estimate:

$$f_{cN} \approx \frac{f_T}{1+G_N} = f_{cN\_est} \qquad (10)$$

$$f_{cP} \approx \frac{1}{\delta}\frac{f_T}{1+G_P} = f_{cP\_est} \qquad (11)$$

Fig. 5 shows a good correlation between simulated points in CADENCE™ and the estimation expressed by Eq. (10).

A. *Gain G distribution between G_P and G_N*

Depending on the distribution of the gain G among the two current mirror gains G_P and G_N, the overall feedback-loop bandwidth f_c changes. An optimal distribution can be identified. So, an expression of the bandwidth using a geometrical averaging of the two time constants is proposed:

$$1/f_{c\_est} = \sqrt{1/f_{cN\_est}^{\,2} + 1/f_{cP\_est}^{\,2}} \qquad (12)$$

Fig. 4 shows the optimal choice of G_P depending on the value of G. Note the higher G, the lower the bandwidth.

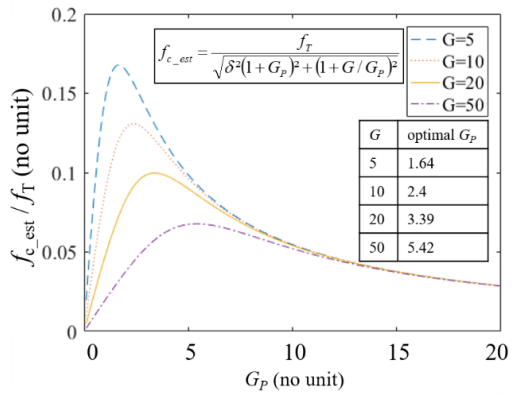

Fig. 4. Normalized cutoff frequency of the feedback-loop as a function of the PMOS mirror gain G_P for several values of G.

B. *Distribution between G and C_S*

For a targeted attenuation of dv_{DS}/dt, the product GC_S is imposed. Now, an optimal distribution of values between the gain G and the capacitor C_S, has to be determined to maximize the feedback loop bandwidth f_c. Indeed, the higher C_S, the lower G but the current i_{CS} increases and the transistor size accordingly.

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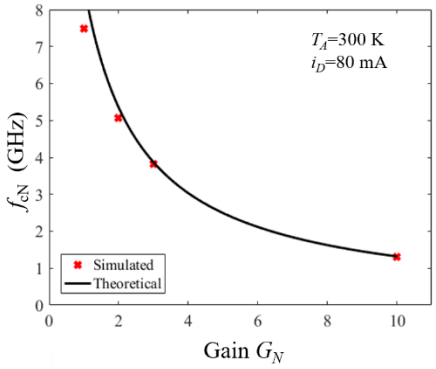

Fig. 5. Bandwidth of one NMOS current mirror as a function of its gain.

To compute accurately f_c, all the intrinsic capacitances present in Eq. (5) and (6) are taken into account. Fig. 6 shows the Matlab™ computations using the appropriate technology parameters with GC_S equals to 10pF. Simulation results using C_S= 100fF, 1pF and 10pF confirm the theoretical projections.

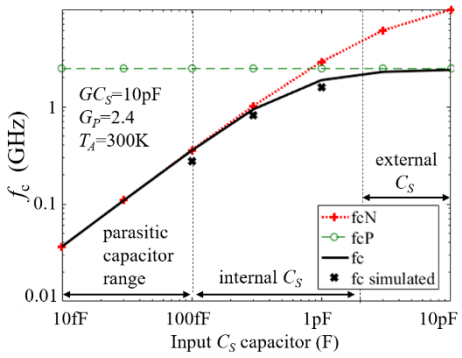

Fig. 6. Feedback-loop bandwidth as a function of C_S for a constant GC_S = 10pF.

IV. Surface Analysis

Now, considering a given product GC_S constant, the separate values of G and C_S have an impact on the silicon area required. The surface S_{Mp} and S_{Mp} of the PMOS and NMOS current mirrors can be expressed respectively by:

$$S_{Mp} = (1+G_P)\alpha L_{MIN} W_{1MIN} \qquad (13)$$

$$S_{Mn} = G_P(1+G_N)\alpha L_{MIN} W_{3MIN} = (G_P+G)\frac{\alpha}{\delta} L_{MIN} W_{1MIN} \qquad (14)$$

where α is the swell factor, i.e. the ratio between the active areas and the actual total area required by the transistors.

It should be noted that W_{1MIN} is a function of the size of C_S due to the increase of the current $i_{D(CL)}$ when C_S increase. According to Eq. (3) it is possible to write:

$$W_{1MIN}(C_S) = \frac{2L_{MIN}}{\mu_{Peff} C_{OX} (V_{GS\_CL} - V'_{TH})} \frac{dv_{DS}}{dt}\bigg|_{CL} C_S; \qquad W_{1MIN}(C_S) = \frac{1}{J_P L_{MIN}} \frac{dv_{DS}}{dt}\bigg|_{CL} C_S \qquad (15)$$

where J_P is the current density of M1 linked to the choice of v_{GS_CL} (see Fig. 3).

The total silicon area S_{tot} required for the proposed circuit is the surface of both current mirrors plus the in-chip high-voltage capacitor C_S surface. Its expression is the following:

$$S_{tot}(C_S)=\left(\left(1+G_P\right)+G_P\left(1+\frac{G}{G_P}\right)\frac{1}{\delta}\right)\alpha L_{MIN}W_{1MIN}(C_S)+\frac{C_S}{C_S'} \quad (16)$$

$$S_{tot}(C_S)=\frac{1}{\delta}\frac{\alpha}{J_P}\frac{dv_{DS}}{dt}\bigg|_{CL}(A_{tt}-1)C_{rss}+\left(\left(1+G_P(1+\frac{1}{\delta})\right)\frac{\alpha}{J_P}\frac{dv_{DS}}{dt}\bigg|_{CL}+\frac{1}{C_S'}\right)C_S \quad (17)$$

where C_{rss} is the GaN power device reverse transfer capacitance, C_S' is the capacitance per surface unit in the CMOS technology between the metal layers 4 to 6.

Eq. (17) has a minimum value is achieved for low values of C_S. Fig. 7 shows the surface S_{tot} versus C_S for a constant GC_S product. S_{tot} increase proportionally with C_S at high C_S values.

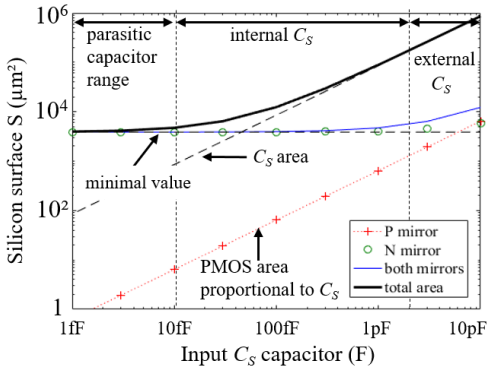

Fig. 7. Silicon surface as a function of the input sensing capacitor C_S for a constant attenuation product GC_S=10pF.

V. Experimental Results

In order to achieve the best bandwidth a higher value of C_S is chosen even if it will consume more surface. It can be seen in Fig. 5 the bandwidth is inversely proportional to the gain.

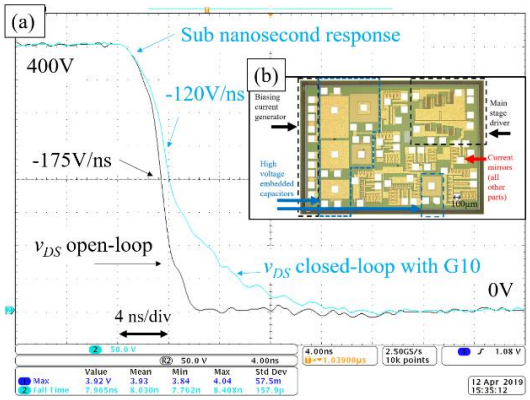

Fig. 8. (a) Experimental waveforms of AGD controlling *dv/dt* from 175V/ns to 120V/ns with in-chip HV capacitor of 1pF (b) microscope picture of the ASIC AGD

Fig. 8 (b) is the AGD designed with the high voltage in-chip capacitors. Attenuation factor of 1.45 (A_{tt}=175/120 V/ns) is demonstrated in Fig. 8 (a) with C_S=1pF and G=10. A difference between expected attenuation in *dv/dt* and obtained experiment value is observed. The first reason is due to the presence of parasitic elements inside the chip and the PCB that are not taken into account in the theoretical study. The second reason is because some extra current is required to put M5 transistor in saturation mode before the feedback loop becomes effective.

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A sub-nanosecond response with the proposed technology is experimentally demonstrated. It can be seen in Fig. 8 the derivative of v_{DS} of the GaN transistor starts to change in less than 1ns due to the feedback-loop effect. Fig. 9 shows the output voltage of the feedback-loop starts to change in less than 1ns just after the GaN transistor v_{DS} falling-edge.

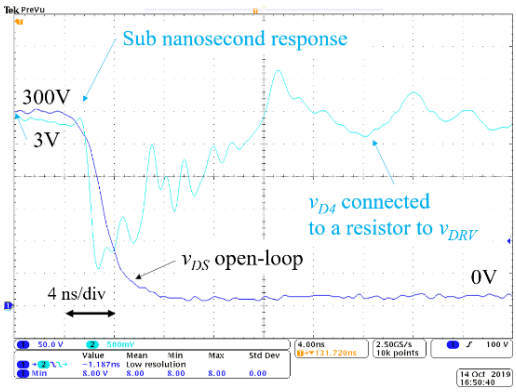

Fig. 9. Experimental waveforms of the propsed system showing an open-loop response with a resistive load (R_G=14.7Ω) connected to v_{DRV}.

VI. Conclusion

This paper develops a theoretical analysis to provide the optimum distribution between the gains of the two current mirrors and the value of the sensing capacitor to maximize the bandwidth of a *dv/dt* feedback control loop. It is demonstrated that the bandwidth of the proposed circuit is correlated to the transition frequency of the CMOS technology. Therefore, choosing a technology with the highest transition frequency, with appropriate voltage capabilities to sustain 5V for GaN and 25V for SiC and IGBT applications, is the best choice. It is also demonstrated that for a given constant GC_S product, the higher the sensing capacitor C_S, the higher the bandwidth for the feedback-loop. However, the silicon surface increase with C_S and a trade-off has to be considered.

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