Optimizing heat harvesting in a membrane based planar μTEG: modelling and fabrication, & vice versa

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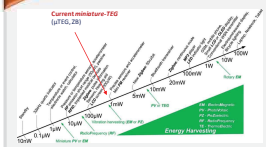
1/ Introduction



Harvested power for different scavenging technologies and corresponding electric power consumption for given devices
M. Haras and T. Skotnicki, Thermoelectricity for IoT – A review, Nano Energy 54 (2018) 461–476

Micro-thermoelectric generators (µTEGs) are energy harvesting solutions to supply electrical power for autonomous microsystems and other miniature applications. We study here original all-Silicon µTEGs with a planar configuration in which the heat to harvest flows in-plane of a TE thin film. Such planar modules are based on a polySi/Au thermopile periodically distributed onto dielectric membranes; a heat-collector permits to concentrate the energy to harvest onto half the junctions of the thermopile. This planar topology allows the implementation of thermocouples with a high aspect ratio compared to classical vertical TEGs. Heat concentrator is able to collect any form of lost heat (even evaporation enthalpy a priori, or radiation..)

2. IEMN µTEG design & process

1st Initial design : semi-3D micro thermoelectric generator, planar structure, CMOS compatible process of microfabrication. Surface foot -print ~ 1/3 cm², build up with 2 parts:

– **Bottom part**: N_M membranes periodically etched in a Si(100) substrate & made of a dielectric bilayer (1,4µm SiO_2/Si_xN_y). A **poly-Silicon** (pSi, e_{TE}=0,3-0,9 µm thick , first thermoelement) stripe is deposited on this bilayer & is periodically covered with gold (Au, 2nd thermoelement). This defines a **zig-zag shaped thermopile**, series of pSi/Au thermocouples (TC) . N_M tested : 1, 2, 5, 10

$$\alpha_{TE/Au} = (\alpha_{Au} - \alpha_{TE}) / (1 + \rho_{TE}/e_{TE} \cdot e_{Au}/\rho_{Au})$$

* The pSi width (L =50, 70 or 200 µm) is larger than the Au plated parts (10 µm) → this **modulated-width** thermopile has a reduced internal electrical resistance R_{INT} → electrical & thermal simulations show a gain in output power generated for larger stripes.

* The TC number, N, is a function of N_M and L : N= x.N_M (x =144, 112, 46 for L=50, 70 ,200µ). For fixed L , R_{INT} is the same.

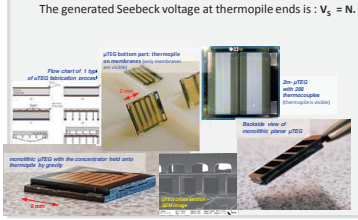
* The whole is covered with a 15µm thick PolyImide layer (robustness & electrical isolation): 15µm is a compromise (for 2m-µG up to 32% higher ΔT for 30µm PI but the benefice fastly diminish with N_M for 10µTEG it is even worse; *see evolution in figure section 4.C/...*)

– **Second part** : heat concentrator HC (surf~0,3cm²) also fabricated starting from Si(100). It has as much **pillars** (N_M) as there are membranes (200µm thick, 5.1 mm long & width optimised versus N_M). Pillars canalyze the heat flow to harvest (Φ , that arrives on its surface) into half of the thermopile junctions. A periodical ΔT is created at each TC.
The HC has also **4 bosses** at its corners (mechanical stability, avoid membranes breaking) that short-cut one part of Φ:

$$\Phi_{Total} = \Phi_{Pillars} + \Phi_{Bosses} + \Phi_{convection} + \Phi_{cavities}$$

Example of planar µTEG: with N_M = 5 membranes (noted 5m-µG) with a modulated-width type thermopile

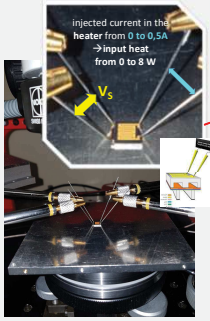
The generated Seebeck voltage at thermopile ends is : $V_S = N.\ a_{TE/Au} \cdot \Delta T_{TC}$

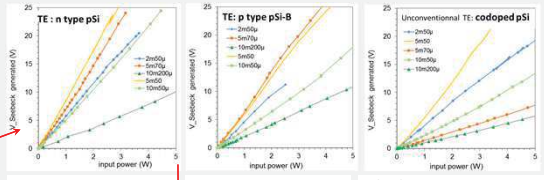


3. Characterisation of µTEG performance

Typical µTEG experimental behaviour : at RT, the heat to harvest is varied from low to very high (Φ : 0→8W)
Open circuit voltage is measured → it gives Seebeck voltage generated $V_{S\text{-}EXP.}$ and the difference of temperature ΔT is deduced using $\Delta T_{TC} = V_S / (N.\ \alpha_{TE/Au})$
Here is given : characterization of µTEG integrating optimum n or p type polySi as the TE layer.

Layer Power Factor is given : PF = α^2/ρ
The Efficiency Factor is experimental: F = $P_{MAX}/\Delta T^2$
(but F is 'weak' parameter to evaluate performance ....)



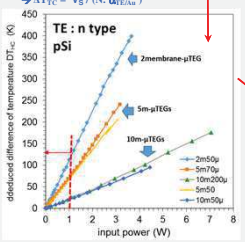


TE : n type pSi Phosphorus doped & annealed
n=7,5.10²⁰.cm⁻³ , α = -178 µV/K
PF = 8,4 µW/K²/cm
R_{INT} : 45 --> 560 kΩ (a function of N_M)
F_{INT} : 5 --> 114 nW/K²/cm²
$V_{S\text{-}EXP}$ and ΔT are consistent with λ ~ 31 W/K/m

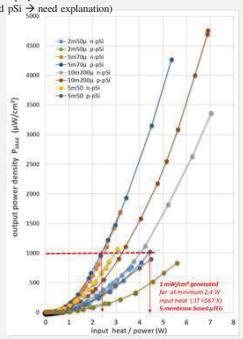
TE : p type pSi Boron implanted & annealed
p=1,8.10²⁰.cm⁻³ , α = 166 µV/K
PF = 21,4 µW/K²/cm
R_{INT} : 36 --> 580 kΩ
F_{INT} : 3 --> 119 nW/K²/cm²
$V_{S\text{-}EXP}$ and ΔT consistent with λ ~ 31 W/K/m

Codoped pSi Phosphorus and Arsenic & annealed
n=1,3.10²⁰.cm⁻³ , α = -198 µV/K
PF = 24 µW/K²/cm
R_{INT} : 23 --> 340 kΩ
F_{INT} : 9 --> 264 nW/K²/cm²
$V_{S\text{-}EXP}$ and deduced ΔT are too low: what is the value of λ ~ ?
→ λ higher than expected (modified microstructure or so...)
see hereafter reverse deduction by modelling (section 4.D/)

→ $\Delta T_{TC} = V_S / (N.\ \alpha_{TE/Au})$



→ maximum output power on adapted load : $P_{MAX} = V_S^2 / 4.\ R_{INT}$
Best output power for polySi with best PF
(exception: codoped pSi → need explanation)



The µTEG module thermal resistance:
in a conservative evaluation, it is given by the slope of the ΔT(Φ) experimental curve: $r_{TH} \sim \Delta T_{TC}/\Phi$

Experimental findings
2m-µG : r_{TH} ~ 70-113 K/W
(module for situation needing high thermal adapt°)
5m-µG : r_{TH} ~ 30-71 K/W
(best module in terms of P_{MAX})
10m-µG : r_{TH} ~ 11-27 K/W
(for fixed Φ has lower ΔT so module is less damaged with time)

Large values are consistent with our geometry using very long TC.

P_{MAX} expected value is given by: $= \frac{N^2 \alpha_{TE/Au}^2 \Delta T_{hc}^2}{4 R_{INT}}$

The experimental thermopile internal electrical resistance R_{INT} often contains a non negligible contribution from contact resistance (between thermoelements)

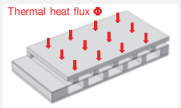
Best output power generated for 1W heat to harvest
2m-µG : P_{MAX} ~ 28 - 62 µW/cm² (expected 46 – 66)
5m-µG : P_{MAX} ~ 45 - 165 µW/cm² (expected 124 – 192)
10m-µG : P_{MAX} ~ 16 - 86 µW/cm² (expected 67 – 135)
µTEGs with codoped pSi : not taken into account

→ *For a fixed amount of heat to harvest, 5-membranes µTEGs are confirmed to perform the best*
→ *However, in any case, these values are low because of large internal electrical resistance R_{INT} of the thermopiles pSi/Au.*

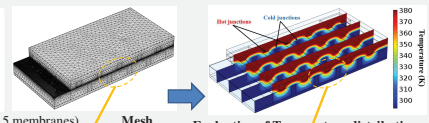
4. Thermal Modelling - Reducing heat losses & considering superior TE layer properties

Renewed design to improve the performance: ***a few routes to be validated by forthcoming experiments***

•4.A/ 3D thermal modelling using COMSOL Multiphysics®,

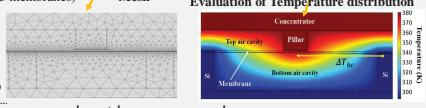


Geometry of half µTEG (here 5 membranes) **Mesh** **Evaluation of Temperature distribution**



A heat flux of 1W is applied on the concentrator surface and the temperature of the backside of the Si substrate is kept at 293 K (RT).

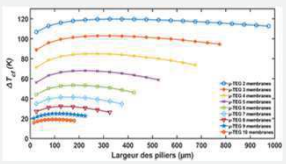
An equivalent layer is considered to Account for multi-layer membranes...



$$\lambda_{eq} e_{eq} = \lambda_{SiO_2} e_{SiO_2} + \lambda_{Si_xN_y} e_{Si_xN_y} + \lambda_{polysi} e_{polysi} \frac{l_{polysi} + l_{Au} + 2l}{l_{polysi} + l_{Au} + 2l} + \lambda_{Au} e_{Au} \frac{l_{Au}}{l_{polysi} + l_{Au} + 2l}$$

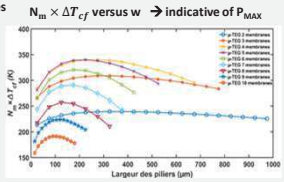
•4.B/ Geometrical structure optimisation (Φ=1W)

ΔT_{cf} versus pillar width, w, for µTEG with 2 to 10 membranes



The difference of temperature at each TC in the thermopile has a maximum at an optimum pillar width value.

$N_m \times \Delta T_{cf}$ versus w → indicative of P_{MAX}



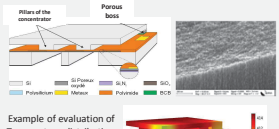
The 4 and 5 membranes µTEG configurations would generate the highest output power (within this modelling and its assumptions) Their HC should be tailored with optimum pillar width ~ 225 µm.

The difference of temperature being higher for µTEGs with 4 membranes , these latter will have the highest thermal resistance r_{TH} compared to 5m-µTEG → to be taken into account in future design

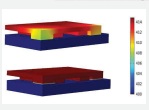
•4.C/ Reducing the heat lost in the bosses of the heat-concentrator

Reducing Φ_{Bosses} by lowering bosses thermal conductivity: done via local fabrication of *Porous Silicone* by anodization then oxidization (annealing at high temperature).

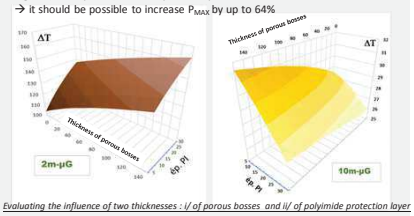
λ_{Si} = 140 W/m/K VERSUS $\lambda_{porous\text{-}Si\ oxidized}$ ~ 1 W/m/K



Example of evaluation of Temperature distribution in a half 2m-µTEG when (top) bosses are normal & (bottom) when bosses are made of **porous-Si**



The difference of temperature ΔT can be up to 28% higher (in 2m-µTEGs) with 150µm thick porous-Si bosses
→ it should be possible to increase P_{MAX} by up to 64%



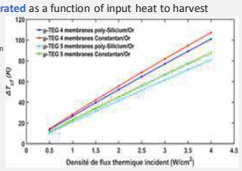
Evaluating the influence of two thicknesses : i/ of porous bosses and ii/ of polyimide protection layer

•4.D/ Modelling the impact of TE thermal conductivity & optimisation of generated output power

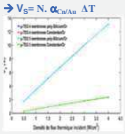
a/ Considering a metal TE layer with good PF and which impacts less R_{INT} (reduced value and no parasitic contact resistance)
→ **Constantan/Au thermopile**

ΔT_{cf} to be generated as a function of input heat to harvest

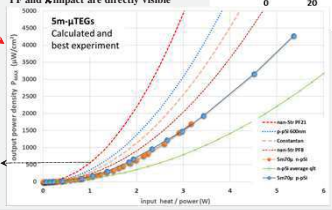
Constantan layer :
PF(Cn) ~ 28,9µW/K²/cm
α = 38µV/K
e = 600 nm



→ $V_S = N.\ \alpha_{Cn/Au}\ \Delta T$

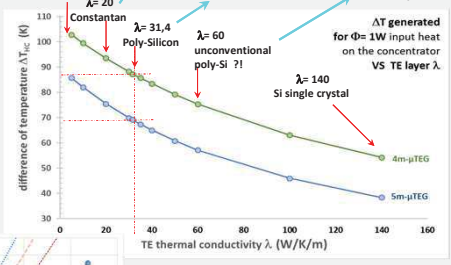


→ $P_{MAX} = V_S^2 / 4.\ R_{INT}$
PF and λ impact are directly visible



With a nanostructured TE layer (λ =4 & PF= 21) the max output power would be > 0,5mW/cm² for Φ=1W heat input

b/ Considering different TE layers with different thermal conductivities λ
Preliminary test validate higher ΔT
To be continued with also better PF



- Case Constatan/Au: 600/250nm
- Cases for TE layers with PF 8 or 21:
---Experimental points : *p and n type polySi as for p-pSi layer e_{TE}=280nm, an extrapolation for 600nm is calculated*
---Nanostructured TE layer taken with λ = 4 W/K/m

Any new polySi would be interesting if it combines low λ (<10W/K/m) and large PF (>15µW/K²/cm) in order the µTEGs to perform equivalently or better than the theoretical Cn/Au case ...

5 - Conclusions

All-Silicon planar µTEG with a modular thermal resistance (11-113 K/W) are fabricated by CMOS compatible microtechnology, integrating a thermopile built up with micro/nano-structured polySi as TE material. The number of membranes on which is periodically laying the thermopile can be varied and the heat to harvest is collected through a pillar-based Si-concentrator. The weak point of our µTEGs is their high internal electrical resistance: P_{MAX} are moderate: up to 62µW/cm², **164µW/cm²**, and 86 µW/cm², for respectively 2, **5** or 10 membranes µTEGs (1W heat injected).

To better clarify further improvements to be carried out, while keeping the high r_{TH} values, COMSOL 3D thermal simulation was done for different new situations:

- Better dimensioning: - the optimum membrane number is 4 (not 5): same P_{MAX} and higher r_{TH}
  - use larger stripe (L=200µm versus currently 70µm) should be considered (20% increase in P_{MAX})
- Elimination of parasitic heat losses:
  - ✓Polyimide layer : confirmation of an optimal thickness (around 15µm)
  - ✓a modified heat-collector/concentrator with corner bosses made of porous Silicon allows to generate up to 64% more power, but this requires to be validated by experiments (soon)
- Higher Power Factor (PF) effect: considering a thermopile integrating a Constantan layer can double P_{MAX} (~300 µW/cm² for 1W injected). Compared to modules with *non optimum polySi* (ie. with PF < 10 µW/K²/cm or so) this represent a reliable way to enhance P_{MAX} by a factor of up to 3. However this is only valid for a TE stripe width of L=50 µm (for larger L it decreases) →this is being evaluated (together with 4-membranes configuration and porous bosses in the heat-concentrator)
- High PF but bad microstructure of the TE layer : it results in poorer module performance *("cold case" explained* : codoped polySi layer may have λ> 60W/K/m...)
- Considering nanostructured TE layer with a thermal conductivity λ reduced by a factor of 10 compared to polySi (ie even better than Cn) should result in a higher ΔT (24,6% for 5m-µTEG), so in a P_{MAX} 65% higher (assuming same PF as our best p-type polySi) → in such a case 550-660 µw/cm² should be obtained for a 5m-µTEG harvesting 1W input heat.

Some previous work :
K. Zioucha et al. JMEMS 26, 067003 (2017)45
Z. Bougrioua et al., 14th Eur. Thermoelectric Conf. (2016), Lisboa
Z. Yuan et al. , Sensors and Actuators, A 221 (2015) 67

Key Words: micro-generator, ThermoElectric, thermal conductivity, power factor, module modelling, planar

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