



HAL
open science

Optimizing heat harvesting in a membrane based planar μ TEG: modelling and fabrication, & vice versa

Zahia Bougrioua, Ibrahim Bel-Hadj, Katir Ziouche

► To cite this version:

Zahia Bougrioua, Ibrahim Bel-Hadj, Katir Ziouche. Optimizing heat harvesting in a membrane based planar μ TEG: modelling and fabrication, & vice versa. ECT 2019 – 17th European Conference on Thermoelectrics, Sep 2019, Limassol, Cyprus. . hal-02906736

HAL Id: hal-02906736

<https://hal.science/hal-02906736v1>

Submitted on 9 Dec 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

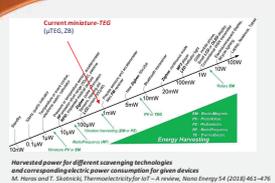
Optimizing heat harvesting in a membrane based planar μ TEG: modelling and fabrication, & vice versa

Zahia BOUGRIOUA*, Ibrahim BEL-HADI, Katir ZIOUCHE

IEMN, Institut d'Electronique de Micro-electronique et de Nanotechnologie,
CNRS and Lille University, avenue Poincaré, 59652 Villeneuve d'Ascq, FRANCE

E-mail *: zahia.bougrioua@iemn.fr

1/ Introduction



Micro-thermoelectric generators (μ TEGs) are energy harvesting solutions to supply electrical power for autonomous microsystems and other miniature applications. We study here original all-Silicon μ TEGs with a planar configuration in which the heat to harvest flows in-plane of a TE thin film. Such planar modules are based on a polySi/Au thermopile periodically distributed onto dielectric membranes; a heat-collector permits to concentrate the energy to harvest onto half the junctions of the thermopile. This planar topology allows the implementation of thermopiles with a high aspect ratio compared to classical vertical TEGs. Heat concentrator is able to collect any form of lost heat (even evaporation enthalpy a priori, or radiation...)

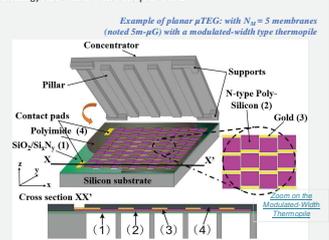
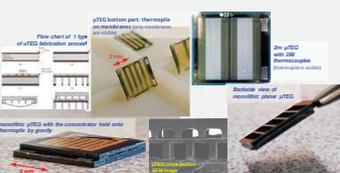
2. IEMN μ TEG design & process

1st Initial design : semi-3D micro thermoelectric generator, planar structure, CMOS compatible process of microfabrication. Surface foot-print $\sim 1/3$ cm², build up with 2 parts:

- Bottom part: N_M membranes periodically etched in a Si(100) substrate & made of a dielectric bilayer (1.4 μ m SiO₂/Si₃N₄). A poly-Silicon (pSi, $e_{pSi} \sim 0.3-0.9$ μ m thick, first thermopile) strip is deposited on this bilayer & is periodically covered with gold (Au, 2nd thermopile). This defines a zig-zag shaped thermopile, series of pSi/Au thermopiles (TC) : N_M tested : 1, 2, 5, 10
- * The pSi width ($L = 50, 70$ or 200 μ m) is larger than the Au plated parts (10 μ m) \rightarrow this modulated-width thermopile has a reduced internal electrical resistance R_{int} \rightarrow electrical & thermal simulations show a gain in output power generated for larger stripes.
- * The TC number, N , is a function of N_M and L : $N = x \cdot N_M$ ($x = 144, 112, 46$ for $L = 50, 70, 200$ μ m). For fixed L , R_{int} is the same.
- * The whole is covered with a 15 μ m thick Polyimide layer (robustness & electrical isolation): 15 μ m is a compromise (for 2m- μ G up to 32% higher ΔT for 30 μ m PI but the benefits fastly diminish with N_M , for 10 μ m TEG it is even worse; see evolution in figure section 4.C...)
- Second part : heat concentrator HC ($surf = 0.3$ cm²) also fabricated starting from Si(100). It has as much pillars (N_H) as there are membranes (200 μ m thick, 5.1 mm long & width optimised versus N_M). Pillars catalyze the heat flow to harvest (Φ , that arrives on its surface) into half of the thermopile junctions. A periodical ΔT is created at each TC.

$$\Phi_{Total} = \Phi_{Pillars} + \Phi_{Bosses} + \Phi_{convection} + \Phi_{cavities}$$

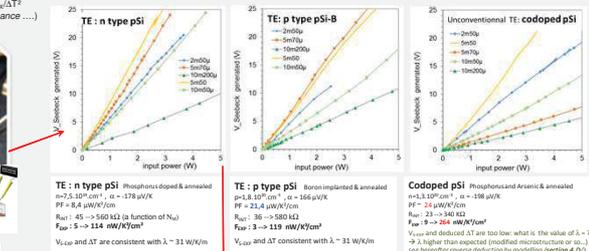
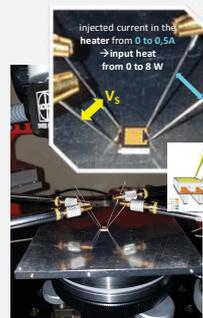
The generated Seebeck voltage at thermopile ends is : $V_S = N \cdot \alpha_{TE/Au} \cdot \Delta T_{TC}$



3. Characterisation of μ TEG performance

Typical μ TEG experimental behaviour : at RT, the heat to harvest is varied from low to very high ($\Phi : 0 \rightarrow 8$ W)
Open circuit voltage is measured \rightarrow it gives Seebeck voltage generated $V_{S,OC}$ and the difference of temperature ΔT is deduced using $\Delta T_{TC} = V_S / (N \cdot \alpha_{TE/Au})$
Here is given : characterization of μ TEG integrating optimum n or p type polySi as the TE layer.

Layer Power Factor is given : $PF = \alpha^2 / \rho$
The Efficiency Factor is experimental: $F = P_{MAX} / \Delta T^2$
(but F is 'weak' parameter to evaluate performance...)



The μ TEG module thermal resistance: in a conservative evaluation, it is given by the slope of the $\Delta T(\Phi)$ experimental curve:
 $R_{TH} = \Delta T_{TC} / \Phi$

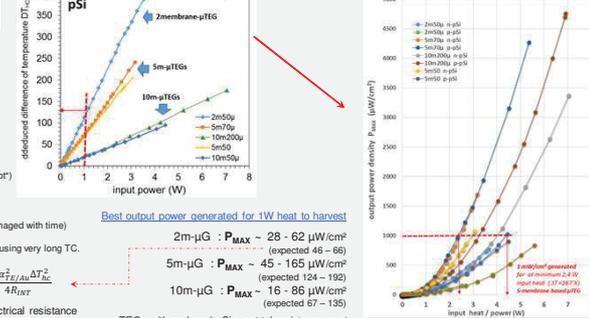
Experimental findings:
2m- μ G : $F_{TH} \sim 70-113$ KW (module for situation needing high thermal adapt)
5m- μ G : $F_{TH} \sim 30-71$ KW (best module in terms of P_{MAX})
10m- μ G : $F_{TH} \sim 11-27$ KW (for fixed Φ has lower ΔT so module is less damaged with time)

Large values are consistent with our geometry using very long TC.

$$P_{MAX} \text{ expected value is given by: } \frac{N^2 \alpha_{TE/Au}^2 \Delta T_{TC}^2}{4 R_{int}}$$

The experimental thermopile internal electrical resistance R_{int} often contains a non negligible contribution from contact resistance (between thermoelements)

\rightarrow maximum output power on adapted load : $P_{MAX} = V_S^2 / 4 \cdot R_{int}$
Best output power for polySi with best PF (exception: codoped pSi \rightarrow need explanation)

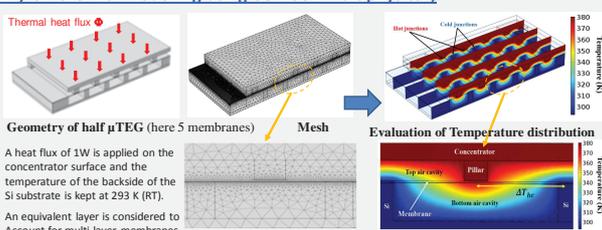


\rightarrow For a fixed amount of heat to harvest, 5-membranes μ TEGs are confirmed to perform the best
 \rightarrow However, in any case, these values are low because of large internal electrical resistance R_{int} of the thermopiles pSi/Au.

4. Thermal Modelling - Reducing heat losses & considering superior TE layer properties

Renewed design to improve the performance: a few routes to be validated by forthcoming experiments

4.A/ 3D thermal modelling using COMSOL Multiphysics®



Geometry of half μ TEG (here 5 membranes)

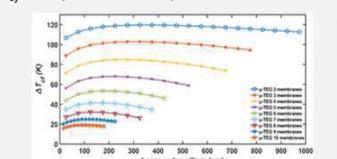
A heat flux of 1W is applied on the concentrator surface and the temperature of the backside of the Si substrate is kept at 293 K (RT).

An equivalent layer is considered to Account for multi-layer membranes...

$$\lambda_{eq} = \lambda_{SiO2} e_{SiO2} + \lambda_{Si3N4} e_{Si3N4} + \lambda_{pSi} e_{pSi} + \lambda_{Au} e_{Au}$$

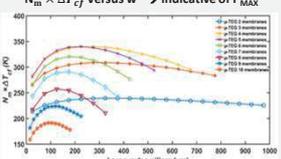
4.B/ Geometrical structure optimisation ($\Phi = 1$ W)

ΔT_{TC} versus pillar width, w , for μ TEG with 2 to 10 membranes



The difference of temperature at each TC in the thermopile has a maximum at an optimum pillar width value.

$N_M \times \Delta T_{TC}$ versus $w \rightarrow$ indicative of P_{MAX}

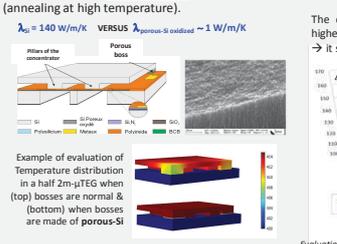


The 4 and 5 membranes μ TEG configurations would generate the highest output power (within this modelling and its assumptions) Their HC should be tailored with optimum pillar width ~ 225 μ m.

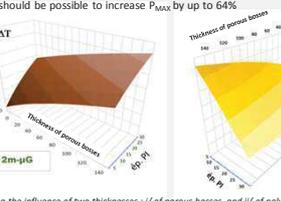
4.C/ Reducing the heat lost in the bosses of the heat-concentrator

Reducing Φ_{Bosses} by lowering bosses thermal conductivity: done via local fabrication of Porous Silicon by anodization then oxidation (annealing at high temperature).

$$\lambda_{Si} = 140 \text{ W/m/K} \text{ VERSUS } \lambda_{porous-Si} \text{ oxidized} \sim 1 \text{ W/m/K}$$



The difference of temperature ΔT can be up to 28% higher (in 2m- μ TEG) with 150 μ m thick porous-Si bosses \rightarrow it should be possible to increase P_{MAX} by up to 64%

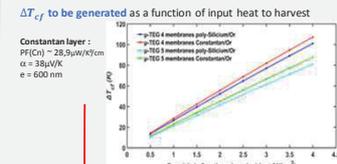


Evaluating the influence of two thicknesses : l_p of porous bosses and l_{PI} of polyimide protection layer

4.D/ Modelling the impact of TE thermal conductivity & optimisation of generated output power

a/ Considering a metal TE layer with good PF and which impacts less R_{int} (reduced value and no parasitic contact resistance) \rightarrow Constantan/Au thermopile

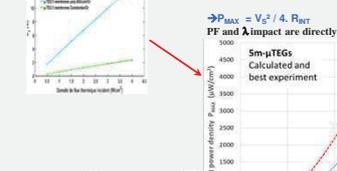
ΔT_{TC} to be generated as a function of input heat to harvest



$$V_S = N \cdot \alpha_{TE/Au} \cdot \Delta T$$

$\rightarrow P_{MAX} = V_S^2 / 4 \cdot R_{int}$

PF and Ampact are directly visible



With a nanostructured TE layer ($\lambda = 4$ & PF = 21) the max output power would be > 0.5 MW/cm² for $\Phi = 1$ W heat input

b/ Considering different TE layers with different thermal conductivities λ

Preliminary test validate higher ΔT To be continued with also better PF

Constantan/Metal TC are being tested (2019 - 2020)

$\lambda = 4$ nanostructured TE

$\lambda = 20$ Constantan

$\lambda = 31,4$ Poly-Silicon

$\lambda = 60$ unconventional poly-Si ?!

$\lambda = 140$ Si single crystal

ΔT generated for $\Phi = 1$ W input heat on the concentrator VS TE layer λ .

\rightarrow To be confirmed

Detrimental codoping ?

4m- μ TEG

5m- μ TEG

Case Constantan/Au: 600/250nm

Cases for TE layers with PF 8 or 21:

Experimental points: p and n type polySi

as for p-Si layer $e_{pSi} = 280$ nm, an extrapolation for 600nm is calculated

Nanostructured TE layer taken with $\lambda = 4$ W/K/m

Any new polySi would be interesting if it combines low λ (<10W/K/m) and large PF (>15 μ W/K²cm) in order the μ TEGs to perform equivalently or better than the theoretical Cn/Au case ...

5 - Conclusions

All-Silicon planar μ TEG with a modular thermal resistance (11-113 K/W) are fabricated by CMOS compatible microtechnology, integrating a thermopile built up with micro/nano-structured polySi as TE material. The number of membranes on which is periodically laying the thermopile can be varied and the heat to harvest is collected through a pillar-based Si-concentrator. The weak point of our μ TEG is their high internal electrical resistance: P_{MAX} are moderate: up to 62 μ W/cm², 16 μ W/cm², and 86 μ W/cm², for respectively 2, 5 or 10 membranes μ TEGs (1W heat injected).

To better clarify further improvements to be carried out, while keeping the high F_{TH} values, COMSOL 3D thermal simulation was done for different new situations:

- Better dimensioning: the optimum membrane number is 4 (not 5): same P_{MAX} and higher F_{TH} - use larger stripe ($L = 200$ μ m versus currently 70 μ m) should be considered (20% increase in P_{MAX})
- Elimination of parasitic heat losses:
 - polyimide layer: confirmation of an optimal thickness (around 15 μ m)
 - a modified heat-collector/concentrator with corner bosses made of porous Silicon allows to generate up to 64% more power, but this requires to be validated by experiments (soon)
- Higher Power Factor (PF) effect: considering a thermopile integrating a Constantan layer can double P_{MAX} (~ 300 μ W/cm² for 1W injected). Compared to modules with non optimum polySi (ie. with PF < 10 μ W/K²cm or so) this represent a reliable way to enhance P_{MAX} by a factor of up to 3. However this is only valid for a TE stripe length of $L = 50$ μ m (for larger L it decreases) \rightarrow this is being evaluated (together with 4-membranes configuration and porous bosses in the heat-concentrator)
- High PF but bad microstructure of the TE layer: it results in poorer module performance ("cold case" explained: codoped polySi layer may have $\lambda > 60$ W/K/m...)
- Considering nanostructured TE layer with a thermal conductivity λ reduced by a factor of 10 compared to polySi (ie even better than Cn) should result in a higher ΔT (24,6% for 5m- μ TEG), so in a P_{MAX} 65% higher (assuming same PF as our best p-type polySi) \rightarrow in such a case 550-660 μ W/cm² should be obtained for a 5m- μ TEG harvesting 1W input heat.