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# Optimizing heat harvesting in a membrane based planar $\mu$ TEG: modelling and fabrication, & vice versa

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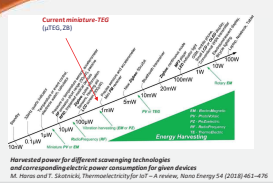
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## 1/ Introduction



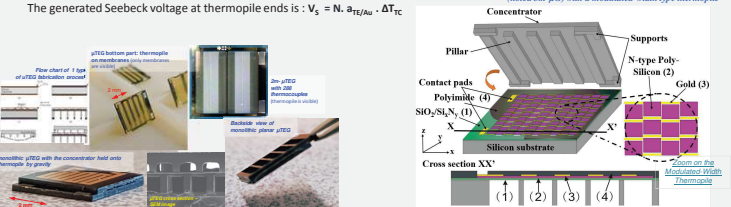
Micro-thermoelectric generators ( $\mu$ TEGs) are energy harvesting solutions to supply electrical power for autonomous microsystems and other miniature applications. We study here original all-Silicon  $\mu$ TEGs with a planar configuration in which the heat to harvest flows in-plane of a TE thin film. Such planar modules are based on a polySi/Au thermopile periodically distributed onto dielectric membranes; a heat-collector permits to concentrate the energy to harvest onto half the junctions of the thermopile. This planar topology allows the implementation of thermopiles with a high aspect ratio compared to classical vertical TEGs. Heat concentrator is able to collect any form of lost heat (even evaporation enthalpy a priori, or radiation...)

## 2. IEMN $\mu$ TEG design & process

1<sup>st</sup> Initial design : semi-3D micro thermoelectric generator, planar structure, CMOS compatible process of microfabrication. Surface foot-print  $\sim 1/3$  cm<sup>2</sup>, build up with 2 parts:

- **Bottom part:**  $N_m$  membranes periodically etched in a Si(100) substrate & made of a dielectric bilayer (1.4  $\mu$ m SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>). A poly-Silicon (pSi,  $e_{pSi} \sim 0.3-0.9$   $\mu$ m thick, first thermopile) strip is deposited on this bilayer & is periodically covered with gold (Au, 2<sup>nd</sup> thermopile). This defines a zig-zag shaped thermopile, series of pSi/Au thermopiles (TC) :  $N_m$  tested : 1, 2, 5, 10
- \* The pSi width ( $L=50, 70$  or  $200$   $\mu$ m) is larger than the Au plated parts ( $10$   $\mu$ m)  $\rightarrow$  this modulated-width thermopile has a reduced internal electrical resistance  $R_{int}$   $\rightarrow$  electrical & thermal simulations show a gain in output power generated for larger stripes.
- \* The TC number,  $N$ , is a function of  $N_m$  and  $L$ :  $N = x \cdot N_m$  ( $x=144, 112, 46$  for  $L=50, 70, 200$   $\mu$ m). For fixed  $L$ ,  $R_{int}$  is the same.
- \* The whole is covered with a 15  $\mu$ m thick Polyimide layer (robustness & electrical isolation): 15  $\mu$ m is a compromise (for 2m- $\mu$ G up to 32% higher  $\Delta T$  for 30  $\mu$ m PI but the benefits fastly diminish with  $N_m$ , for 10  $\mu$ m TEG it is even worse; see evolution in figure section 4.C...)
- **Second part :** heat concentrator HC ( $surf \sim 0.3$  cm<sup>2</sup>) also fabricated starting from Si(100). It has as much pillars ( $N_{hp}$ ) as there are membranes (200  $\mu$ m thick, 5.1 mm long & width optimised versus  $N_m$ ). Pillars catalyze the heat flow to harvest ( $\Phi$ , that arrives on its surface) into half of the thermopile junctions. A periodical  $\Delta T$  is created at each TC.
- The HC has also 4 bosses at its corners (mechanical stability, avoid membranes breaking) that short-cut one part of  $\Phi$ :  

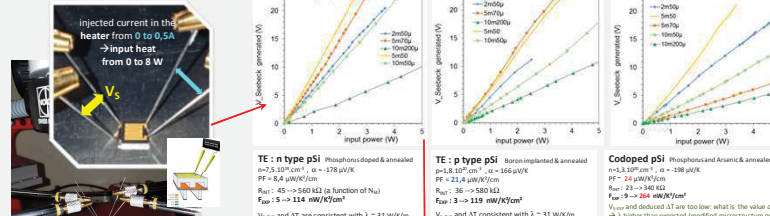
$$\Phi_{Total} = \Phi_{Pillars} + \Phi_{Bosses} + \Phi_{concentration} + \Phi_{Cavities}$$



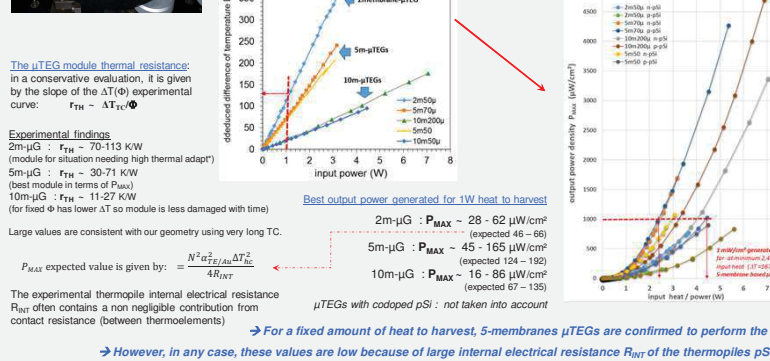
## 3. Characterisation of $\mu$ TEG performance

Typical  $\mu$ TEG experimental behaviour : at RT, the heat to harvest is varied from low to very high ( $\Phi : 0 \rightarrow 8$  W)  
Open circuit voltage is measured  $\rightarrow$  it gives Seebeck voltage generated  $V_{oc}$  and the difference of temperature  $\Delta T$  is deduced using  $\Delta T_{TC} = V_{oc} / (N_m \cdot \alpha_{TE/Au})$   
Here is given : characterization of  $\mu$ TEG integrating optimum n or p type polySi as the TE layer.

Layer Power Factor is given :  $PF = \alpha^2 \rho$   
The Efficiency Factor is experimental:  $F = P_{MAX} / \Delta T^2$   
(but  $F$  is weak parameter to evaluate performance...)



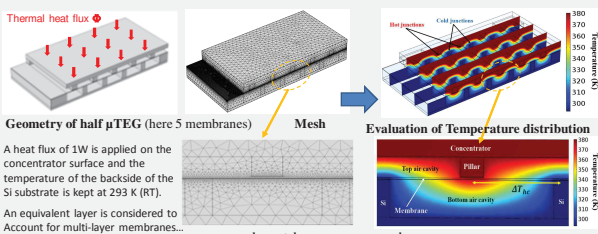
$\Delta T_{TC} = V_{oc} / (N_m \cdot \alpha_{TE/Au})$   
 $\rightarrow$  maximum output power on adapted load:  $P_{MAX} = V_{oc}^2 / 4 \cdot R_{int}$   
Best output power for polySi with best PF (exception: codoped pSi  $\rightarrow$  see explanation)



## 4. Thermal Modelling - Reducing heat losses & considering superior TE layer properties

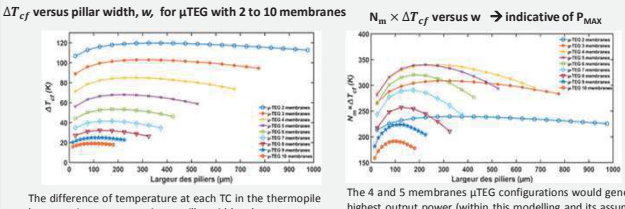
Renewed design to improve the performance: a few routes to be validated by forthcoming experiments

### 4.A/ 3D thermal modelling using COMSOL Multiphysics®



A heat flux of 1W is applied on the concentrator surface and the temperature of the backside of the Si substrate is kept at 293 K (RT).  
An equivalent layer is considered to Account for multi-layer membranes...

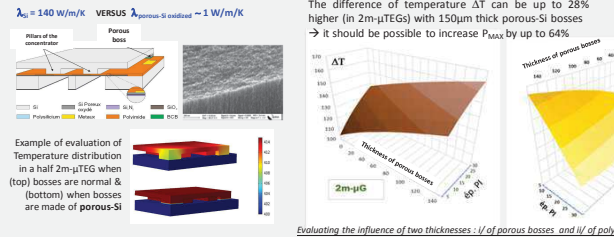
### 4.B/ Geometrical structure optimisation ( $\Phi=1$ W)



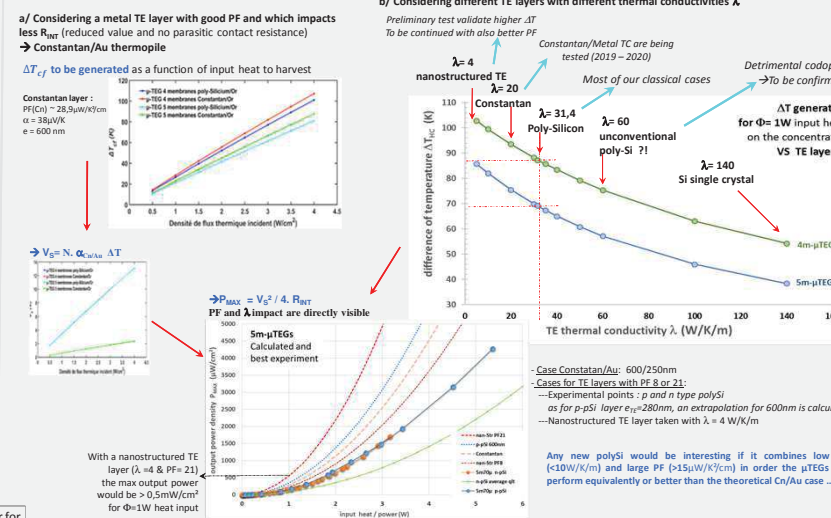
The difference of temperature at each TC in the thermopile has a maximum at an optimum pillar width value.

### 4.C/ Reducing the heat lost in the bosses of the heat-concentrator

Reducing  $\Phi_{Bosses}$  by lowering bosses thermal conductivity: done via local fabrication of Porous Silicon by anodization then oxidation (annealing at high temperature).



### 4.D/ Modelling the impact of TE thermal conductivity & optimisation of generated output power



## 5 - Conclusions

All-Silicon planar  $\mu$ TEG with a modular thermal resistance (11-113 K/W) are fabricated by CMOS compatible microtechnology, integrating a thermopile built up with micro/nano-structured polySi as TE material. The number of membranes on which is periodically laying the thermopile can be varied and the heat to harvest is collected through a pillar-based Si-concentrator. The weak point of our  $\mu$ TEG is their high internal electrical resistance:  $P_{MAX}$  are moderate: up to 62  $\mu$ W/cm<sup>2</sup>, 16  $\mu$ W/cm<sup>2</sup>, and 86  $\mu$ W/cm<sup>2</sup>, for respectively 2, 5 or 10 membranes  $\mu$ TEGs (1W heat injected).

- To better clarify further improvements to be carried out, while keeping the high  $r_{th}$  values, COMSOL 3D thermal simulation was done for different new situations:
  - Better dimensioning: the optimum membrane number is 4 (not 5): same  $P_{MAX}$  and higher  $r_{th}$  - use larger stripe ( $L=200$   $\mu$ m versus currently 70  $\mu$ m) should be considered (20% increase in  $P_{MAX}$ )
  - Elimination of parasitic heat losses:
    - ✓ Polyimide layer: confirmation of an optimal thickness (around 15  $\mu$ m)
    - ✓ a modified heat-collector/concentrator with corner bosses made of porous Silicon allows to generate up to 64% more power, but this requires to be validated by experiments (soon)
  - Higher Power Factor (PF) effect: considering a thermopile integrating a Constantan layer can double  $P_{MAX}$  ( $\sim 300$   $\mu$ W/cm<sup>2</sup> for 1W injected). Compared to modules with non optimum polySi (ie. with PF  $< 10$   $\mu$ W/K<sup>2</sup>cm or so) this represent a reliable way to enhance  $P_{MAX}$  by a factor of up to 3. However this is only valid for a TE stripe length of  $L=50$   $\mu$ m (for larger  $L$  it decreases)  $\rightarrow$  this is being evaluated (together with 4-membranes configuration and porous bosses in the heat-concentrator)
  - High PF but bad microstructure of the TE layer : it results in poorer module performance ("cold case" explained : codoped polySi layer may have  $\lambda > 60$ W/K/m...)
  - Considering nanostructured TE layer with a thermal conductivity  $\lambda$  reduced by a factor of 10 compared to polySi (ie even better than Cn) should result in a higher  $\Delta T$  (24.6% for 5m- $\mu$ TEG), so in a  $P_{MAX}$  65% higher (assuming same PF as our best p-type polySi)  $\rightarrow$  in such a case 550-660  $\mu$ W/cm<sup>2</sup> should be obtained for a 5m- $\mu$ TEG harvesting 1W input heat.