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# Optimizing heat harvesting in a membrane based planar μTEG: modelling and fabrication, & vice versa

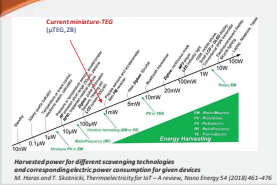
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## 1/ Introduction

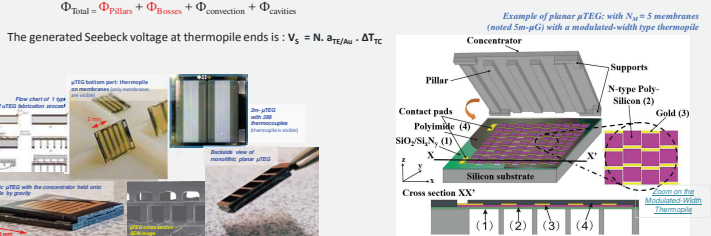


Micro-thermoelectric generators (μTEGs) are energy harvesting solutions to supply electrical power for autonomous microsystems and other miniature applications. We study here original all-Silicon μTEGs with a planar configuration in which the heat to harvest flows in-plane of a TE thin film. Such planar modules are based on a polySi/Au thermopile periodically distributed onto dielectric membranes; a heat-collector permits to concentrate the energy to harvest onto half the junctions of the thermopile. This planar topology allows the implementation of thermopiles with a high aspect ratio compared to classical vertical TEGs. Heat concentrator is able to collect any form of lost heat (even evaporation enthalpy a priori, or radiation...)

## 2. IEMN μTEG design & process

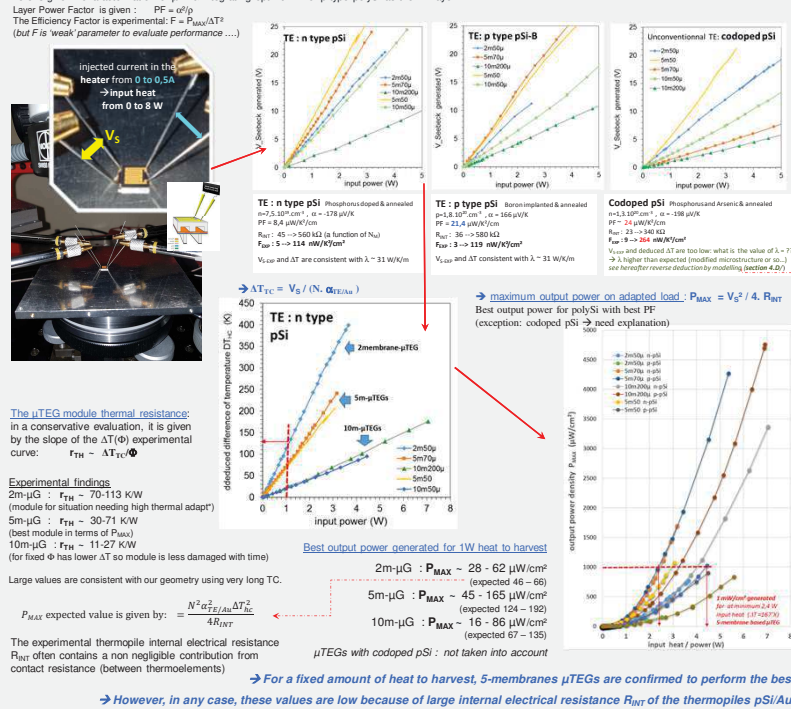
1<sup>st</sup> Initial design : semi-3D micro thermoelectric generator, planar structure, CMOS compatible process of microfabrication. Surface foot-print ~ 1/3 cm<sup>2</sup>, build up with 2 parts:

- **Bottom part:** N<sub>μ</sub> membranes periodically etched in a Si(100) substrate & made of a dielectric bilayer (1.4μm SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>). A poly-Silicon (pSi, e<sub>μ</sub>=0.3-0.9 μm thick, first thermoelement) strip is deposited on this bilayer & is periodically covered with gold (Au, 2<sup>nd</sup> thermoelement). This defines a zig-zag shaped thermopile, series of pSi/Au thermocouples (TC) : N<sub>μ</sub> tested : 1, 2, 5, 10
- \* The pSi width (L=50, 70 or 200 μm) is larger than the Au plated parts (10 μm) → this modulated-width thermopile has a reduced internal electrical resistance R<sub>int</sub> → electrical & thermal simulations show a gain in output power generated for larger stripes.
- \* The TC number, N<sub>μ</sub> is a function of N<sub>μ</sub> and L: N = x.N<sub>μ</sub> (x=144, 112, 46 for L=50, 70, 200μ). For fixed L, R<sub>int</sub> is the same.
- \* The whole is covered with a 15μm thick Polyimide layer (robustness & electrical isolation): 15μm is a compromise (for 2m-μG up to 32% higher ΔT for 30μm PI but the benefits fastly diminish with N<sub>μ</sub>, for 10μTEG it is even worse; see evolution in figure section 4.C...)
- **Second part :** heat concentrator HC (surf=0.3cm<sup>2</sup>) also fabricated starting from Si(100). It has as much pillars (N<sub>μ</sub>) as there are membranes (200μm thick, 5.1 mm long & width optimised versus N<sub>μ</sub>). Pillars catalyze the heat flow to harvest (Φ, that arrives on its surface) into half of the thermopile junctions. A periodical ΔT is created at each TC.



## 3. Characterisation of μTEG performance

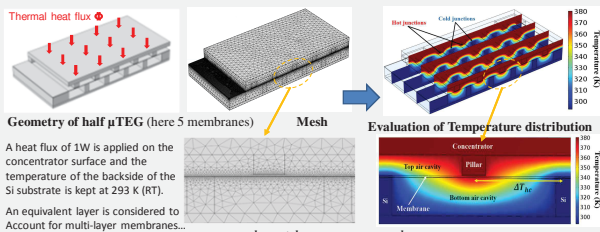
Typical μTEG experimental behaviour : at RT, the heat to harvest is varied from low to very high (Φ : 0-8W)  
Open circuit voltage is measured → it gives Seebeck voltage generated V<sub>OC</sub> and the difference of temperature ΔT is deduced using  $\Delta T_{TC} = V_S / (N_{\mu} \alpha_{TE/Au})$   
Here is given : characterization of μTEG integrating optimum n or p type polySi as the TE layer.



## 4. Thermal Modelling - Reducing heat losses & considering superior TE layer properties

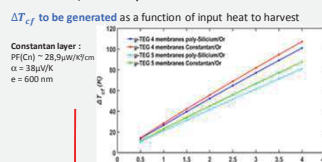
Renewed design to improve the performance: a few routes to be validated by forthcoming experiments

### 4.A/ 3D thermal modelling using COMSOL Multiphysics®

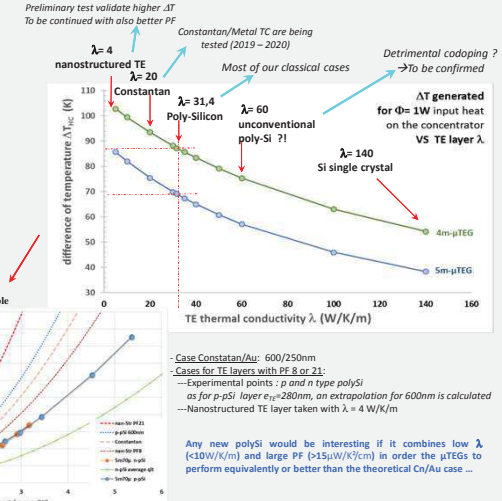


### 4.D/ Modelling the impact of TE thermal conductivity & optimisation of generated output power

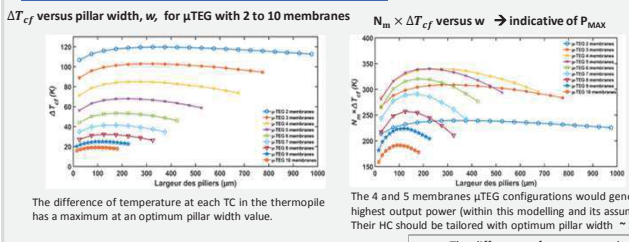
a/ Considering a metal TE layer with good PF and which impacts less R<sub>int</sub> (reduced value and no parasitic contact resistance)  
Less R<sub>int</sub> → constant/Au thermopile



b/ Considering different TE layers with different thermal conductivities λ

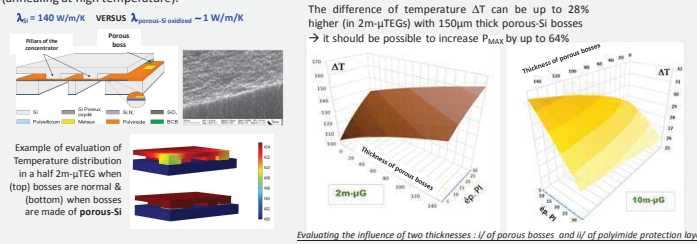


### 4.B/ Geometrical structure optimisation (Φ=1W)



### 4.C/ Reducing the heat lost in the bosses of the heat-concentrator

Reducing Φ<sub>bosses</sub> by lowering bosses thermal conductivity: done via local fabrication of Porous Silicon by anodization then oxidation (annealing at high temperature).



## 5 - Conclusions

- All-Silicon planar μTEG with a modular thermal resistance (11-113 K/W) are fabricated by CMOS compatible microtechnology, integrating a thermopile built up with micro/nano-structured polySi as TE material. The number of membranes on which is periodically laying the thermopile can be varied and the heat to harvest is collected through a pillar-based Si-concentrator. The weak point of our μTEG is their high internal electrical resistance. P<sub>MAX</sub> are moderate: up to 62μW/cm<sup>2</sup>, 164μW/cm<sup>2</sup>, and 86 μW/cm<sup>2</sup>, for respectively 2, 5 or 10 membranes μTEGs (1W heat injected).
- To better clarify further improvements to be carried out, while keeping the high T<sub>th</sub> values, COMSOL 3D thermal simulation was done for different new situations:
  - Better dimensioning: the optimum membrane number is 4 (not 5): same P<sub>MAX</sub> and higher T<sub>th</sub> → use larger stripe (L=200μm versus currently 70μm) should be considered (20% increase in P<sub>MAX</sub>)
  - Elimination of parasitic heat losses:
    - polyimide layer: confirmation of an optimal thickness (around 15μm)
    - a modified heat-collector/concentrator with corner bosses made of porous Silicon allows to generate up to 64% more power, but this requires to be validated by experiments (soon)
  - Higher Power Factor (PF) effect: considering a thermopile integrating a Constantan layer can double P<sub>MAX</sub> (~300 μW/cm<sup>2</sup> for 1W injected). Compared to modules with non optimum polySi (ie. with PF < 10 μW/K<sup>2</sup>·cm or so) this represent a reliable way to enhance P<sub>MAX</sub> by a factor of up to 3. However this is only valid for a TE stripe length of L=50 μm (for larger L it decreases) → this is being evaluated (together with 4-membranes configuration and porous bosses in the heat-concentrator)
  - High PF but bad microstructure of the TE layer : it results in poorer module performance ("cold case" explained : codoped polySi layer may have λ > 60W/K·m...)
- Considering nanostructured TE layer with a thermal conductivity λ reduced by a factor of 10 compared to polySi (ie even better than Cn) should result in a higher ΔT (24,6% for 5m-μTEG), so in a P<sub>MAX</sub> 65% higher (assuming same PF as our best p-type polySi)  
→ in such a case 550-660 μW/cm<sup>2</sup> should be obtained for a 5m-μTEG harvesting 1W input heat.