Highly tunable high-Q inversion-mode MOS varactor in the 1-325-GHz band

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Highly-Tunable High-Q Inversion-Mode MOS Varactor in the 1 GHz -325 GHz band

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***Abstract*—This paper presents the design, experimental results and modeling of an inversion-mode CMOS varactor integrated in the STMicroelectronics 55-nm BiCMOS technology. The device was characterized from 1 GHz to 325 GHz, demonstrating high quality factor at mm-waves. For instance, a quality factor of 7 around 190 GHz for a tuning ratio (C_{max}/C_{min}) greater than 4 was measured. This performance overpasses that of accumulation-mode varactors usually provided in CMOS technologies design kits, for frequencies beyond about 100 GHz. In addition, a small-signal electrical model is provided from 100 GHz to 250 GHz.**

***Index Terms*—Millimeter-Wave, high Q-factor, high tuning ratio.**

I. Introduction

CURRENT needs of high-speed data transmission together with the development of nanometric technology nodes is leading communication standards (e.g., 5G) towards the mm-wave band. The use of mm-wave bands also concerns automotive radars, imaging or medical applications. In higher frequency bands, the user benefits from wider bandwidths and thus, can obtain the desired increase in the data rate or radar resolution. On the other hand, consumer applications require low-cost solutions, such as the ones provided by CMOS or BiCMOS technologies. However, while transistors reach working frequencies (f_T/f_{max}) higher than 400 GHz in BiCMOS technologies to address mm-wave applications [1], the variety of passive tunable elements in these technologies is limited to a few types of varactors or switched inductors. Tunable elements are required, either for performing necessary RF functions, such as tuning of VCOs [2], phase-shift control, in particular to build beam-steering systems allowing to compensate the increase of path-loss in free space [3], calibration purposes, [4] etc. The performance of tunable devices is quantified in terms of tuning range and quality factor (Q). High tuning range and high Q-factor tunable devices are required for state-of-the-art applications. However, these two parameters appear as a trade-off, and the Q-factor of varactors tends to decrease with the working frequency. In this scenario, the design of novel devices with high tuning range and high Q-factor is a key issue in the mm-wave frequency bands. For reference, the reported Q-factor for state-of-the-art varactors in CMOS technologies is around 10 with a tuning ratio (C_{max}/C_{min}) of 1.4 at 100 GHz [5].

In this work, the use of n-type MOSFETs for the design of an Inversion-mode MOS (I-MOS) varactor is proposed. This approach leads to several advantages: (i) I-MOS are present in any CMOS process Design Kit, (ii) the MOSFET model tends to be the more accurate compared to other devices models, in particular compared to Accumulation-mode MOSFETs (A-MOS) varactors, and (iii) their biasing circuitry is simpler than in A-MOS architectures. The study is focused in the 100 GHz to 250 GHz band, even if experimental results are given from 1 GHz to 325 GHz. Beyond about 150 GHz, it is shown that I-MOS varactors lead to higher overall performance (Q-factor vs tuning ratio) as compared to A-MOS varactors. To the best of authors knowledge, this is the first time that I-MOS varactors are studied in the whole mm-wave band up to J-band.

This work is organized as follows: section II presents the theoretical basis of this work together with the state-of-the-art in the field. In section III, the proposed architecture is presented together with a small-signal electrical model of the device. In section IV, after having detailed the measurement setup and its specificities, the measured results are presented and compared to the small-signal model presented in the previous section. Finally, section V presents conclusions of this work.

II. Theoretical Basis

In a CMOS process, varactors can be implemented using four main architectures: (i) Reverse-biased PN junctions (i.e. diodes), (ii) MOS, (iii) A-MOS, and (iv) I-MOS varactors.

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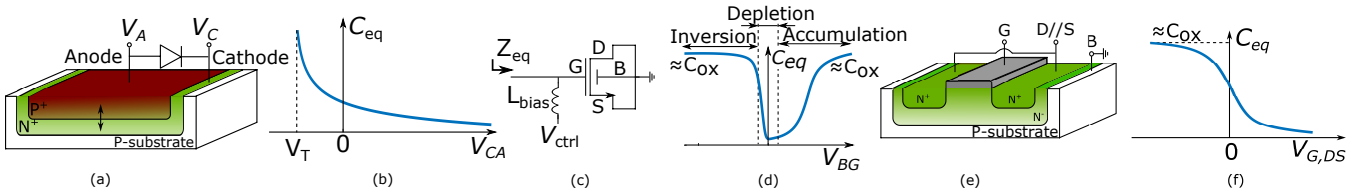

Fig. 1. (a) PN junction and its symbolic representation as a diode. The arrows depict the movement of the charge carriers when the voltage difference between cathode and anode (V_{CA}) increases. (b) Capacitance versus V_{CA}. (c) nMOS transistor with B, D and S connected together. (d) Input capacitance versus V_{BG}. (e) A-MOS varactor. (f) Capacitance at D//S level versus $V_{G,DS}$.

A. *Reverse-biased PN junction*

A PN junction, as depicted in Fig. 1(a), consists of two semiconductors that have been doped to have an excess of electrons or holes (i.e., N-type or P-type semiconductors, respectively). If no bias voltage is applied ($V_{CA} = 0$), the mobile carriers close to the junction diffuse, creating a depletion region near the PN interface. If a bias voltage $V_{CA} < 0$ is applied, the PN junction is said to be forward biased. The holes in the P region and the electrons in the N region are pushed to the interface, thus reducing the width of the depletion zone. For bias voltages $V_{CA} < V_T$, where V_T is the threshold voltage of the junction, the depletion region becomes thin enough to allow conduction across the PN interface.

For voltages $V_{CA} > 0$, the junction is polarized in the so-called reverse bias. The holes in the P region (electrons in the N region) are pulled away from the junction, thus increasing the width of the depletion region (until the diode breaks down or enters in avalanche conduction). From an electrical point of view, for biasing voltages $V_{CA} > V_T$ the PN junction can be modelled as a variable capacitance. The magnitude of voltage V_{CA} controls the width of the depletion region and hence the value of the junction capacitance.

The equivalent capacitance of reverse-biased PN junctions is shown in Fig. 1(b). The equivalent capacitance, C_{eq}, is calculated as in (1):

$$C_{eq} = \frac{-1}{\Im(Z_{eq}) \cdot \omega}, \tag{1}$$

where Z_{eq} (i.e. Z_{11}) is the equivalent impedance of the device and ω the angular frequency at which the measurement is performed.

This capacitance has a large variation range for V_{CA} values close to V_T. However, in this region the leakage currents are non-negligible, resulting in a very lossy, low Q-factor varactor. On the other hand, for values where $V_{CA} >> V_T$ the Q-factor is greatly improved due to reduced leakage currents, but the tuning ratio (C_{max}/C_{min}) is dramatically reduced. In addition, the Q-factor of these devices is often limited by their accesses (e.g. buried collector). To summarize, even though these devices represent a simple solution for the integration of varactors, their intrinsic trade-offs generally make them a less interesting option than their A-MOS or I-MOS counterparts [6].

B. *MOS varactor*

It is well-known that a MOSFET, as depicted in Fig. 1(c), with its drain (D), source (S) and body (B) connected together, performs as a variable capacitance between its gate (G) and B (i.e. D and S) ports, whose value is a function of the voltage difference between body and gate accesses (V_{BG}). In Fig. 1(c), V_{BG} is equivalent to $-V_{ctrl}$, which is applied through an ideal biasing inductance L_{bias} placed at gate level. Such a device can work in the accumulation mode for $V_{BG} > V_T$, where V_T is the threshold voltage of the transistor, when the voltage difference between the bulk silicon and the gate of the transistor is positive and high enough to allow charge carriers to move freely. This device can also work in the inversion mode, where an inversion channel with mobile electrons builds up, for $V_{BG} < -V_T$. Between these two regions, the depletion region is found, where there are very few charge carriers at the gate oxide interface. These operating regions together with the equivalent capacitance are plotted in Fig. 1(d).

The maximum capacitance of these varactors in the strong-accumulation (i.e. $V_{BG} >> V_T$) and strong-inversion (i.e. $V_{BG} << -V_T$) regions approximates to $C_{ox} = \epsilon_{ox} \cdot S/t_{ox}$ (neglecting second-order effects such as the quantum capacitance that slightly reduces this maximum value), where ϵ_{ox} is the oxide permittivity, S the channel area and t_{ox} the oxide thickness.

C. *A-MOS varactor*

A-MOS varactors are built from traditional MOS transistors with a variation in drain/source doping to ensure that they operate either in depletion or accumulation modes, never entering in the inversion mode. Such doping variations usually consist in N^+-drain/source implants in an N^--well. Fig. 1(e) displays an A-MOS varactor. For the sake of simplicity, let us name the ports of the A-MOS as if it was a traditional transistor (i.e. gate (G), drain (D), source (S), and body (B)). When the B of such device is connected to the ground, its D and S ports are connected together and a control voltage is applied to G, the device acts as a varactor between its G and D ports. The equivalent capacitance seen from D level, as a function of the voltage difference between G and D, $V_{G,DS}$, is displayed in Fig. 1(f).

These devices present a large tuning range and low parasitic resistance [5-7]. However, they require a differential voltage between their ports that usually goes from $-V_{DD}/2$ to $+V_{DD}/2$, for devices integrated using the typical oxide thickness of the technology, or $-V_{DD}$ to $+V_{DD}$ for devices designed using a thicker oxide, which are widely used due to their reduced leakage.

D. *I-MOS varactor*

I-MOS varactors are based on classical nMOS or pMOS transistors. When the drain and the source are connected together, the body is connected to the ground (to V_{DD}, for the pMOS-based I-MOS) and a control voltage is applied to the gate, this configuration leads to an equivalent variable capacitance between its D and G ports, as for the A-MOS. This configuration is depicted in Fig. 2(a). The variable capacitance is a function of the voltage difference between the gate and the

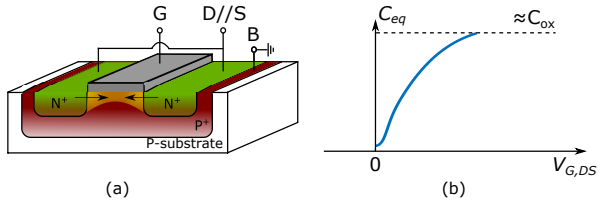

Fig. 2 (a) nMOS-based I-MOS varactor. (b) Capacitance versus $V_{G,DS}$.

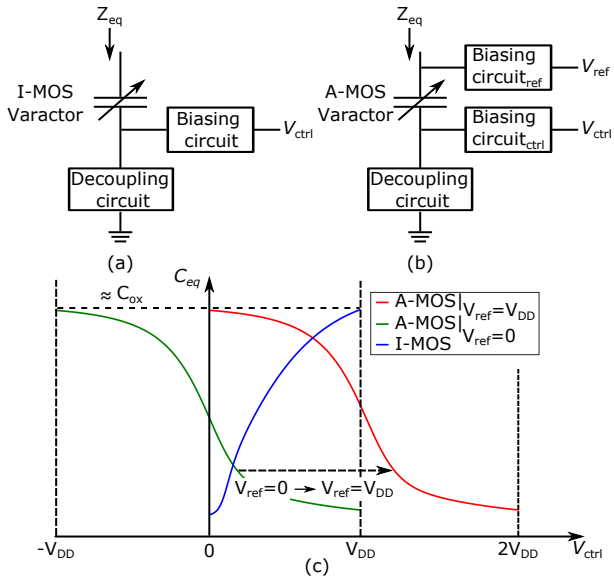

Fig. 3. (a) I-MOS varactor and the biasing/decoupling circuits. (b) A-MOS varactor and the biasing/decoupling circuits. (c) Capacitance versus V_{ctrl} for: (i) a thick-oxide A-MOS varactor with V_{ref} = 0 V (i.e. only Biasing Circuit,ctrl is necessary), (ii) a thick-oxide A-MOS varactor with V_{ref}= V_{DD} and (iii) an I-MOS varactor.

drain ($V_{G,DS}$), as shown in Fig. 2(b). The equivalent capacitance of the I-MOS varactor, as for its A-MOS counterpart, reaches a maximum approximately equal to C_{ox}.

At RF frequencies, I-MOS varactors show similar performance as their A-MOS counterparts in terms of capacitance variation, overhead area and Q-factor [6-9]. As a disadvantage, the sensitivity of I-MOS to the control voltage is greater than its A-MOS counterparts, especially to those integrated using the thick-oxide. This may lead to self-biasing issues when a large signal is applied.

E. A-MOS vs I-MOS architectures

Biasing circuitry: Let us consider a thick-oxide A-MOS varactor and an I-MOS varactor. Fig. 3(a) and 3(b) show the required biasing/decoupling circuits needed to operate the I-MOS and A-MOS architectures, respectively. For the A-MOS varactor, the designer has to choose between integrating extra circuitry to generate negative V_{ctrl} voltages or designing two biasing networks, one for V_{ctrl} and one for V_{ref}, as depicted in Fig. 3(b). Fig. 3(c) displays the capacitance variation versus V_{ctrl}. Three cases were considered: (i) a thick-oxide A-MOS with $V_{ref} = V_{DD}$ applied to one of its ports, (ii) a thick-oxide A-MOS with $V_{ref} = 0$ (i.e. only the Biasing circuit,ctrl is required) and (iii) an I-MOS. First, note that I-MOS and A-MOS varactors exhibit almost the same capacitance tuning ratio.

For the I-MOS case, only one biasing circuit is required and the applied control voltage, V_{ctrl}, ranges from 0 to V_{DD}. For the A-MOS where $V_{ref} = V_{DD}$ is applied on one of the varactor's ports ($V_{DD}/2$ for the typical-oxide architecture), the other varactor port must be fed with positive V_{ctrl} voltages. Thus, in this case, the A-MOS needs two biasing circuits. Moreover, in the case of a thick-oxide A-MOS, extra circuitry has to be integrated to generate $2 \cdot V_{DD}$. For an A-MOS with $V_{ref} = 0$, only one biasing circuit is required. However, extra circuitry has to be integrated to generate on-chip negative V_{ctrl} voltages. In any case, these issues lead to a greater area overhead, consumption and even a decrease of the varactor performance when two biasing circuits have to be integrated. In addition, integrating devices with a thick oxide often requires additional steps during the manufacturing process. Contrarily, I-MOS varactors are based on classical MOS transistors.

1) Q-factor: The Q-factor of lumped elements at mm-waves is critical due to its low value. In order to illustrate the different performance of A-MOS and I-MOS varactors in terms of Q-factor, let us consider a practical example with an A-MOS and an I-MOS designed and simulated using the PSP compact models in the STM BiCMOS 55-nm technology Process Design Kit (PDK). For a fair comparison, same capacitance tuning ratio (C_{max}/C_{min}) equal to 4.5 and same C_{min} were considered for both devices at 200 GHz. This was achieved using an A-MOS varactor with two fingers and a total length and width of 531 nm and 3.33 μm, respectively. In order to match the capacitance variation of the A-MOS, the I-MOS was also designed with two fingers and a total length and width of 1.6 μm and 7.47 μm, respectively. Note that the required area for the I-MOS is greater than for the A-MOS. However, this tends to be negligible regarding the size of the circuits in which these devices are integrated. For the sake of simplicity, ideal elements to perform biasing functions were considered to focus on the intrinsic capabilities of the varactors. Fig. 4(a) shows a schematic-level simulation of the effective capacitance of these varactors at 50, 100, 150, 200, and 250 GHz, calculated as in (1). On the other hand, Fig. 4(b) shows a schematic-level simulation of the Q-factor of these varactors for the same range of frequencies.

In Fig. 4(b), the Q-factor of the I-MOS varactor slightly increases with frequency while it decreases for the A-MOS varactor. Both devices have the same Q-factor around 120 GHz. This particular frequency only makes sense for the considered geometries and technology, but it has the interest to provide an order of magnitude. Note that, for the higher-end of the mm-wave band the reported simulations are frequency-extrapolated since the PDK is not fully mature at these high frequencies. It is evident that the A-MOS varactor is a better design option below about 50 GHz. On the other hand, above 150 GHz the I-MOS seems to clearly exhibit a superior performance. Between these two frequencies, other factors (e.g. model maturity, area overhead, biasing circuitry…) than the Q-factor only should be considered to achieve a fair comparison.

The conclusion carried out from Fig. 4(a) and 4(b) is clear for frequencies below 50 GHz and above 150 GHz. However, it is difficult to compare one frequency to another due to the fact that different Q-factor and capacitance ratio is observed. For this reason, we propose to use the following Figure-of-Merit (FoM) (2):

$$FoM = Q \cdot \left(\frac{C_{max}}{C_{min}}\right). \quad (2)$$

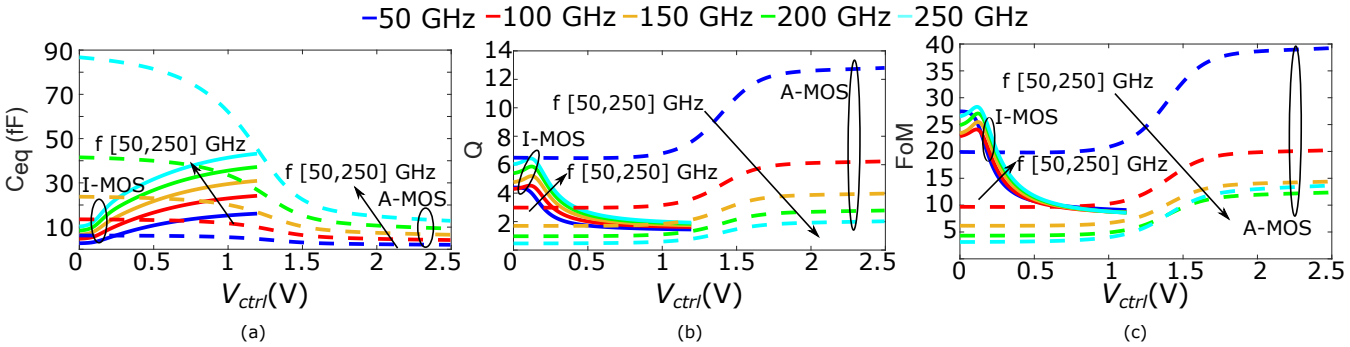

Fig. 4. Simulated performance for A-MOS and I-MOS varactors in the STM 55-nm BiCMOS technology at 50, 100, 150, 200, and 250 GHz. (a) Equivalent capacitance. (b) Q-factor. (c) Figure-of-Merit.

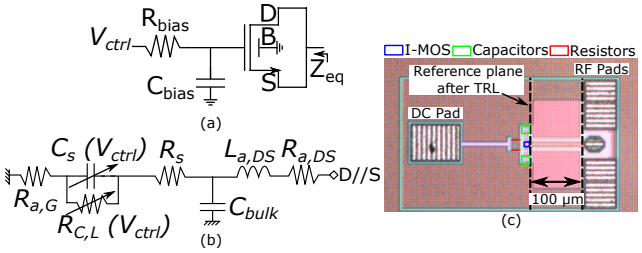

Fig. 5 (a) I-MOS varactor architecture. (b) Proposed small-signal model. (c) Micrograph of the fabricated circuit.

This metric allows evaluating the well-known trade-off between capacitance variation and Q-factor of a varactor. Figure 4(c) shows the FoM obtained for the considered I-MOS and A-MOS at 50, 100, 150, 200 and 250 GHz, respectively. This FoM shows that, for a given capacitance ratio, above around 150 GHz the FoM of the I-MOS varactor is better than the A-MOS one as expected from Fig. 4(b).

In the next section, an I-MOS varactor architecture is proposed and characterized to experimentally verify the behavior observed in Fig. 4(a) and 4(b).

III. Proposed Architecture

The proposed varactor architecture is shown in Fig. 5(a). It requires a biasing circuit to apply a DC voltage to the gate to control the varactor without interfering with the RF signal. The biasing circuit is composed by a resistor and a capacitance, R_{bias} and C_{dec}, respectively. Since the varactor is voltage-controlled through the gate, the DC biasing can be implemented with a high-value resistor R_{bias}, which presents a high impedance to RF signals. Other architectures to apply V_{ctrl}, such as inductors or quarter-wave length transmission lines could be used. However, a resistor presents the best solution for wide-band operation and low area overhead. In addition, a high-value capacitance, C_{dec}, is used for decoupling purposes. The proposed I-MOS varactor uses a traditional MOSFET, and the control voltage varies from 0 V to V_{DD}. Note that, due to the high operating frequencies, the capacitance and resistor composing the biasing circuit cannot be treated as ideal elements. These devices include parasitic effects that are non-negligible at mm-waves. In this case study, the effects of the biasing circuit itself within the varactor model were included.

A simple circuit model, depicted in Fig. 5(b), was developed to describe the behavior of the proposed device. The model is composed of a resistance $R_{a,DS}$ and an inductance $L_{a,DS}$ at drain/source level, corresponding to the resistance and inductance of the access from the top metal layer to the active region, respectively. C_{bulk} models the electrical coupling from the access interconnections and drain/source implants to the bulk silicon. R_s models the resistance of the contact and N^+-implants (i.e. drain and source). $R_{C,L}$ models the leakage, as well as the resistance of the channel. C_s models the capacitive coupling between the channel, drain and source to the gate of the MOSFET. Finally, $R_{a,G}$ models the resistance at gate level together with the parasitic resistance of the decoupling capacitance, C_{dec}. Note that the ohmic losses and parasitic capacitance occurring in the biasing circuit are embedded into $R_{a,G}$ and C_s. For the sake of simplicity but also to achieve a physics-based model, only C_s and $R_{C,L}$ depend on the tuning voltage V_{ctrl}.

IV. Experimental Results

For a proof of concept, an I-MOS varactor with a large tuning ratio C_{max}/C_{min} was designed, C_{max} and C_{min} being calculated as in (1), for the two extreme biasing voltages. As the standard impedance of RF circuits in typical applications is 50 Ω, a varactor is efficient in a circuit when its equivalent impedance is not too far from -j·50 Ω. Hence the size of the varactor was chosen so that C_{max} and C_{min} surround -j·50 Ω impedance at a working frequency of 190 GHz, i.e. $\frac{-j}{C_{min}\cdot\omega} < -j\cdot 50\ \Omega < \frac{-j}{C_{max}\cdot\omega}$.

Finally, the I-MOS varactor was designed to obtain a capacitance ratio of 4.4 along with C_{min} equal to 8 fF, leading to $\frac{-j}{C_{min}\cdot\omega} = -j\cdot 105\ \Omega$ and $\frac{-j}{C_{max}\cdot\omega} = -j\cdot 24\ \Omega$, at 190 GHz. The layout was optimized to maintain the greatest Q-factor while minimally reducing the tuning range. After a post-layout simulation, the transistor showed a C_{min} of 13 fF and a reduction of the tuning ratio to 3.2, due to parasitic capacitances. These values were obtained with a standard nMOS transistor with a width of 7.47 μm, a length of 1.6 μm and two fingers. Note that, the gate length of the designed I-MOS varactor makes it suitable for larger technology nodes. A high-resistivity polysilicon resistor was considered to achieve a DC-resistor R_{bias} was fixed to 90 kΩ. This value was achieved using two 180 kΩ resistors connected in a parallel configuration. Thanks to the high-resistivity polysilicon layer embedded in this technology, such high values could be achieved with resistors with a width and length of 0.9 μm and 27 μm, respectively. The decoupling capacitance C_{dec} was implemented using two MOM capacitors, connected in a

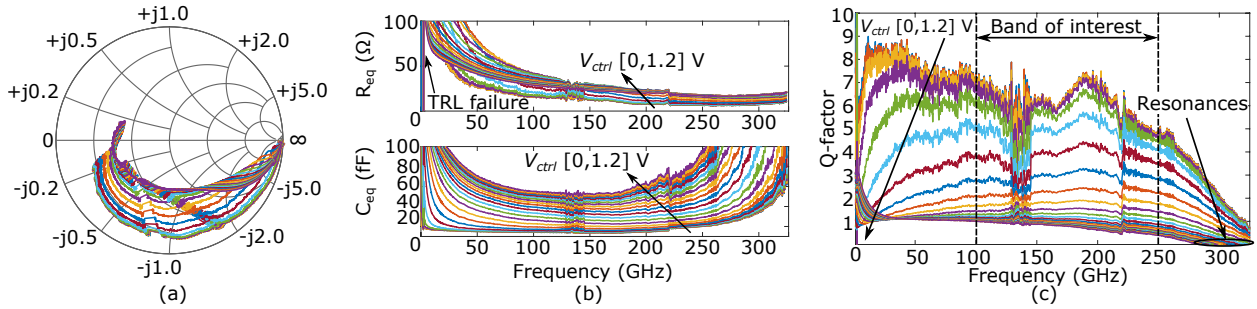

Fig. 6. Measurement results in the 1 GHz to 325 GHz band as a function of V_{ctrl} (a) S_{11}. (b) R_{eq} and C_{eq}. (c) Q-factor.

parallel configuration, to achieve a value of 200 fF. These capacitances represent a surface of 81 μm^2 each. They exhibit a -j·4.1-Ω impedance at 190 GHz, which is a compromise between a quasi-short circuit and moderate area overhead. Larger capacitances would lead to a better ground connection for the RF signal. However, due to their larger size, the magnitude of their parasitics would also be larger, possibly masking the performance of the proposed I-MOS with self-resonances appearing at lower frequencies.

The proposed device was measured using three different Vector Network Analyzers (VNAs): (i) an Anritsu VectorStar ME7838A4, from 1 GHz to 140 GHz, (ii) an Oleson extender associated to a R&S VNA, from 140 to 220 GHz, and (iii) a R&S extender associated to a R&S VNA from 220 to 325 GHz. An on-wafer Thru-Reflect-Line (TRL) calibration [10] was performed to eliminate the effect of the pads and the 100-μm microstrip feeding lines. A micrograph of the fabricated circuit is shown in Fig. 5(c) together with the reference planes after the TRL calibration.

A. TRL Calibration

The TRL is a calibration method that uses the characteristic impedance of the Line standard to set the reference impedance of the measured S-parameters. The Line standard must be sufficiently short to avoid the resonance appearing at $\theta = 180°$, where θ is the electrical length difference between the Line and Thru standards. Due to the wide frequency band considered in this work, two 50-Ω Line standards of different lengths, Line_1 and Line_2, respectively, were integrated on-wafer. Line_1 and Line_2 were designed using a microstrip line. Their extra lengths (as compared to the Thru standard) were set to 350 μm and 170 μm, respectively. Line_1 was used to perform the calibration from 1 GHz to 140 GHz whereas Line_2 was used for the 140 GHz to 325 GHz band. Line_1 exhibits an extra electrical length of 0.8° at 1 GHz and 109° at 140 GHz. On the other hand, Line_2 exhibits an extra electrical length of 53° at 140 GHz and 123° at 325 GHz. Note that, while the extra electrical length of Line_2 provides with enough margin to ensure proper reading of the Line's characteristic impedance, this is not applicable for the Line_1. Below 1 GHz, Line_1 has an electrical length that is close to the sensitivity of the VNA, which is around 0.06 °, and the measurements close to this frequency were certainly affected by a non-ideal calibration. Nevertheless, the two-Line approach ensures almost complete coverage throughout the measured frequency band.

B. Results

Fig. 6(a) presents a Smith's chart of S_{11} after TRL calibration. It displays 25 traces corresponding to the V_{ctrl} tuning voltage in steps of 50 mV, from 0 to 1.2 V. At 190 GHz, S_{11} magnitude varies from -1.2 dB to -6.9 dB and its phase varies from -80° to -144°, respectively. Fig. 6(b) displays the series equivalent capacitance and resistance, C_{eq} and R_{eq}, throughout the 1 GHz to 325 GHz frequency band for a V_{ctrl} step of 50 mV. The equivalent series capacitance was calculated as in (1). On the other hand, the equivalent series resistance reduces to $R_{eq} = \Re(Z_{eq})$. Around 1 GHz, the vertical traces on R_{eq} indicate that the TRL is no longer valid since the sensitivity becomes really poor. Note that beyond 250 GHz, C_{eq} shows a dispersive behavior. This is due to the fact that (1) is a calculation of the equivalent capacitance. Hence, when using this equation near resonances, the equivalent capacitance tends to the infinity, since $\Im(Z_{eq}) \to 0$.

At 190 GHz, the measured varactor presents an overall equivalent capacitance varying from 13 fF to 54 fF. The average slope is equal to 26 aF/mV, presenting low sensitivity to the biasing voltage variations, since C_s has a low sensitivity to the tuning range, as it will be shown at the end of this section. This is interesting for practical applications. Fig. 6(c) shows the extracted Q-factor for different values of V_{ctrl} in the 1 GHz to 325 GHz frequency band. The Q-factor is relatively flat throughout the 140-220 GHz band, reaching a maximum value of 7 around 190 GHz. Above 190 GHz, the Q-factor decreases, and resonances appear beyond 290 GHz, thus the extraction of C_{eq} above the resonance frequency would lead to negative values. Below 190 GHz, the effect of the relatively-low quality factor of C_{dec} in series with the I-MOS varactor limits the increase of its Q-factor. This can be easily explained by the degradation of the MOM capacitor quality factor at mm-wave frequencies. For instance, at 140 GHz, the measured quality factor of a MOM capacitor in this technology is around 10 [11]. Thus, it can be expected a quality factor around 20 at 70 GHz. At 70 GHz, the maximum measured Q-factor of the varactor is around 8, which means that the intrinsic varactor's Q-factor, disregarding the MOM capacitance, is around 14. On the other hand, for frequencies below 50 GHz, the low Q-factor shown in Fig. 6(c) can only be explained by a low value of the intrinsic varactor's Q-factor, since the quality factor of C_{dec} is much higher.

Table I shows the state-of-the-art of mm-wave CMOS varactors reported in the literature so far. The varactor presented in this work shows the greatest tuning ratio

TABLE II
STATE-OF-THE-ART MM-WAVE VARACTORS

Ref	Type	Frequency (GHz)	Q-factor	$\frac{C_{max}}{C_{min}}$	FoM
[5]	A-MOS	100	10	1.4	14
[12]	A-MOS	60	9	2	18
[13]	A-MOS	24	100	1.6	160
This work	**I-MOS**	**190**	**7**	**4.2**	**29**

(C_{max}/C_{min}) while maintaining a high Q-factor and FoM, considering the very high working frequencies.

In order to integrate the developed varactor into a conventional design flow, an empirical model was developed by fitting the proposed small signal model in Fig. 5(b) to the measurement results. The varactor presents an $R_{a,DS}$ and $L_{a,DS}$ of 0.5 Ω and 7.5 pH, respectively. R_s is equal to 12 Ω. C_{bulk} and $R_{a,G}$ are equal to 6 fF and 8 Ω, respectively.

The variation of $R_{C,L}$ and C_S as a function of the control voltage V_{ctrl} was modeled by empirically fitting the measurements using standard regression functions. $R_{C,L}$ was coded using a 4^{th}-order Gaussian and C_s was coded using a 3^{rd}-order Fourier's series. The modeled variation of $R_{C,L}$ and C_s versus V_{ctrl} is plotted in Fig. 7(a). $R_{C,L}$ ranges between 1.6 kΩ and 67 Ω, and C_s ranges from 9 to 34 fF. The behavior of these parameters is consistent with the expected electrical response of the structure. When the V_{ctrl} is low, the channel is not formed and only the losses from leakage currents are present, thus leading to a high-value resistor and a low-value capacitance. As the V_{ctrl} increases, the channel begins to form, thus increasing the capacitance between drain/source and gate. The formation of the channel with the increase of V_{ctrl} leads to a decrease of $R_{C,L}$, thus increasing the losses.

In Fig. 7(b), the values of R_{eq} and C_{eq} extracted from measurements are compared to the electrical model proposed in Fig. 5(b) for working frequencies equal to 100, 150, 200 and 250 GHz, respectively. A good agreement between measurement results and model is observed for frequencies above 100 GHz. Below this frequency, the model shows some disagreement for the estimation of R_{eq}. This can be easily explained as none of the model elements include frequency dependent behaviors. Hence, frequency-dependent effects such as the skin effect or the Non-Quasi-Static effect, which were present when the model parameters were optimized between 100 GHz and 250 GHz, will overestimate e.g. the losses at lower frequencies. However, developing a small-signal model the between 1 to 325 GHz is out of scope for this paper.

V. CONCLUSION

In this work, a simple I-MOS varactor architecture for high-frequency applications has been proposed. The operation of the proposed I-MOS has been described and a small-signal model has been developed. Experimental results in the frequency band from 1 GHz to 325 GHz have shown interesting electrical performance, especially beyond about 100 GHz, thus highlighting the interest of the proposed I-MOS varactor for mm-wave applications. The proposed device offers a large variation of the capacitance (greater than 4) and a quality factor that reaches 7 at 190 GHz. To sum up, the proposed I-MOS varactor presents many advantages as compared to its A-MOS counterpart, such as: (i) availability and compatibility with industrial Design kits, (ii) reliability of the models, (iii) high tuning range, (iv) no extra digital circuitry needed for biasing purposes, and (v) higher quality factor for frequencies above about 100 GHz.

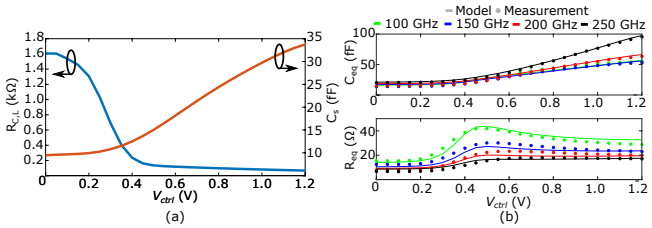

Fig. 7. (a) Modeled variation of $R_{C,L}$ and C_s versus V_{ctrl}. (b) Measured and modeled C_{eq} and R_{eq} variation at 60, 100, 150, 200, and 250 GHz as a function of V_{ctrl}.

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