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A non-intrusive machine learning-based test methodology for millimeter-wave integrated circuits

Florent Cilici, *Student Member IEEE*, Manuel J. Barragan, *Member IEEE*, Estelle Lauga-Larroze, Sylvain Bourdel, *Member IEEE*, Gildas Leger, Loïc Vincent, and Salvador Mir, *Member IEEE*

Abstract—In this manuscript, we leverage the power of machine learning algorithms to propose a test methodology for mm-wave integrated circuits. The proposed test strategy is based on identifying the main process degradation mechanisms in a particular Device Under Test (DUT) and then designing dedicated process monitor circuits to characterize this degradation and infer the DUT performance. The resulting process monitors do not load or couple to any of the DUT nodes and the methodology can be adapted to any mm-wave device without complex co-design. The proposed test methodology is illustrated on a set of 21 fabricated samples of a 65 GHz PA designed in STMicroelectronics 55 nm CMOS technology.

Index Terms—mm-wave IC test, machine learning-based test, non-intrusive test, process monitor circuits, BIST, Design-for-Test.

I. INTRODUCTION

Continuous demand for high data-rate transmissions and high-speed systems has led the industry towards mm-wave frequencies. This trend is supported by the continuous scaling of CMOS technologies that enables the fabrication of transistors with transition frequencies higher than 200 GHz. While such advanced fabrication processes allow the integration of mm-wave circuits, they are also especially prone to large process variations that may result in substantial performance degradation and low fabrication yield. Hence, integrated mm-wave circuits require extensive production testing to evaluate the performance of the fabricated parts. However, testing mm-wave circuits in the production line is especially demanding since test procedures often involve complex at-speed measurements that require costly dedicated Automated Test Equipment (ATE) and long test times.

Recent works have focused on reducing the complexity and cost of testing RF and mm-wave circuits by moving some of the tester functionalities into the Device Under Test (DUT), in such a way that the device becomes self-testable. This is the key concept behind the so-called Built-In Self-Test (BIST) techniques that may reduce this way the overall test cost by taking test into consideration at the design stage.

Several BIST implementations targeted at different RF and mm-wave circuit families have been presented in the last

few years. Thus, a classic RF/mm-wave test method that has been implemented on chip is the loop-back test, that gives a convenient way to test a complete transceiver by connecting the transmitter output to the receiver input [1], [2]. Despite its apparent simplicity, it may incur a noticeable area overhead, require careful co-design of DUT and test circuitry and may not be able to fully differentiate transmitter and receiver impact in the overall performance.

Integrated VNAs for on-chip testing have been presented in [3]–[5]. The work in [3] presents a dual-port 50-100 GHz VNA that can be used to perform measurements on a wide variety of mm-wave circuits or to provide BIST capabilities, while the work in [4], [5] proposes an on-chip I/Q receiver for the evaluation of the S-parameters of phased-array receivers and transmitters. Although promising silicon results have been reported, the complexity of the on-chip instrumentation is high, which requires careful co-design with the DUT and increases the design effort.

On the other hand, simple on-chip DC-sensors, such as power detectors, peak detectors, envelope detectors, temperature sensors, etc. have been also proposed for simplifying the read out of high-frequency signals [6]–[8]. These sensors are often used in combination to machine learning algorithms with the goal of simplifying (or avoiding the need of) high-frequency on-chip measurements [9]–[12]. These works replace the measurement of complex RF specifications by simpler low-frequency signatures obtained from the sensors. Then, a regression function obtained using machine learning algorithms is used to map the signatures to the DUT performance. However, since these sensors usually tap into critical circuit nodes of the DUT, they usually require a careful co-design to avoid the degradation of the DUT performances.

Although test cost may be significantly reduced, implementing BIST techniques for mm-wave circuits is still a challenging task due to the excessive design effort of co-designing DUT and test circuitry without degrading the device performance. The feasibility region in the design space may be significantly reduced by the introduction of BIST and the performance may even become unreachable in the worst cases. The recently proposed non-intrusive indirect test paradigm may be a solution to the aforementioned issues. The main concept was first proposed in [13] for mixed-signal test applications, and later extended to the RF and mm-wave domains in [14]–[17]. This test strategy proposes to integrate a set of non-intrusive process monitor circuits (also called process variation sensors, or non-intrusive sensors) in the close proximity of the DUT but not electrically connected to it, in such a way that both

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the DUT and the monitors will undergo the same process variations. Then, a machine learning regression model is used to infer the performance of the DUT from the outputs of the process monitors. Thus, this non-intrusive test is aimed at detecting excessive process variations that may degrade the functionality of the DUT. Moreover, it has the additional advantage of not loading the DUT nodes, so no complex co-design of DUT and sensors is needed. Furthermore, the output of the process monitor circuits is usually DC or low-frequency which eliminates the need of costly high-frequency testers.

Unfortunately, recent attempts to extend the non-intrusive test strategy to the mm-wave domain show serious practical limitations [16], [17]. Thus, the proposal in [16] is only targeted at the estimation of return loss in a 80 GHz LNA, while the work in [17] is not able to estimate some of the S-parameters of a 60 GHz LNA. Designing appropriate non-intrusive sensors to estimate the missing specifications is highlighted as a key open problem in both works. Moreover, no silicon results have been yet reported to experimentally validate this test strategy in the mm-wave domain.

In [18] we presented a first attempt at systematizing the design of an indirect test program for mm-wave integrated circuits. However, our methodology assumed that Monte Carlo process variation models are available for all the elements in the DUT. This is not usually the case in mm-wave integrated circuit designs, where passive components such as transmission lines, couplers, baluns, etc. are often custom-built in the Back End of Line (BEOL) of the technology. In the present manuscript, we extend our previous work in [18] to cover also custom-built passive devices. This way, we define a systematic methodology for designing an indirect test program (including the definition and design of the necessary process monitors and the set of necessary indirect measurements) for a generic mm-wave integrated circuit. Moreover, our methodology is supported by experimental results in a proof-of-concept case study consisting in a set of 65 GHz Power Amplifiers fabricated in STMicroelectronics 55 nm CMOS technology. To our knowledge, this is the first time that the non-intrusive test strategy of mm-wave integrated circuits is validated with silicon results.

The rest of this manuscript is organized as follows. Section II details our non-intrusive indirect test strategy and the proposed methodology for non-intrusive sensors design. In Section III the presented methodology is illustrated with a proof-of-concept step-by-step application on a 65 GHz PA designed in a CMOS 55 nm technology. Section IV validates the proposed test strategy based on experimental results from 21 fabricated samples of the 65 GHz PA. Finally, Section V summarizes the main contributions of this work and outlines future research in this line.

II. NON-INTRUSIVE TEST PROGRAM GENERATION FOR MM-WAVE INTEGRATED CIRCUITS

A. Problem statement

Let us consider a mm-wave integrated circuit that may contain both active and passive components modeled in the design kit of the technology and full-custom passive devices

built in the BEOL of the technology. Let us consider as well that this mm-wave integrated circuit has m performances $\{P_1, \dots, P_m\}$ that have to be characterized during production test. The goal of our methodology is to propose a non-intrusive test program containing: a) a set of non-intrusive process monitors, and b) a set of n low-frequency measurements, that we will denote as signatures $\{S_1, \dots, S_n\}$, extracted from these non-intrusive process monitors. The key idea in the methodology is that the designed signatures will capture the main causes of performance degradation due to process variations, in such a way that we can build a machine learning regression model, f , in order to accurately infer the circuit performances from the measurement of the signatures as,

$$f : [S_1, \dots, S_n] \rightarrow [P_1, \dots, P_m]. \quad (1)$$

In the production line, this indirect test protocol is developed in two stages. In a first stage, usually called the training stage, both the signatures and the performances are measured for a reduced set of fabricated devices. These measurements are used for training a machine learning regression model. Then, in the second stage, usually called the testing stage, for the rest of produced devices only the signatures are measured and the device performances are inferred using the previously trained regression model.

As a starting point, the proposed methodology assumes that we have access to: a) the netlist and layout of the mm-wave integrated circuit, and b) the technological information available in the design kit of the technology, including the Monte Carlo process variation models and information about the BEOL layers (i.e., thickness, dielectric constant, fabrication corners, etc.). No particular assumptions are made about the nature of the mm-wave device itself.

It has to be noticed that the resulting test program is specifically tailored to be sensitive to performance degradation due to process variations. Local degradation effects such as spot defects cannot be detected by non-intrusive process control monitors. Nevertheless, this limitation can be eventually overcome by complementing the resulting test program with other well-known defect-based test techniques [19], [20].

The proposed methodology is schematically illustrated in Fig. 1 and it is divided into two main steps. The first step aims at finding the root causes of performance degradation in the simulation environment. The second step is aimed at designing process-aware sensors that are sensitive to the identified set of degradation root causes. Let us describe these two steps separately.

B. Step 1: Assessment of parametric performance variation root causes

This first step in our methodology intends to find which of the components in the DUT have the most relevant contributions to the overall parametric performance variation of the DUT. As mentioned above, in a generic mm-wave DUT we can distinguish two families of components: standard components that are modeled in the Process Design Kit (PDK) of the technology and full-custom passive components built by the designer in the technology BEOL. In the following, as it is

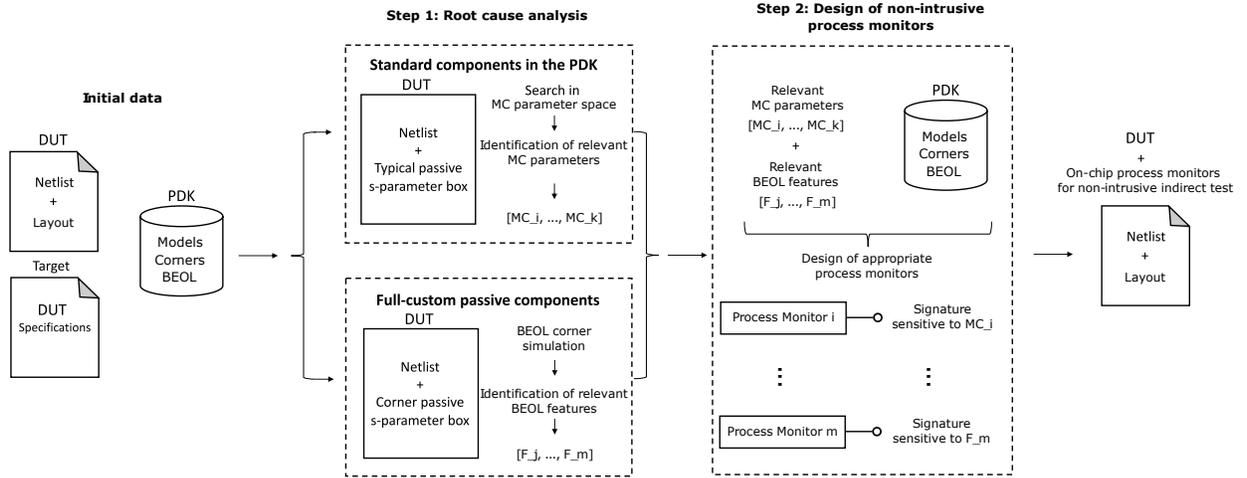


Fig. 1. Conceptual block diagram of the proposed methodology for the generation of non-intrusive indirect test using on-chip process monitors.

usual practice in mm-wave designs, we assume that we have a netlist of the DUT where all custom-built components are replaced by a box of S-parameters obtained by electromagnetic simulation. The contributions of these two families of components to the DUT performance degradation are considered separately.

1) *Performance degradation due to standard components process variations:* For the degradation of the DUT performance due to process variation of components modeled in the PDK of the technology, we actually have direct access to the root causes of variation in the simulation environment, that is, the set of Monte Carlo (MC) process variation parameters defined in the PDK. Intuitively, it would be possible to explore the set of MC parameters to determine, in the design stage, which are the most relevant parameters for explaining the observed performance degradation. However, in practice, performing this exploration in an efficient way may be challenging since current nanometric technologies usually include a few hundred MC parameters in the PDK process variation models. In the field of statistics, this can be seen as a classical feature selection problem.

A feature selection problem can be formalized as follows: given a set of random variables, usually called features (in our case, the set of MC parameters) and a set of target variables (in our case, the set of DUT performances), find the smallest subset of features required for inferring the target variables (using a machine learning regressor) while minimizing the regression error. In other words, a feature selection algorithm identifies the subset of features that are actually relevant for explaining the variation observed in the target variables. A wide variety of feature selection algorithms are available in the literature. The interested reader is referred to [21] for an excellent introduction to this topic. Although a full description is out of the scope of this manuscript, in essence there are two main families of feature selection algorithms: filters and wrappers. A filter selects or discards features based on a statistical metric, for instance, based on its correlation to the target performances. A wrapper is an optimization loop that iteratively searches for the optimum subset of features that

minimizes the regression error. Generally, filters are time-efficient but they tend to capture only the most significant variation components. On the other hand, wrappers offer an accurate evaluation of the prediction error (since it is actually computed in each iteration of the optimization loop) but the computational burden of the search in the space of features may be prohibitive, especially when the cardinality of this set is high. Some of the authors of this manuscript proposed a hybrid feature selection technique in [18], [22] –the so called Brownian distance correlation-directed search– that combines the advantages of both filters and wrappers. This technique guides the search in the input signature space based on the dynamic evaluation of a correlation metric. In this manuscript we adapt this technique for an efficient identification of the variation root-causes to the challenging case of mm-wave circuits, which are very sensitive to process variability.

The proposed feature selection algorithm, conceptually represented in Algorithm 1, is an iterative search guided by the distance correlation metric [23]. The algorithm starts by generating a data set of MC instances of the DUT. In this DUT instances, all full-custom passive components are replaced by a box of S-parameters representing its operation and performance at the typical corner. The generated DUT instances are then simulated at the operation frequency using standard simulation testbenches for evaluating the main performance figures of the DUT. The set of MC parameters associated to each MC instance of the DUT is also stored. Then the algorithm employs the distance correlation metric [23] to rank the MC process parameters with respect to their correlation to the target performance. An initial regression model is then built to predict the target performance from the best correlated MC parameter. The algorithm continues by computing the regression error for each of the DUT instances and then it ranks the remaining MC process parameters with respect to their distance correlation to the regression errors. The distance correlation is actually computed between the augmented input space –that is, the matrix of previously selected MC process parameters plus each new candidate– and the vector of regression errors. In this way, multi-parameter contributions

Algorithm 1 Exploring the space of MC process parameters using a Brownian Distance Correlation-Directed Search

- 1: Generate a set of MC instances of the DUT. Generate a data set containing the target performance and the set of MC process parameters for each MC instance.
 - 2: Compute the distance correlation of all individual MC process parameter with the performance and add the associated most correlated process parameter to the input space
 - 3: **while** *continue* **do**
 - 4: Train a model mapping the input space onto the performance
 - 5: Compute the residues of the model
 - 6: Compute the mean square of the residues (the mean square error of the model fit)
 - 7: **if** The mean square error is less than or equal to a given threshold **then**
 - 8: *continue* $\leftarrow 0$
 - 9: **else**
 - 10: *continue* $\leftarrow 1$
 - 11: Compute the multivariate distance correlation of the remaining MC process parameters with the residue: the distance correlation is computed between the matrix of previously selected MC process parameters plus each new candidate and the residue of the previous fit
 - 12: Add the most correlated MC process parameter to the input space
 - 13: **end if**
 - 14: **end while**
 - 15: **return** the input space (the most significant MC process parameters) and the mean square error of the fit
-

to performance degradation are naturally taken into account during the search. Then, the most correlated parameter is added to the set of selected relevant MC parameters and the process is iterated. Each iteration of the algorithm should identify a MC parameter that adds relevant information that improves the regression error. The process continues until the regression error is below a pre-defined threshold.

A key aspect of the previous search algorithm is the concept of correlation, that is based on the evaluation of the distance correlation. This multidimensional non-linear correlation metric allows to detect complex non-linear multi-parameter dependencies between the set of candidate MC parameters and target performances. The reader is referred to Appendix A for a brief introduction to the distance correlation statistics. It is also worth noticing that the iterative nature of the algorithm makes the search computationally feasible even for high-dimensionality spaces, at the cost of reducing the search space. This is a common trade-off in feature selection algorithms. Indeed, the goal of a feature selection technique is to find a good-enough set of parameters, that is, a set that complies with a desired target for the prediction error, with a reasonable computational effort. The goal is not to find the global optimum that minimizes the prediction error, which would be computationally unfeasible for the majority

of practical applications.

2) *Performance degradation due to full-custom component parametric variations*: Full-custom passive components are usually designed using electromagnetic simulation tools in the typical fabrication corner of the technology. In order to evaluate the degradation of the DUT performance due to process variations of full-custom components, we rely on the fabrication corner information available in the PDK. In this line, we assume that we have access to the information about fabrication corners for the different layers of the BEOL. This includes BEOL features such as thickness and dielectric constant variations among corners for dielectrics, and thickness and conductivity variations among corners for metal layers. With this information, corner passive components can be generated using an electromagnetic simulation tool. The generated corner passive components can be then introduced in the DUT netlist and simulated in the electrical domain.

Ideally, the aforementioned procedure could be introduced in a Monte Carlo simulation loop in which a random set of BEOL features are sampled for each iteration and simulated. In that case, BEOL features could be considered as additional Monte Carlo technological parameters that could be integrated in the same feature selection analysis described above for PDK devices. Unfortunately, the computational burden of electromagnetic simulation makes this direct approach unfeasible even for simple circuits. Instead of replicating Monte Carlo simulation at the electromagnetic level, we propose a simplified analysis based on the sensitivity of the DUT performance to each feature. This analysis has the goal of determining which are the most relevant BEOL variability features for predicting the performance of the DUT. In this line, we will introduce a scalar metric, $\Delta P(F)$, that will be used as a proxy of the sensitivity. This metric can then be used to rank the relevance of each BEOL variability feature according to their impact to the DUT performance. The proposed $\Delta P(F)$ metric is defined as the normalized variation of the target performance P when we vary a given BEOL feature F between its minimum, typical and maximum technological corners while all other BEOL features are kept at their typical values, that is,

$$\Delta P(F) = \frac{|P(F_{typ}) - P(F_{min})| + |P(F_{typ}) - P(F_{max})|}{P(F_{typ})} \quad (2)$$

where $P(F_{typ})$, $P(F_{min})$, and $P(F_{max})$ correspond to the DUT performance obtained by electrical simulation when the BEOL feature F is set to its typical, minimum and maximum fabrication corner, respectively.

The proposed sensitivity metric can be easily extended to take into account multi-parameter variation by replacing feature F by a vector of features $\mathbf{F} = (F_1, \dots, F_k)$ in such a way that we can define our scalar metric ΔP as

$$\Delta P(\mathbf{F}) = \frac{|P(\mathbf{F}_{typ}) - P(\mathbf{F}_{min})| + |P(\mathbf{F}_{typ}) - P(\mathbf{F}_{max})|}{P(\mathbf{F}_{typ})} + \frac{\delta_{min,max}(\mathbf{F})}{P(\mathbf{F}_{typ})} \quad (3)$$

where $P(\mathbf{F}_{typ})$, $P(\mathbf{F}_{min})$, and $P(\mathbf{F}_{max})$ correspond to the DUT performance obtained by electrical simulation when the BEOL

features in vector \mathbf{F} are set to their typical, minimum and maximum fabrication corner, respectively, and $\delta_{min,max}(\mathbf{F})$ includes cross-variation terms. As an example, if we consider bi-variate contributions, then $\delta_{min,max}(\mathbf{F}) = |P(\mathbf{F}_{typ}) - P(F_{1,min}, F_{2,max})| + |P(\mathbf{F}_{typ}) - P(F_{1,max}, F_{2,min})|$.

Clearly, even with the introduction of this simplified sensitivity metric, a blind evaluation for exploring all the defined BEOL features in a given technology would require a number of electromagnetic simulations that would still be prohibitively high, especially if multi-parameter variations are considered. In order to further reduce the number of necessary simulations, this evaluation should be guided using expert design knowledge on the particular custom passive component. Typically, only a limited subset of BEOL features will have an impact on its performance, which may significantly reduce the simulation effort for this evaluation. Thus, analytical design equations that link the geometry of the passive component to its electromagnetic behavior may be used to quickly identify the subset of candidate BEOL features for which the ΔP metric should be computed. In this line, a variety of analytical models can be found in the literature for typical passive components in millimeter-wave circuits such as spiral inductors [24], slow-wave coplanar waveguides [25], MIM capacitors [26], microstrip lines [27], [28], interdigitated capacitors [29], etc.

C. Step 2: Design of non-intrusive process variation sensors

Once the previous step has been completed, we have identified a set of MC parameters and BEOL variation features that are relevant for explaining the degradation of the DUT performance due to process variations. It is worth noticing that even if the DUT operates at mm-wave frequencies, the identified parameters are frequency-independent physical properties (e.g., metal thickness, gate oxide thickness, dopant concentration, etc). Hence, it would be possible to propose low-frequency indirect tests that target the measurement of these physical properties. Given that the at-speed DUT performance is correlated to the identified parameters, if we are able to propose low-frequency measurements (i.e., signatures) correlated to the same identified parameters, it follows that the at-speed performance and the low-frequency signatures would also be correlated and hence we should be able to infer one from the other. Since the original performance simulation was performed at the DUT operation frequency, the effects of high-frequency operation are naturally taken into account within the accuracy range of the employed simulator and simulation models.

The next step in the proposed methodology is then to design simple tests that target the measurement of the identified parameters so that they can be used as signatures for predicting the DUT performance. In this line, we will rely on non-intrusive process monitor circuits sensitive to the identified parameters.

For the identified MC parameters, we make use of the information in the PDK of the technology to determine their physical meaning. Together with the identified BEOL features, this information can be used to guide the design of appropriate

non-intrusive process monitors. Our goal is to devise simple circuitry that generates a signature sensitive to the identified degradation mechanisms. The designed process monitors and their associated signatures may be stored in a library for further reuse. This way, if we were to design a test program for a different DUT in the same technology, it would be possible to reuse the same process monitors and signatures already designed. Actually, if the library covers the complete set of process variation parameters, designing the test program would be reduced to choosing the appropriate set of process monitors and signatures for a particular set of identified relevant DUT parameters.

The final result of the proposed methodology for non-intrusive indirect test of mm-wave integrated circuits is the set of non-intrusive sensors and the set of measurements (i.e., the signatures associated to the sensors) that can be used for the regression of the DUT performances.

III. CASE STUDY

A. Device Under Test

As a proof-of-concept, this section details a case study application in order to illustrate the proposed test generation methodology. The selected DUT is a class A one-stage 65 GHz Power Amplifier designed in STMicroelectronics 55 nm CMOS technology. This circuit has been chosen as a test vehicle since it is highly sensitive to process variation of both active and passive parts. The transistor level schematic of the DUT is displayed in Figure 2. The PA input and output nodes are matched to a 50Ω impedance at 65 GHz using full-custom microstrip line stubs. The microstrip lines and T-junctions were designed and simulated using the electromagnetic simulator Momentum. The matching network structure is based on shunt stubs with MOM capacitors to synthesize the shunt (i.e., a low impedance at the working frequency). These cells also play the role of decoupling cells for the power supplies to filter DC bias voltage variations.

The goal of this proof-of-concept case study is to design a complete non-intrusive indirect test protocol for the test of the PA main specifications. Namely, we target the test of the PA S-parameters (S_{21} , S_{11} and S_{22}), saturation power (P_{sat}), input and output 1-dB compression point (ICP_{1dB} and OCP_{1dB} , respectively), maximum power added efficiency (PAE), saturation output power (P_{sat}) and current consumption (I_{DC}). That is, we target the design of non-intrusive process monitors and a set of associated simple measurements that allows the prediction of the PA specifications using a machine learning regression model. In the following subsections, the methodology proposed in the previous section is applied step by step.

B. Step 1: Assessment of parametric performance variation root causes

As described above, at the design stage the methodology distinguishes between degradation causes due to process variations of standard components modeled in the PDK of the technology and BEOL variations of full-custom passive components.

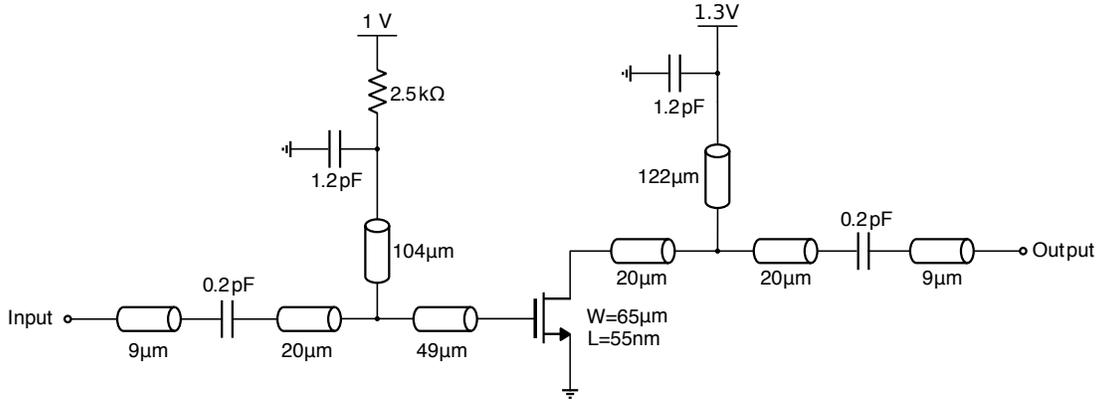


Fig. 2. Transistor level schematic of the Power Amplifier under test.

1) *Performance degradation due to standard components process variations*: Firstly, all full-custom passive devices in the DUT netlist are replaced by S-parameter boxes, obtained by electromagnetic simulation in Keysight Momentum, describing their performance in the typical corner. A data set of 1000 instances of the resulting PA was then generated using the Monte Carlo models in the PDK of the technology. These instances were simulated using the SpectreRF simulator to extract the PA performances at the operation frequency of the DUT. The PA is simulated using standard simulation test benches for performance characterization. Thus, we employed a small signal test bench for characterizing S -parameters, large signal test benches for P_{sat} , PAE and compression point, and a DC test bench for I_{DC} characterization.

The MC simulation of the DUT in the 55 nm CMOS technology includes more than 500 independent process parameters. As described in the previous section, we explore the space of MC parameters to find the root causes of performance degradation. For performing this search, we rely on the proposed Brownian distance correlation-directed search. A simple perceptron Neural Network implemented in Matlab is used as the machine learning regression algorithm for predicting the PA performances during the search.

As an application example, the procedure is fully detailed for the small signal gain (i.e., S_{21}) as the target specification of the PA under test. The procedure can be then iterated for the rest of the specifications. Thus, Fig. 3 shows the Root-Mean-Square (RMS) error and the maximum absolute error of the PA gain prediction in an independent set of PA instances, as a function of the number of MC process parameters selected by the search algorithm. In each iteration, our search algorithm identifies a new MC parameter (by order of relevance) that is added to the set of selected relevant parameters for predicting the target performance. As it can be seen, after 16 iterations the search identified the most significant 16 MC process parameters that allow the prediction of the PA gain with an error below 0.01 dB. For confidentiality reasons we cannot disclose the actual names of the MC parameters in the PDK. Instead, we provide a label that describes its physical meaning. Thus, parameters labelled as $poly_i$ refer to variations affecting to the polysilicon transistor gate, MOS_i refers to other MOS

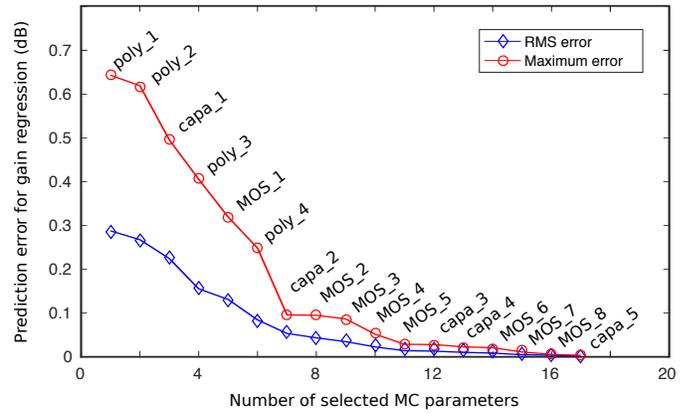


Fig. 3. RMS and maximum error for the prediction of the PA small signal gain as a function of the number of selected MC parameters. Labels associated to each datapoint represent the selected MC process parameter. Parameters labelled as $poly_i$ refer to variations affecting to the polysilicon transistor gate, MOS_i refers to other MOS transistor features, and $capa_i$ refers to variations of MOM capacitor features.

transistor features, and $capa_i$ refers to variations of MOM capacitor features.

Given the topological simplicity of the DUT, it is possible to interpret the results from an electrical point of view. Thus, the set of selected parameters basically reflect a trade-off between load adaptation, electrical losses and transistor operation point, which is in the know-how of an expert mm-wave designer. However, in this case they were obtained automatically by the proposed search algorithm, without the need of previous electrical knowledge of the PA.

This process is then iterated for the rest of the PA specifications. The results are listed in Table I. This table shows the sets of identified MC parameters that are relevant for the prediction of each PA specification, ranked by relevance. For each specification, the selection of MC parameters has been stopped when the prediction error does not improve significantly by incorporating additional parameters. As it can be seen, the degradation of the selected specifications due to process variations is dominated by a subset of only 16 different parameters.

2) *Performance degradation due to full-custom component parametric variations*: This step requires knowledge of the

TABLE I
IDENTIFIED RELEVANT MC PARAMETERS FOR THE PREDICTION OF THE PA SPECIFICATIONS

Specification	Identified Monte Carlo parameters (ranked by relevance)
Gain (S_{21})	poly_1, poly_2, capa_1, poly_3, MOS_1, poly_4, capa_2, MOS_2, MOS_3, MOS_4, MOS_5, capa_3, capa_4, MOS_6, MOS_7, MOS_8
S_{11}	poly_1, poly_2, poly_3, capa_1, poly_4, MOS_1, capa_2, MOS_4, MOS_2, capa_4, MOS_7
S_{22}	poly_1, poly_3, poly_2, MOS_1, capa_1, MOS_2, poly_4, capa_2, MOS_4, capa_4, MOS_7, MOS_3, MOS_8, MOS_5, capa_3, MOS_6
Power Added Efficiency, PAE	poly_1, capa_1, poly_3, MOS_1, poly_2, capa_2, MOS_8, capa_3, MOS_5, MOS_6, capa_5, MOS_4, MOS_7
DC current, I_{DC}	poly_3, MOS_8, MOS_4, MOS_5, MOS_3
Input referred 1 dB Compression point, ICP_{1dB}	poly_1, poly_2, MOS_1, capa_1, poly_1, poly_3, MOS_2, MOS_4, capa_4, MOS_7, capa_2, capa_3, MOS_6, MOS_8, MOS_3
Output referred 1 dB Compression point, OCF_{1dB}	poly_1, capa_1, poly_3, capa_2, poly_2, MOS_3, MOS_4, capa_4, MOS_5, poly_4, MOS_7, capa_5, MOS_1, capa_3, MOS_8
Saturation output power, P_{sat}	capa_1, poly_1, poly_3, MOS_1, capa_2, poly_2, MOS_2, MOS_4, MOS_8, MOS_3, poly_4, MOS_5, capa_3, capa_4, MOS_6, MOS_7

BEOL feature variations described in the PDK of the technology. In the selected 55 nm CMOS technology, the BEOL is composed of 8 metal layers. Metal layers 1 to 5 are thin, metal layers 6 to 7 are thick and layer 8 is an ultra-thick metal layer. The full-custom transmission lines in the PA under test employ the last metal layer for the signal while the metal 1 layer is used for the ground plane, as represented in Fig. 4. Metal layers 2 to 7 are dummy metal structures connected to ground that are needed for respecting the local metal density rules of the technology.

Following the proposed methodology for analyzing the root causes of performance degradation related to full-custom components, we should vary the BEOL features (e.g., metal thickness, dielectric constant, metal conductivity, etc.) according to the PDK of the technology. Then we build S-parameter boxes for each corner of the passive components using an electromagnetic simulator, introduce these variations into the PA netlist and compute the associated ΔP metrics using an electrical simulator. However, even for our simple circuit, this is clearly computationally unfeasible if the complete set of BEOL features and all possible multi-variate contributions have to be considered. Instead, the procedure can be greatly simplified by using some design knowledge on the custom components.

In our case we take advantage of the theoretical equations proposed in [27], [28], [30] for microstrip lines design in order to simplifying the number of BEOL features that will be considered in the study. It should be noted that although these equations require some corrections for advanced silicon technologies, they still provide a consistent theoretical basis for predicting first-order behavior. According to these equations, the characteristic impedance, Z_c , of the transmission lines in our case study can be expressed as [28],

$$Z_c = \frac{\eta_0}{\sqrt{\epsilon_{eff}}} \left[\frac{w_{eq}}{h} + 1.393 + 0.667 \ln \left(\frac{w_{eq}}{h} + 1.444 \right) \right], \quad (4)$$

where η_0 is the impedance of free space, ϵ_{eff} is the effective dielectric constant, h is the dielectric thickness and w_{eq} is the equivalent width of the line taking into account the effect of the line thickness and it is given by [27],

$$w_{eq} = w + \frac{t}{\pi h} \left[1 + \ln \left(\frac{2h}{t} \right) \right], \quad (5)$$

where w and t are the width and thickness of the line, respectively. Additionally, the losses in the transmission line can be approximated by [30],

$$\alpha_c = \frac{\sqrt{\pi f \mu_0 / \sigma}}{Z_c w} \quad (6)$$

$$\alpha_d = \frac{\pi \epsilon_r (\epsilon_{eff} - 1) \tan \delta}{\lambda \epsilon_{eff} (\epsilon_r - 1)} \quad (7)$$

where α_c represents the conduction losses and α_d represents the dielectric losses expressed in Neper per meter. Parameter μ_0 is the permeability of free space, σ is the conductivity of the metal line, f is the operation frequency, ϵ_r is the permittivity of free space and $\tan \delta$ is the loss tangent [30].

Equations (4)-(7) show that microstrip line performances are highly dependent on the width, thickness and conductivity of the metal line, the dielectric thickness and the dielectric constant, as schematically represented in Fig. 4. According to the information provided by the PDK, the dielectric constants and metal widths are parameters with a very small process variation that do not change noticeably the performance of the passive structure. Hence, they are excluded from the analysis. Similarly, the most relevant multi-parameter contribution to process variation appears to be the combination of the dielectric thickness, h , and the thickness of the line, t , since they appear as a ratio in (5).

Consequently, our methodology begins by computing the ΔP metrics for one-dimensional variations of the selected BEOL features and the set of target specifications. For that we have built seven corner models of the microstrip lines using the Momentum electromagnetic simulator. The PA under test was simulated using these corner models to infer the ΔP metrics associated to the BEOL features. The results are listed in Table II. This table shows the sets of identified BEOL features that are relevant for the prediction of each PA specification, ranked by relevance, together with the obtained ΔP values. In this analysis we have considered ΔP values below 0.05 as second-order effects that can be neglected with respect to the dominant variation contributions. According to the obtained results, the variations of the dielectric thickness, metal 8 thickness and metal 8 conductivity have a significant impact on the S-parameters and the PAE of the PA and a moderate impact on the linearity and saturation power. Other BEOL features show no significant contributions to these specifications. Concerning the current consumption, no significant impact is observed for any of the BEOL features. It is interesting to notice that there was no need of computing bi-variate $\Delta P(h, t)$ values, since both parameters were already identified as relevant parameters based on one-dimensional variations.

Again, given the topological simplicity of the DUT, it is possible to interpret the results from an electrical point of view. Indeed, the selected BEOL features have a direct impact on load adaptation and electrical losses in the DUT, which could have been anticipated by an expert mm-wave designer.

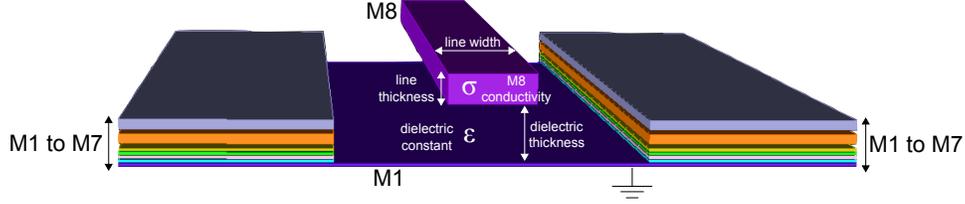


Fig. 4. Full-custom microstrip line and relevant BEOL features.

TABLE II
IDENTIFIED RELEVANT BEOL FEATURES FOR THE PREDICTION OF THE PA SPECIFICATIONS

Specification	Identified BEOL features ($\Delta P(F)$)
Gain (S_{21})	dielectric thickness (1.09), metal 8 thickness (0.25), metal 8 conductivity (0.25)
S_{11}	dielectric thickness (3.25), metal 8 conductivity (1.25), metal 8 thickness (1.02)
S_{22}	dielectric thickness (5.29), metal 8 thickness (1.29), metal 8 conductivity (0.36)
Power Added Efficiency, PAE	dielectric thickness (2.62), metal 8 thickness (0.79), metal 8 conductivity (0.54)
DC current, I_{DC}	–
Input referred 1 dB Compression point, ICP_{1dB}	dielectric thickness (0.54), metal 8 conductivity (0.33)
Output referred 1 dB Compression point, $OCPI_{1dB}$	dielectric thickness (0.54), metal 8 thickness (0.24)
Saturation output power, P_{sat}	dielectric thickness (0.81), metal 8 thickness (0.27)

However, in this case they were obtained from the proposed sensitivity metric.

C. Step 2: Design of non-intrusive process variation sensors

As a result of the previous step, we have identified two subsets of parameters related to process variations of standard and full-custom components, respectively, that are deemed relevant for explaining the degradation of the DUT performance. The following step in our methodology consists in designing a set of non-intrusive process monitors that generate simple signatures that are strongly correlated to the identified parameters.

The design of the non-intrusive process monitors and their associated signatures is guided by the physical meaning of the identified parameters. Thus, following the previous root-cause analysis, we have developed a set of 5 non-intrusive sensors and 7 signatures that are strongly correlated to the complete set of identified parameters and hence can be used for predicting the gain of the PA under test using a machine learning algorithm. It is important to notice that, eventually, signatures may be correlated to several process variation parameters, which may reduce the number of necessary signatures. Table III lists the set of designed non-intrusive process monitors and the associated signatures generated from each monitor.

As a sanity check, an additional step is performed to verify, at simulation level, that the proposed signatures measured from the designed process monitors are actually correlated to the identified set of relevant process parameters. Thus, for process monitors composed of standard components (i.e., process monitors labelled “MOM capacitor”, “Junction capacitance sensor” and “NMOS transistor” in Table III) we run a process Monte Carlo simulation for each monitor circuit and extract the generated signatures and the set of MC parameters for each sample. Then, we employ Algorithm 1 to verify

which MC parameters are relevant to explain the observed variations of the signatures. For process monitors composed of passive components (i.e., process monitors labelled “Thin microstrip line” and “Wide microstrip line” in Table III), both the analytical equations (4)-(7) and the sensitivity analysis based on corner analysis that was performed in the previous section validate that the proposed signatures should be well correlated to the intended BEOL physical parameters. As a result of this sanity check, the most relevant MC and BEOL parameters for explaining the variation of the signatures are listed in the column “Process parameters covered” in Table III.

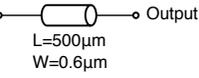
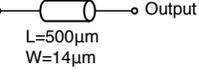
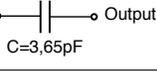
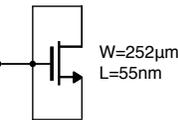
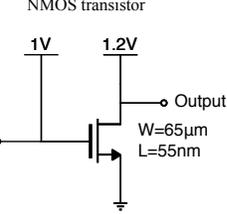
It is important to remark that the proposed signatures are a set of DC or low frequency measurements (compared to the operation frequency of the PA under test), which may enable the test of mm-wave circuits without the need of expensive mm-wave test equipment.

IV. RESULTS

In order to verify the feasibility and performance of the developed non-intrusive indirect test program, a proof-of-concept prototype containing the designed PA and the set of developed non-intrusive process monitors have been integrated in the selected 55 nm CMOS technology. The goal of our validation will be to show the equivalence between the direct measurement of the PA specifications using mm-wave equipment, and the proposed indirect measurement based on predicting the PA specifications from the set of developed signatures using a machine learning model.

Figure 5 shows a microphotograph of the fabricated prototype, including the PA under test, the non-intrusive process monitors and a set of de-embedding structures. The PA under test is labelled as PA, a corresponds to the thin transmission line, b to the wide transmission line, c to the MOM capacitor, d to the NMOS junction capacitance sensors and e to the NMOS

TABLE III
DEVELOPED NON-INTRUSIVE SENSORS AND ASSOCIATED SIGNATURES FOR PREDICTING THE PA UNDER TEST PERFORMANCE

Process variation sensor schematic	Signature description	Process parameters covered
<p>Thin microstrip line</p> 	<ul style="list-style-type: none"> • S_1: Resistance 	<ul style="list-style-type: none"> • Metal 8 thickness, Metal 8 conductivity
<p>Wide microstrip line</p> 	<ul style="list-style-type: none"> • S_2: Phase of S_{21} @ 1 GHz 	<ul style="list-style-type: none"> • Dielectric thickness, Metal 8 thickness, Metal 8 conductivity
<p>MOM Capacitor</p> 	<ul style="list-style-type: none"> • S_3: Real part of Y_{11} @ 1 GHz • S_4: Imag part of Y_{11} @ 1 GHz 	<ul style="list-style-type: none"> • $capa_1, capa_4, capa_2, capa_5, capa_3$ • $capa_2, capa_4, capa_5$
<p>Junction capacitance sensor</p> 	<ul style="list-style-type: none"> • S_5: Imag part of Y_{11} @ 1 GHz 	<ul style="list-style-type: none"> • $MOS_1, MOS_2, poly_3, MOS_8, MOS_6, MOS_7, MOS_5$
<p>NMOS transistor</p> 	<ul style="list-style-type: none"> • S_6: Gate resistance • S_7: Bias current 	<ul style="list-style-type: none"> • $poly_1, poly_2, poly_3, poly_4, MOS_7$ • $poly_3, MOS_8, MOS_5, MOS_4, MOS_7, MOS_3$

transistor. Structure e_2 is another test circuit not related to this study. Devices T, R, L and S are de-embedding structures, thru, reflect (open), line and short respectively. They were used to de-embed the sensors access for verification and design debugging and they are not actually needed for this study.

Although it may seem that the area overhead of the proposed test structures makes this approach unfeasible, it is convenient to remark that the developed prototype has been conceived as a proof-of-concept case study and as such, dedicated pads for probe test have been added to each non-intrusive sensor. In an actual system-level implementation, the non-intrusive sensors will be placed in the unused space within a transceiver and the access pads for the on-chip test structures can be multiplexed to save area. Indeed, the active area of the sensors (highlighted in blue in Fig. 5) represents only 0.0185 mm^2 , dominated mainly by the wide transmission line process monitor structure, while the PA under test occupies an area of 0.1430 mm^2 excluding pads. It is important to remark, however, that the access pads for the on-chip test structures should not be multiplexed with the DUT functional pads. Otherwise the technique would become intrusive and it might degrade the performance of the DUT. Thus, the area of the test access pads, even if they are multiplexed and shared for the different process monitors, should be computed as area overhead.

In total, we received 21 fabricated samples of the prototype integrated circuit that were characterized in the laboratory. Concerning our test setup, the PA specification measure-

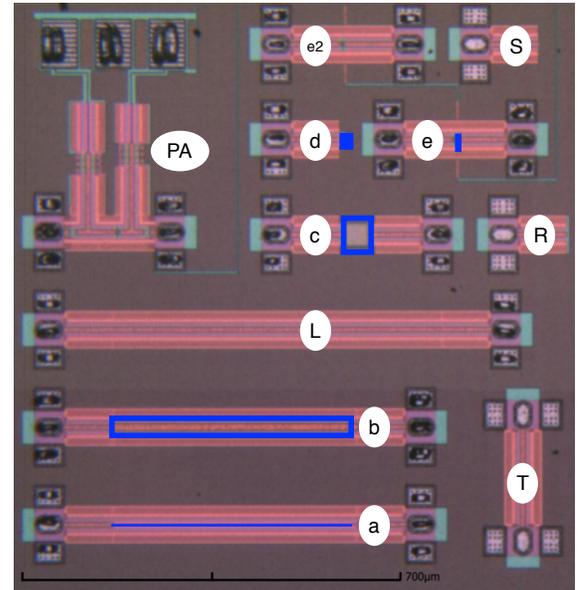


Fig. 5. Microphotograph of the PA under test with the proposed non-intrusive process monitors and de-embedding structures.

ments were performed using an Anritsu ME7838D4 Vector Network Analyzer (VNA), a Cascade S300 semi-automatic probe station and $50 \mu\text{m}$ GSG 145 GHz Infinity Probes from Cascade. Calibration was performed using the LRRM method on a Cascade impedance standard substrate P/N 138-356. DC

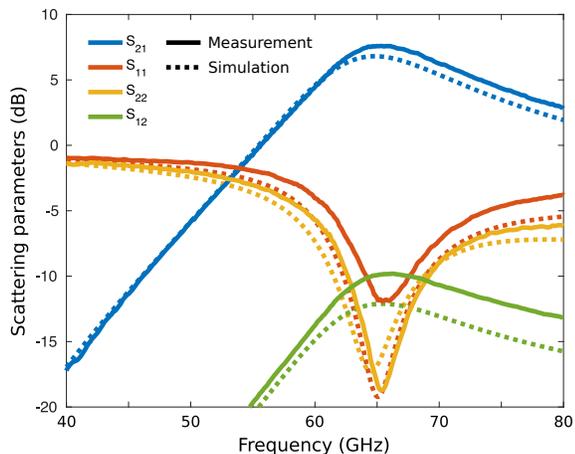


Fig. 6. Measured and simulated scattering parameters of the fabricated PA.

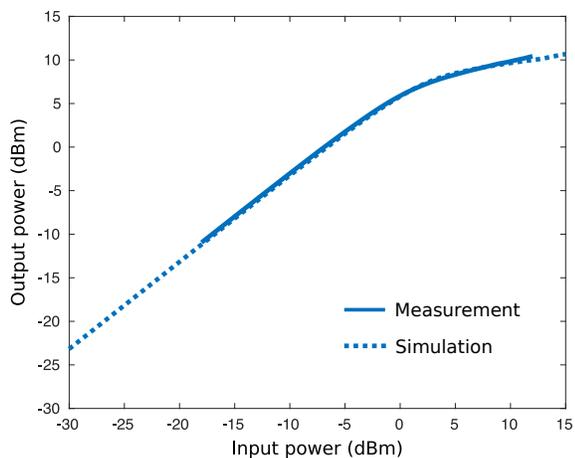


Fig. 7. Measured and simulated power characteristics of the fabricated PA.

supply was provided by a Keysight B2902A unit using $100\ \mu\text{m}$ SGS multi-contact Wedge Picoprobes from GGB. For large signal measurements, a 55–65 GHz PA (SP6010-30-20W from Space Labs) was used to drive the input of the PA under test. Power calibration was performed using Agilent V8486A power sensor, connected to a Hewlett-Packard 437B power-meter.

In order to show the performance of the fabricated PA, Fig. 6 and 7 show the measured S-parameters and the input-output power characteristic, respectively, for one of the fabricated PA samples. Solid lines correspond to the obtained measurements in the laboratory, while dotted lines represent post-layout simulations. As it can be observed, there is a good agreement between the obtained measurements and the expected simulation results. These characterization measurements were repeated for the 21 fabricated samples. The obtained minimum and maximum values at 65 GHz, together with the standard variation for each measured performance are listed in Table IV.

The signatures associated to each non-intrusive process monitor were extracted using $50\ \mu\text{m}$ GSG 145 GHz Infinity Probes from Cascade on the same VNA and probe station for AC signatures. For DC signatures, the operating point of the

monitor circuits was provided through the VNA bias tee.

For the thin microstrip line sensor, resistance (S_1) was calculated using Ohm's law with a 1 mV voltage difference across the line. Small signal measurements were performed at 1 GHz on the wide microstrip line, the MOS junction capacitor and the MOM capacitor (S_2 , S_3 , S_4 and S_5). It should be noted that the measurement of S_3 shows a very poor repeatability due to a high dependency on the probe placement in our test setup. Due to this experimental limitation we will not use signature S_3 in the proposed indirect test. Fortunately, most of the information present in S_3 is redundant with the information in S_4 , which should mitigate, to some extent, the effect of removing this signature.

Gate resistance process variations (signature S_6 in Table III) were inferred from small signal measurements using the following expression [31],

$$S_6 = \frac{\text{Real}(Y_{11})}{\text{Imag}(Y_{11})^2}. \quad (8)$$

where admittance parameter Y_{11} refers to the input node of the NMOS transistor process monitor in Table III.

The goal of the proposed indirect test is to infer the PA specifications from the extracted signatures. As it was presented in section II-A, this requires training a regression function f that maps the signatures to the target specifications of the PA under test as described in equation (1). In this case study we use a machine learning regression model, namely a perceptron Neural Network implemented in Matlab, for building the regression function f . In order to validate this indirect test strategy, we present two sets of experiments using the available data obtained from the fabricated samples. Thus, our first set of experiments is aimed at evaluating the performance (that is, the accuracy) of the proposed indirect test, while the second set of experiments shows the feasibility of the approach in a practical application scenario.

A. Evaluation of the indirect test performance

In general, the performance of a machine learning regression is measured by evaluating its prediction ability on independent test data, and it is typically expressed as the RMS error of the predicted values with respect to the actual ones. If we are in a data-rich situation, the best approach is to randomly split the data into two sets: a training set and a test set. The training set is used to fit the regression model, and then the independent test set is used for evaluating the RMS error of the predictions.

In the production line, the training of the regression model would be performed during the pre-production phase of the DUT on a data sample containing a few hundred (or thousand) devices. In our case study we do not have access to such fabrication volume. Special techniques have to be used for providing a realistic estimation of the model performance. The simplest and most widely used method for estimating the prediction error is the so-called K -fold cross-validation [32]. K -fold cross-validation uses a part of the available data to fit the model and a different part to test it. The data is split into K roughly equal-sized parts. The k -th part is set apart and the model is trained with the remaining $K - 1$

parts of the data. Then, the prediction error of the model is computed for the predictions of the k -th part of the data. The process is iterated for $k = 1, 2, \dots, K$ and the prediction error is estimated by combining the K partial estimations. When K is equal to the number of available data samples, the technique is known as leave-one-out cross-validation and it can be proved that the resulting error estimation is a good metric of the model performance that approximates the true prediction error (i.e., the expected prediction error that could be achieved in a data-rich scenario). The interested reader is referred to [32] for a detailed mathematical analysis of the cross-validation technique.

In order to provide a reliable estimation of the proposed indirect test performance, we have trained the perceptron Neural Network regression models using the leave-one-out cross-validation technique as described in [32] using our 21 fabricated samples. The procedure is fully detailed in Algorithm 2. The obtained estimations of the RMS prediction error for all the considered DUT performances are listed in Table IV. It can be seen that the obtained prediction errors are very contained. To provide further insight into these results, Table IV shows a direct comparison between the standard deviation (σ) in the functional measurement of all the considered specifications of the PA under test, and the RMS prediction error obtained in the prediction of each specification from the proposed set of low-cost signatures. In this line, we defined a Figure of Merit (FoM) as the ratio between the standard deviation of the functional measurement and the RMS prediction error, for each specification. Thus, a FoM larger than one indicates that the regression model predicts the specification with a better accuracy than the standard deviation of the specification in the considered set of devices. As it can be observed, the RMS prediction error is significantly smaller than the specification standard deviation for all the considered specifications which leads to high values of FoM. This is a strong indication of the accuracy of the proposed indirect test, even more noteworthy if we consider the very limited number of samples at our disposal for this case study.

B. Practical application example

In order to show the feasibility of the proposed indirect test for the prediction of the PA specifications, we present a practical direct application example. For this application example, we have split the data into a random partition. Thus, 16 randomly selected samples out of the 21 fabricated samples have been selected to train a perceptron Neural Network for the prediction of the PA specifications from the set of proposed low-cost indirect signatures. The resulting regression models are then verified in the remaining 5 samples, that are kept apart from the training and used as an independent test set.

Fig. 8 shows scatterplots of the obtained results for each of the considered specifications of the PA under test. The vertical axis represents the prediction of the PA under test specifications obtained from the proposed set of low-cost signatures. The horizontal axis represents the actual specification of the PA under test, obtained by standard mm-wave measurements. The dashed red line represents the perfect 1:1

Algorithm 2

- Leave-one-out cross-validation for training and verification of machine learning models with limited data sets
- 1: Measure the set of signatures from the m process monitors for each of the n fabricated samples. Build signature matrix $\mathbf{S} = \{S_{ij}\}$ for $i = 1, \dots, n$ and $j = 1, \dots, m$
 - 2: Measure the set of p target performances for each of the n fabricated samples. Build performance matrix $\mathbf{P} = \{P_{ik}\}$ for $i = 1, \dots, n$ and $k = 1, \dots, p$
 - 3: **for** $t=1$ **to** n **do**
 - 4: Define training sets excluding device t : $\mathbf{S}^* = \mathbf{S} \setminus \{S_{tj}\} \forall j$ and $\mathbf{P}^* = \mathbf{P} \setminus \{P_{tk}\} \forall k$ (i.e., excluding row t from matrices \mathbf{S} and \mathbf{P})
 - 5: Define device t as verification set: $\{\{S_{tj}\}, \{P_{tk}\}\} \forall j, k$
 - 6: Build regression model f using \mathbf{S}^* and \mathbf{P}^*
 - 7: Validate the regression for left-out device t :
 - 8: Compute predicted performances from measured signatures: $\{P_{t1}^{\text{predicted}}, P_{t2}^{\text{predicted}}, \dots, P_{tp}^{\text{predicted}}\} = f(S_{t1}, S_{t2}, \dots, S_{tm})$
 - 9: Compute prediction error for each performance: $\epsilon_{tk} = P_{tk} - P_{tk}^{\text{predicted}}$ for $k = 1, \dots, p$
 - 10: **end for**
 - 11: **return** Estimate the quality of the regression as the root-mean-square prediction error: $\epsilon_{RMS,k} = \sqrt{\sum_t \epsilon_{tk}^2 / n}$ for the $k = 1, \dots, p$ performances.
-

regression line for visual reference. Hollow circle markers are used for samples in the training set, while full diamond markers are used for samples in the independent test set. As it can be seen, even with our limited number of training devices, we observe a significant correlation between the predictions and the actual specifications for all the considered PA performances. To provide further insight into the quality of the overall regression, Fig. 8 includes the RMS prediction error, ϵ_{RMS} , computed for the samples in the independent test set for each considered specification. The obtained RMS prediction error values show a very good accuracy for the prediction of all the PA specifications. In fact, for most performances, the obtained RMS prediction error is not degraded with respect to the prediction error estimations in Table IV obtained using the leave-one-out cross-validation technique. This is again an indication of the strong correlation between the proposed low-frequency signatures and the DUT high-frequency performances.

V. CONCLUSIONS

We have presented a systematic methodology for designing non-intrusive indirect test strategies for mm-wave circuits based on on-chip process monitors. The proposed methodology targets the test of mm-wave integrated circuits containing both standard devices modeled in the PDK of the technology and full-custom passive components built in the BEOL of the technology. For a given DUT, the proposed test generation strategy is based on analyzing the root-causes of parametric performance degradation. This analysis guides the design of a set of non-intrusive process monitors that yield low cost signatures sensitive to the identified degradation root-causes.

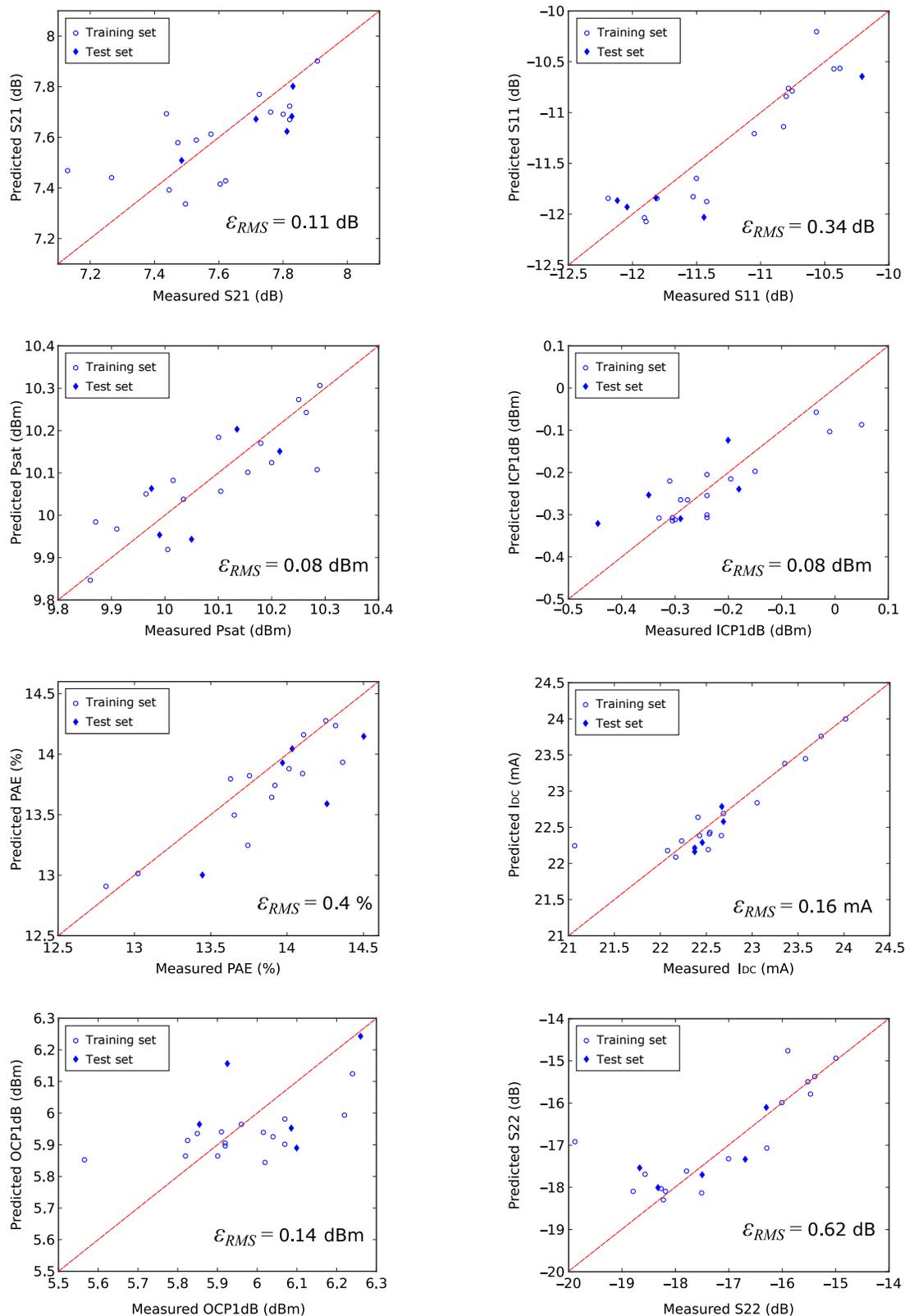


Fig. 8. Prediction of PA specifications from the set of low-cost signatures versus standard mm-wave functional measurements. Data randomly split into 16 samples for the training set and 5 samples for the test set. The RMS prediction error evaluated in the test set has been included for each specification.

TABLE IV
MEASURED PERFORMANCES OF THE PA AND PREDICTION RESULTS

PA performance	Unit	Functional measurement			RMS prediction error	FoM
		Minimum	Maximum	Std. dev. σ		
DC current, I_{DC}	mA	21.1	24.0	0.64	0.15	2.13
Gain, S_{21}	dB	7.13	7.91	0.21	0.11	1.91
S_{11}	dB	-12.4	-10.2	0.67	0.21	3.19
S_{22}	dB	-19.9	-15.0	1.38	0.47	2.94
Saturation output power, P_{sat}	dBm	9.86	10.29	0.14	0.07	2.00
Input referred 1 dB Compression point, ICP_{1dB}	dBm	-0.45	0.05	0.12	0.07	1.71
Output referred 1 dB Compression point, OCP_{1dB}	dBm	5.57	6.26	0.16	0.08	2.00
Maximum Power Added Efficiency, PAE_{max}	%	12.82	14.50	0.44	0.30	1.33

The generated indirect test is completed with a machine learning model that allows inferring the DUT specifications from the set of low-cost signatures.

The feasibility of the proposed technique has been experimentally validated with a proof-of-concept case study consisting on a 65 GHz PA fabricated in STMicroelectronics 55 nm CMOS technology. A set of non-intrusive process monitors has been designed according to the proposed methodology and integrated together with the PA under test. Experimental measurements on a set of 21 fabricated PAs show a very good agreement between the direct functional measurement of the PA specifications using dedicated mm-wave test equipment and the proposed indirect test based on low-cost low-frequency non-intrusive signatures. The remarkably good results that have been obtained from such a limited number of fabricated devices are a promising indicator of the feasibility of the proposed technique and may attract the attention of the industry for further validation in a high-volume production scenario.

Future work in this research includes the validation of the proposed test technique in case studies that are very different in nature, complexity and scale, such as mm-wave VCOs, distributed amplifiers, and complete transceiver front-ends. In this line the proposed technique can be hierarchically applied in complex systems in order to identify the main variation root causes for each of the building blocks in the system, and then it can be combined with a system-level search to determine how building block variations affect system-level performances.

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REFERENCES

- [1] R. L. Schmid, P. Song, C. T. Coen, A. . Ulusoy, and J. D. Cressler, "A W-band integrated silicon-germanium loop-back and front-end transmit-receive switch for built-in-self-test," in *2015 IEEE MTT-S International Microwave Symposium*, May 2015, pp. 1–4.
- [2] S. Zeinolabedinzadeh, A. C. Ulusoy, R. L. Schmid, F. Inanlou, I. Song, T. Chi, J. S. Park, H. Wang, and J. D. Cressler, "A W-Band SiGe Transceiver with Built-in Self-Test," in *2019 IEEE 19th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan 2019, pp. 1–4.
- [3] I. Nasr, J. Nehring, K. Aufinger, G. Fischer, R. Weigel, and D. Kissinger, "Single- and dual-port 50-100-ghz integrated vector network analyzers with on-chip dielectric sensors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 9, pp. 2168–2179, 2014.
- [4] S. Y. Kim, O. Inac, C. Kim, D. Shin, and G. M. Rebeiz, "A 76–84-GHz 16-Element Phased-Array Receiver With a Chip-Level Built-In Self-Test System," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 3083–3098, Aug 2013.
- [5] O. Inac, F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90–100-GHz Phased-Array Transmit/Receive Silicon RFIC Module With Built-In Self-Test," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 10, pp. 3774–3782, Oct 2013.
- [6] S. M. Bowers, K. Sengupta, K. Dasgupta, B. D. Parker, and A. Hajimiri, "Integrated self-healing for mm-wave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1301–1315, 2013.
- [7] N. Barabino and F. Silveira, "Digitally Assisted CMOS RF Detectors With Self-Calibration for Variability Compensation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 5, pp. 1676–1682, May 2015.
- [8] A. Tang, F. Hsiao, D. Murphy, I. Ku, J. Liu, S. D'Souza, N. Wang, H. Wu, Y. Wang, M. Tang, G. Virbila, M. Pham, D. Yang, Q. J. Gu, Y. Wu, Y. Kuan, C. Chien, and M. F. Chang, "A low-overhead self-healing embedded system for ensuring high yield and long-term sustainability of 60ghz 4gb/s radio-on-a-chip," in *2012 IEEE International Solid-State Circuits Conference*, 2012, pp. 316–318.
- [9] R. Voorakaranam, S. S. Akbay, S. Bhattacharya, S. Cherubal, and A. Chatterjee, "Signature testing of analog and rf circuits: Algorithms and methodology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1018–1031, May 2007.
- [10] V. Natarajan, H. W. Choi, A. Banerjee, S. Sen, A. Chatterjee, G. Srinivasan, F. Taenzler, and S. Bhattacharya, "Low cost evm testing of wireless rf soc front-ends using multitone," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 7, pp. 1088–1101, July 2012.
- [11] N. Kupp, H. Huang, Y. Makris, and P. Drineas, "Improving analog and rf device yield through performance calibration," *IEEE Design Test of Computers*, vol. 28, no. 3, pp. 64–75, May 2011.
- [12] M. J. Barragan, R. Fiorelli, G. Leger, A. Rueda, and J. L. Huertas, "Alternate Test of LNAs Through Ensemble Learning of On-Chip Digital Envelope Signatures," *J. of Electronic Testing*, vol. 27, no. 3, pp. 277–288, Jan. 2011.
- [13] A. Zjajo, M. J. Barragan, and J. P. de Gyvez, "BIST Method for Die-Level Process Parameter Variation Monitoring in Analog/Mixed-Signal Integrated Circuits," in *2007 Design, Automation & Test in Europe Conference & Exhibition*, 2007, pp. 1–6.
- [14] L. Abdallah, H. G. Stratigopoulos, S. Mir, and C. Kelma, "Experiences with non-intrusive sensors for RF built-in test," in *2012 IEEE International Test Conference*, 2012, pp. 1–8.
- [15] M. Andraud, H. Stratigopoulos, and E. Simeu, "One-shot non-intrusive calibration against process variations for analog/rf circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 2022–2035, Nov 2016.
- [16] T. Mahzabeen, R. M. Henderson, and B. Banerjee, "Built-in self-test (bist) algorithm to mitigate process variation in millimeter wave circuits," in *WAMICON 2014*, 2014, pp. 1–3.
- [17] A. Dimakos, H. Stratigopoulos, A. Siligaris, S. Mir, and E. De Foucauld, "Built-in test of millimeter-Wave circuits based on non-intrusive sensors," in *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, 2016, pp. 505–510.

- [18] F. Cilici, M. J. Barragan, S. Mir, E. Lauga-Larroze, and S. Bourdel, "Assisted test design for non-intrusive machine learning indirect test of millimeter-wave circuits," in *2018 IEEE 23rd European Test Symposium (ETS)*, May - June 2018, pp. 1–6.
- [19] L. Abdallah, H. Stratigopoulos, S. Mir, and J. Altet, "Defect-oriented non-intrusive RF test using on-chip temperature sensors," in *IEEE 31st VLSI Test Symposium (VTS)*, April 2013, pp. 1–6.
- [20] A. Coyette, B. Esen, R. Vanhooren, W. Dobbelaere, and G. Gielen, "Automated testing of mixed-signal integrated circuits by topology modification," in *2015 IEEE 33rd VLSI Test Symposium (VTS)*, April 2015, pp. 1–6.
- [21] I. Guyon and A. Elisseeff, "An introduction to variable and feature selection," *Journal of Machine Learning Research*, vol. 3, Mar. 2003.
- [22] G. Leger and M. J. Barragan, "Brownian distance correlation-directed search: A fast feature selection technique for alternate test," *Integration, the VLSI Journal*, vol. 55, pp. 401–414, Sep. 2016.
- [23] G. J. Székely and M. L. Rizzo, "Brownian distance covariance," *The Annals of Applied Statistics*, vol. 3, no. 4, pp. 1236–1265, 2009.
- [24] A. Scuderi, T. Biondi, E. Ragonese, and G. Palmisano, "A lumped scalable model for silicon integrated spiral inductors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 6, pp. 1203–1209, 2004.
- [25] A. Bautista, A. Franc, and P. Ferrari, "Accurate parametric electrical model for slow-wave cpw and application to circuits design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 12, pp. 4225–4235, 2015.
- [26] J. P. Mondal, "An experimental verification of a simple distributed model of mim capacitors for mmic applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 35, no. 4, pp. 403–408, 1987.
- [27] M. V. Schneider, "Dielectric loss in integrated microwave circuits," *The Bell System Technical Journal*, vol. 48, no. 7, pp. 2325–2332, 1969.
- [28] E. O. Hammerstad, "Equations for microstrip circuit design," in *1975 5th European Microwave Conference*, September 1975, pp. 268–272.
- [29] R. Igreja and C. J. Dias, "Analytical evaluation of the interdigital electrodes capacitance for a multi-layered structure," *Sensors and Actuators A: Physical*, vol. 112, no. 2, pp. 291–301, 2004. [Online]. Available: <http://www.sciencedirect.com/science/article/pii/S0924424704000779>
- [30] D. M. Pozar, *Microwave Engineering, 4th Edition*. Wiley, November 2011.
- [31] C.ENZ, "An mos transistor model for rf ic design valid in all regions of operation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 342–359, 2002.
- [32] T. Hastie, R. Tibshirani, and J. Friedman, *The Elements of Statistical Learning, Second Edition*, ser. Springer Series in Statistics. Springer, 2009.

APPENDIX A

BROWNIAN DISTANCE CORRELATION

The concept of distance correlation, \mathcal{R} , was introduced in [23] to test for correlation between a set of candidate features and a set of target performances. This work demonstrated that this independence test statistics is consistent against all types of dependence alternatives with finite second moments.

The distance correlation statistics is defined in [23] and reproduced here for completeness. For a random sample $(\mathbf{X}, \mathbf{Y}) = \{(X_k, Y_k) : k = 1, \dots, n\}$ of n independent random vectors (X, Y) from the joint distribution of random vectors X in \mathbb{R}^p and Y in \mathbb{R}^q , let us compute the Euclidian distance matrices $(a_{kl}) = (|X_k - X_l|_p)$ and $(b_{kl}) = (|Y_k - Y_l|_q)$. We define

$$A_{kl} = a_{kl} - \bar{a}_{k.} - \bar{a}_{.l} + \bar{a}_{..} \quad k, l = 1, \dots, n \quad (9)$$

where

$$\bar{a}_{k.} = \frac{1}{n} \sum_{l=1}^n a_{kl}, \quad \bar{a}_{.l} = \frac{1}{n} \sum_{k=1}^n a_{kl}, \quad \bar{a}_{..} = \frac{1}{n^2} \sum_{k,l=1}^n a_{kl} \quad (10)$$

Similarly, we define $B_{kl} = b_{kl} - \bar{b}_{k.} - \bar{b}_{.l} + \bar{b}_{..}$ for $k, l = 1, \dots, n$. The sample distance covariance $\mathcal{V}_n(\mathbf{X}, \mathbf{Y})$ and sample distance correlation $\mathcal{R}_n(\mathbf{X}, \mathbf{Y})$ are then given by

$$\mathcal{V}_n^2(\mathbf{X}, \mathbf{Y}) = \frac{1}{n^2} \sum_{k,l=1}^n A_{kl} B_{kl} \quad (11)$$

and

$$\mathcal{R}_n^2(\mathbf{X}, \mathbf{Y}) = \begin{cases} \frac{\mathcal{V}_n^2(\mathbf{X}, \mathbf{Y})}{\sqrt{\mathcal{V}_n^2(\mathbf{X})\mathcal{V}_n^2(\mathbf{Y})}} & \mathcal{V}_n^2(\mathbf{X})\mathcal{V}_n^2(\mathbf{Y}) > 0; \\ 0 & \mathcal{V}_n^2(\mathbf{X})\mathcal{V}_n^2(\mathbf{Y}) = 0 \end{cases} \quad (12)$$

respectively, where the sample distance variance is given by

$$\mathcal{V}_n^2(\mathbf{X}) = \mathcal{V}_n^2(\mathbf{X}, \mathbf{X}) = \frac{1}{n^2} \sum_{k,l=1}^n A_{kl}^2 \quad (13)$$

Distance correlation $\mathcal{R}(X, Y)$ generalizes classical Pearson's correlation ρ in the way that it is defined for X and Y in arbitrary dimension, and $\mathcal{R}(X, Y) = 0$ characterizes independence of X and Y . In the bivariate normal case, \mathcal{R} is a deterministic function of ρ , and $\mathcal{R}(X, Y) \leq |\rho(X, Y)|$ with equality when $\rho = \pm 1$. The interested readers are referred to [23] for a detailed discussion of the Brownian distance correlation mathematical properties.



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