



HAL
open science

Characterization and electrical modeling of polycrystalline silicon vertical thin film transistors

P Zhang, Emmanuel Jacques, Régis Rogel, Laurent Pichon, Olivier Bonnaud

► **To cite this version:**

P Zhang, Emmanuel Jacques, Régis Rogel, Laurent Pichon, Olivier Bonnaud. Characterization and electrical modeling of polycrystalline silicon vertical thin film transistors. *Solid-State Electronics*, 2020, 171, pp.107798. 10.1016/j.sse.2020.107798 . hal-02891811

HAL Id: hal-02891811

<https://hal.science/hal-02891811>

Submitted on 9 Jul 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Characterization and electrical modeling of polycrystalline silicon vertical thin film transistors

Peng Zhang^{1,a)}, Emmanuel Jacques², Regis Rogel², Laurent Pichon²,
Olivier Bonnaud²

AFFILIATIONS

¹College of Electronic and Optical Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210023, People's Republic of China

²Département Microélectronique et Microcapteurs, IETR, UMR CNRS 6164, Université de Rennes 1, 35042 Rennes Cedex, France

Corresponding authors: zp@njupt.edu.cn

Abstract

Thin film transistors (TFTs) with lateral channels are limited in current density due to the design rule. For many applications with improved integration, the introduction of vertical channels reduces channel lengths while increasing current density per unit surface area. In previous works, vertical TFTs have been designed and manufactured using low-temperature polycrystalline silicon technology ($T \leq 600^\circ\text{C}$), with a solid

phase crystallization (SPC) based process. In this case, the introduction of an insulating layer between source and drain films has resulted in a significant improvement in the electrical characteristics, mainly in the On/Off state current ($I_{\text{on}}/I_{\text{off}}$) ratio. However, the active layer is deposited on the sidewalls obtained by plasma etching, and the etching process results in morphological defects on the sidewalls that adversely affect the electrical characteristics. The purpose of this paper is to understand the origin and effects of these defects using different models. Thus, the transfer characteristics are analyzed in detail, with Suzuki method to calculate the density of states, while subthreshold slope method and Grünwald method are adopted to verify the Suzuki method for the deep and shallow trap densities, respectively. These methods provide an approach for DOS calculation independent of temperature-related measurement.

Key words: vertical thin film transistors, low temperature polycrystalline silicon, density of states, conduction modeling

1. Introduction

Polycrystalline silicon thin-film transistors (TFTs) are generic components of large-surface electronics made on low-temperature substrates such as glass and, more recently, plastics, polymers and even paper. They have met the needs of various fields, for example, by being

used in radio frequency identification (RFID) tags [1], random access memories (RAM) [2], flat panel displays [3], and more particularly active matrix flat panel displays involving either liquid crystals (AMLCD [4]) or organic light emitting diodes (AMOLED [5]). For these applications, one of the objectives is to produce a high current density at the pixel level that can be obtained either by shortening the channel length of conventional TFTs with parallel conduction to the substrate surface, or by modifying the architecture with vertical conduction. Thus, vertical TFTs have been proposed, in which the source and drain are positioned on the top and at the bottom of the transistor, respectively, and the channel length is defined by the film thickness between the source and drain regions, regardless of the design rule [6]. As a result, the vertical TFT architecture can provide an ultra-short channel length, which theoretically allows a much higher current density. In our previous work, we designed and manufactured a vertical TFT by stacking three layers of *in situ* deposited polycrystalline silicon, as shown in figure 1(a), for which a high drain-source current for the on-state (I_{on}) of about 0.3 mA is obtained, but with a high off-current (I_{off}) measured at the minimum value (about 0.3 μ A), which provides an I_{on}/I_{off} ratio of about 1000. This relatively low ratio is due to the large overlapping area of the source and drain, which limits its potential applications [7]. In order to avoid this phenomenon, a second architecture was proposed with an insulating thin film between source and drain films

and with parallel channels deposited on the sidewalls (see figure 1(b)). The length of the channel remains the same but the conduction in the overlapping area of source and drain is considerably decreased. However, in this case there is a modification of the nature of the sidewalls underneath the channel due the stacking of source layer, undoped polysilicon layer, barrier layer, and drain layer. Because the etching rate is not the same for these materials, the interface between channel polycrystalline Si layer and the quasi-vertical sidewalls is not homogeneous with some roughness. The electrical behavior is thus different from the case of a lateral TFT.

Silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) insulators were adopted as the barrier layer between source and drain, and considering the high etching selectivity between barrier layer and the polycrystalline silicon layer, a thin $\text{SiO}_2/\text{Si}_3\text{N}_4$ layer is appropriate. On the other hand, in order to minimize the short channel effects, the channel length can be moderately increased with the presence of an undoped polycrystalline Si layer for which the thickness is well controlled. After optimization of the process, by involving SiO_2 , the barrier layer between source and drain incorporates a 100 nm SiO_2 layer with a 1 μm undoped polycrystalline Si (figure 1(c)). By involving Si_3N_4 , the barrier layer incorporates a 200 nm Si_3N_4 layer with a 1 μm undoped polycrystalline Si layer (figure 1(d)). It is noteworthy that a thicker Si_3N_4 insulating layer in comparison to SiO_2 guarantees the good insulating property of the Si_3N_4 layer deposited by low temperature

chemical vapor deposition (LPCVD) method, which does not greatly affect the electrical characteristics of the fabricated devices. Even though SiO_2 or Si_3N_4 layers films are very thin, the sidewalls still undergo high roughness and create high density of seed sites for polycrystalline silicon active layer deposition that adversely affects the electrical properties, mainly the transconductance, the on-state and off-state currents.

The fabrication process of the vertical TFT is listed as follows. After a basic RCA cleaning of the substrates, a thick SiO_2 buffer layer of 500 nm is deposited by atmospheric pressure chemical vapor deposition (APCVD) at 420°C . Then, different layers are deposited, in the sequence of a thick N-type *in situ* heavily-doped polycrystalline Si layer by LPCVD, a 100 nm SiO_2 layer by APCVD or a 200 nm Si_3N_4 layer by LPCVD, a 1 μm undoped polycrystalline Si layer, and finally another N-type *in situ* heavily-doped polycrystalline Si layer by LPCVD. Two reactive ion etching (RIE) steps are then carried out to define the multi-tooth configuration as well as form the sidewalls, and to discriminate the source and drain regions. Note that, the source and drain regions are discriminated by a partial etching until reaching the bottom N-type heavily-doped polycrystalline Si layer by the aid of a laser interferometer measurement. Afterwards, an undoped polycrystalline Si layer is deposited and patterned by the third RIE step, which forms a channel at each sidewall. Prior to the gate oxide layer deposition, an essential RCA cleaning is carried out to eliminate most of

the defects at the surface of the active layer. In sequence, a 70 nm gate oxide layer is deposited by APCVD and densified at 600°C for 12 hours to eliminate most defects in the gate oxide, and the gate oxide layer is patterned by the fourth mask to show contact holes for source and drain. Finally, a thick aluminum layer is deposited by thermal evaporation, patterned by a fifth mask and a wet etching process to define source, drain and gate electrodes. The electrical characterization is carried out by an Agilent B1500 semiconductor parameter analyzer in ambient air.

The fabricated device configuration is shown in figure 1(e), which demonstrates a typical four-tooth structure, and therefore eight channels are formed on the sidewalls. The typical measurement is based on drain-on-top configuration, while the source-on-top configuration shows nearly the same electrical characteristics, demonstrating the symmetry of the fabricated structure. Figure 1(c) and 1(d) show the sidewalls based on the 100 nm SiO₂ or 200 nm Si₃N₄ barrier layer, respectively. Due to the higher etching selectivity between SiO₂ and polycrystalline Si, higher roughness is obtained for the sidewall with SiO₂ barrier layer, in contrast, the lower etching selectivity between Si₃N₄ and polycrystalline Si enables a much flatter sidewall, even though there is a recess at the barrier layer for both cases. Predicted by the sidewall roughness, which can greatly affect the grain nucleation, the device with Si₃N₄ barrier enables better electrical characteristics. In the following, a simplified model is expected to explain

this behavior.

2. Results and Discussions

The transfer characteristics of the typical vertical TFTs are shown in figure 2(a) and 2(b), where different drain-source voltages are adopted corresponding to the linear regime. Note that, from output characteristics measurement, a kink region is also observed [8]. The kink effect is due to the short channel length. Indeed, the large electric field at the drain side accelerate the carriers in the channel that collide with the crystal lattice in the pinch-off region to generate extra electron-hole pairs. This adverse effect can be attenuated either by a lightly doped drain structure (LDD) or by an extension of the channel length. Derived from the transfer characteristic curves, the high on/off current ratio reaches about 10^5 for SiO_2 gate insulator, while for the Si_3N_4 barrier layer device, the current ratio is higher and reaches about 10^6 for lower drain-source voltages (10 mV and 100 mV). When increasing the drain-source voltages, the on-current increases proportionally, where the off-current increases superproportionally, which brings about a reduced current ratio. The deduced on/off current ratio $I_{\text{on}}/I_{\text{off}}$, transconductance g_m , threshold voltage V_{th} , subthreshold slope SS, and field effect mobility μ_{FE} , from each transfer curve are shown in table 1. The threshold voltage V_{th} , and the field effect mobility μ_{FE} are deduced from the transistor current formula in the linear

regime shown below:

$$I_{ds} = \frac{WC_i\mu_{FE}}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{1}{2} V_{ds}^2 \right] \quad (1)$$

Where W/L are the channel width/length ratio, C_i is the gate capacitance per unit area, V_{gs} and V_{ds} are the gate bias and the drain-source voltage, respectively. Note that, in the calculation, the channel length is defined as the total thickness of the barrier layer and the undoped polycrystalline Si layer, which is approximately $1.1 \mu\text{m}$ for the device with 100 nm SiO_2 layer, and approximately $1.2 \mu\text{m}$ for the device with $200 \text{ nm Si}_3\text{N}_4$ layer, and the roughness of the sidewall does not greatly affect the channel length. The transconductance g_m is calculated from the slope of the transfer characteristics in the linear coordinate, while the subthreshold slope SS is calculated from the reciprocal of the slope in the subthreshold region of the transfer characteristics in the semi-logarithm coordinate. Note that, due to the high stability of the polycrystalline Si active layer in ambient air and the high design rule precision in the fabrication process, the fabricated device is highly reproducible, which can be verified from the relationship between different devices with different channel width/length ratios [8]. Therefore, the electrical characteristics of the adopted devices are typical and representative.

Three main remarks can be made, (1) for the threshold voltage V_{th} , the devices with SiO_2 barrier layer and with Si_3N_4 barrier layer have approximately the same threshold voltage of approximately 4 V , with a

slightly higher value for the device with Si_3N_4 insulating layer that does not greatly affect the electrical characteristics; (2) with regard to the subthreshold slope SS, the device with SiO_2 barrier layer has a SS comparable to that of the device with Si_3N_4 barrier layer. For low drain-source voltages, the SS of the device with the SiO_2 barrier layer is greater than that of the device with the Si_3N_4 barrier layer, while for high drain source voltage, the SS of the device with SiO_2 barrier layer is smaller than that of the device with Si_3N_4 barrier layer; (3) the transconductance and the field effect mobility of the device with Si_3N_4 barrier layer are greater than that of the device with SiO_2 barrier layer.

The first point indicates similar defects or impurities density in the vertical devices, while the second point indicates similar deep trap densities in the two types of vertical TFTs. In contrast, the third point indicates a higher shallow trap density in TFT with SiO_2 barrier layer, in which carriers must fill the shallow traps, knowing that the remaining untrapped carriers contribute to field effect mobility.

It is also noteworthy that, for the short channel device, the access resistance contributes more to the total resistance, therefore the access resistance needs to be evaluated. Since transistors operate in the linear regime, the access resistance can be deduced from the relationship between R_{total} and $1/(V_{\text{gs}}-V_{\text{th}})$ as shown in Figure 2c. For the vertical TFT with Si_3N_4 barrier layer, the deduced access resistance is approximately 225 Ω , and

the intrinsic field effect mobility is approximately $15.5 \text{ cm}^2/\text{V}\cdot\text{s}$. For reference, the access resistance of a typical lateral TFT is in the order of $100 \text{ }\Omega$, and the field effect mobility reaches in the best case $100 \text{ cm}^2/\text{V}\cdot\text{s}$ [9]. Therefore, the access resistance is not important for the vertical TFT configuration, and comparatively, the lower mobility of vertical TFT is more likely to be due to the low-quality grain nucleation of the active layer on the rugged sidewall, which provides more grain boundaries. In order to further prove that the access resistance does not greatly influence the electrical parameters, such as the threshold voltage v_{th} , a second-derivative method is proposed to extract the threshold voltage v_{th} [10], supposing the ideal condition that the subthreshold current is zero and the drain current increases linearly with the gate bias when it is above the threshold voltage, therefore, a critical transition of the second-derivative curve for the drain current takes place at the threshold voltage. In practice, the critical transition shows as a peak with broadened spreading, with the peak value position corresponding to the threshold voltage v_{th} . Figure 2 (d) and 2 (e) shows the second-derivative curve for the vertical TFTs with SiO_2 and Si_3N_4 barrier layer, respectively, for both types of vertical TFTs, they show the same threshold voltage v_{th} of approximately 4.4 V for a drain-source voltage of 0.1 V , which is consistent with the calculation from the conventional extrapolating method shown above, indicating the independence of the electrical characteristics on the access resistance for

both types of vertical TFTs.

The bandgap density of states (DOS) was studied by the simple Suzuki method [11], for which the transfer characteristics of the typical vertical TFTs are studied and analyzed. From Poisson equation, the potential bending of the surface space charge layer $u(x)$ is defined by:

$$\frac{d^2u(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_a} \quad (2)$$

Where ϵ_a is the dielectric constant of the polycrystalline Si, $\rho(x)$ is the local space charge density at x due to the local Fermi-level shift of $eu(x)$. The local space charge density is related to the gap state density distribution $N(E)$ by:

$$\rho(x) = (-e) \int_{E_F - eu(x)}^{E_F} N(E) dE \quad (3)$$

where E_F is the equilibrium Fermi-level, $eu(x)$ is the band bending, and e is the elementary charge.

The surface potential bending u_a dependence with the gate voltage V_{GS} can be deduced from sheet conductance modulation δG [10]:

$$\delta u_a = \frac{\delta G}{G_0} \cdot \frac{\epsilon_i}{\epsilon_a} \cdot \frac{d_a}{d_i} (V_{GS} - u_{bi} - u_a) / [\exp(eu_a / kT) - 1] \quad (4)$$

where G_0 corresponds to the conductance at the flat-band condition, d_a is the channel thickness of polycrystalline Si (which is set to be 10 nm [12]), ϵ_i and ϵ_a are the relative permittivity of gate dielectric and the active layer of polycrystalline Si respectively, d_a and d_i are the thickness of channel and the gate dielectric layer respectively, and u_{bi} is approximately the flat-band

voltage. By iterative calculation, the relationship between u_a and V_G can be obtained.

Using this method, the bandgap DOS is calculated from the transfer characteristics shown in Figure 3(a), which have been plotted for both types of vertical transistors and for a lateral transistor as reference. Note that, in order to show the similar drain-source electric field, a lower drain-source voltage of 0.1 V is adopted for the vertical short-channel TFTs ($L \approx 1 \mu\text{m}$), and a larger drain-source voltage of 1 V is adopted for the lateral TFT ($L = 20 \mu\text{m}$). For the lateral TFT, as shown in table 1, the subthreshold slope SS is approximately 0.87 V/dec, the threshold voltage V_{th} is approximately 3.7 V, the field effect mobility is approximately $81.1 \text{ cm}^2/\text{V}\cdot\text{s}$, and the smaller I_{off} in the order of 10 pA is assumed to be due to the high-quality polycrystalline Si, especially in the increase of the average grain size and decrease of the intragrain defect density [13]. The calculated DOS for the vertical TFTs and the lateral TFT are plotted in figure 3(b). From the DOS curves, four main comments can be made, (1) the larger $E_F - E$ shows higher DOS, which means the shallow trap density of states is higher than the deep trap density of states; (2) for smaller $E_F - E \leq 0.25 \text{ eV}$, the vertical TFTs with different barrier layers show nearly the same DOS in the order of $10^{19} \text{ eV}^{-1}\cdot\text{cm}^{-3}$, which proves nearly the same subthreshold slope of the two kinds of vertical TFTs; (3) for larger $E_F - E > 0.25 \text{ eV}$, the vertical TFT with Si_3N_4 barrier layer shows a lower DOS, especially when

$E_F - E = 0.4$ eV, the DOS of the Si_3N_4 barrier layer device decreases by one decade compared to the DOS of the device with SiO_2 barrier layer, which proves the greater field effect mobility of the device with Si_3N_4 barrier layer reported in table 1; (4) the DOS for the lateral TFT is much smaller than the DOS of the two vertical TFTs, in the smaller $E_F - E$ zone, the DOS is approximately $10^{18} \text{ eV}^{-1} \cdot \text{cm}^{-3}$, where for $E_F - E = 0.4$ eV, the DOS is ten times smaller than the DOS of vertical TFT with Si_3N_4 barrier layer, and one hundred times smaller than the DOS of vertical TFT with SiO_2 barrier layer. Indeed, strained and dangling bonds correspond respectively to shallow and deep traps, and two types of density distributions are taken into account: exponential band tail states near the mobility edge and Gaussian distribution with a maximum near the midgap [14]. From our DOS calculation, the vertical TFT with Si_3N_4 shows smaller DOS in comparison with the vertical TFT with SiO_2 barrier layer, and the lateral TFT shows smaller DOS than vertical TFTs, indicating a smaller density of strained bonds and dangling bonds, which is closely associated with the density of the grain boundaries in polycrystalline Si active layer. In addition, for the same DOS, the larger $E_F - E$ for the lateral TFT in comparison with vertical TFT indicates the closer of the tail states to the mobility edge, which is beneficial for enlarging the field effect mobility.

In order to evaluate the DOS calculated from the Suzuki method shown above, two extra methods are also proposed to show the DOS in the deep

trap regime and the shallow trap regime, respectively. The DOS in the deep trap regime is calculated from the simple subthreshold slope method, which adopts the relationship between the subthreshold slope and the deep trap density, and the relationship between the surface potential $u(x)$ and the applied gate voltage V_{GS} is shown below [15]:

$$SS = \ln 10 \frac{kT}{q} \frac{dV_{GS}}{du_a} \quad (5)$$

Figure 4(a) and 4(b) shows comparisons of the DOS calculated from the subthreshold slope method and the Suzuki method. Indeed, the DOS calculated from the subthreshold slope method is relevant to the subthreshold region that is approximately below the gate voltage of 4 V, and it is found to be consistent with the DOS calculated from the Suzuki method, indicating the accurate DOS distribution calculation. In addition, the subthreshold slope method gives more details of DOS in this subthreshold region. From this method, the DOS is calculated to range from $5.9 \times 10^{18} \text{ eV}^{-1} \cdot \text{cm}^{-3}$ to $1.59 \times 10^{19} \text{ eV}^{-1} \cdot \text{cm}^{-3}$ in the forward subthreshold region for vertical TFT with SiO_2 barrier layer, and this value is calculated to range from $4.99 \times 10^{18} \text{ eV}^{-1} \cdot \text{cm}^{-3}$ to $1.89 \times 10^{19} \text{ eV}^{-1} \cdot \text{cm}^{-3}$ for the vertical TFT with Si_3N_4 barrier layer. Therefore, nearly the same deep trap density is obtained again for the two kinds of vertical TFTs. However, with the further increase of the charge density in the channel layer, the DOS from the subthreshold slope method deviates from the DOS from Suzuki method. Nevertheless, using the subthreshold slope method, the higher DOS of

vertical TFTs are demonstrated again in comparison to the DOS of lateral TFT, as shown in figure 4(c).

In fact, the subthreshold slope is related to the synergistic effect of the bulk traps and the interface traps, which can be expressed as follows [16]:

$$SS = \ln 10 \frac{kT}{q} \left(1 + \frac{q}{C_i} (\sqrt{\varepsilon_a N_{bulk}} + q N_{int}) \right) = \ln 10 \frac{kT}{q} \left(1 + \frac{q^2}{C_i} N_{\square} \right) \quad (6)$$

Both of the deep bulk traps N_{bulk} and the interface traps N_{int} contribute to the trap density N_{\square} . For vertical TFTs, the larger subthreshold slope SS is due to the calculated trap density for the vertical TFT with SiO₂ barrier layer, the vertical TFT with Si₃N₄ barrier layer, and the lateral TFT are $4.07 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$, $3.55 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$, and $2.97 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$, respectively. Considering the accumulation layer thickness of approximately 10 nm, the calculated volume trap density can only be regarded as a rough estimate for the traps slightly above the Fermi energy.

The shallow DOS trap calculated from the Suzuki method is also verified by the Grünewald method, for which a different relationship between the surface potential u_a and the applied gate voltage U_{GS} is obtained [17]. The surface potential u_a as a function of gate voltage V_{GS} is calculated as:

$$\exp\left(\frac{eu_a}{kT}\right) - \frac{eu_a}{kT} - 1 = \frac{e}{kT} \frac{\varepsilon_i d_a}{\varepsilon_a d_i I_0} \left[U_{GS} I(U_{GS}) - \int_0^{U_{GS}} I(U'_{GS}) dU'_{GS} \right] \quad (7)$$

Where I_0 is the current at flat band condition, U_{GS} and $I(U_{GS})$ is the gate voltage relative to the flat band voltage, and the corresponding current. As shown in Figures 5(a)-5(c), for a shallow trap density, these two methods give almost the same DOS, the maximum DOS being in the order of $10^{22} \text{ eV}^{-1} \cdot \text{cm}^{-3}$ at the gate voltage of 25 V, which verifies the accuracy of the Suzuki method. However, in the deep trap density zone, these two methods show deviation, which might be due to the fluctuation of accuracy for the deep states zone.

3. Conclusion

In conclusion, vertical TFTs were fabricated based on low-temperature polycrystalline Si technology, involving two different barrier layers of SiO_2 and Si_3N_4 in order to minimize the off-state current. For the two types of vertical TFTs, similar electrical characteristics are obtained, where the field effect mobility is one order smaller than their lateral counterpart. The calculated DOS from Suzuki method shows similar deep trap density for the two types of vertical TFTs, and larger shallow trap density for the vertical TFT with SiO_2 barrier layer, whereas the vertical TFTs show larger DOS than lateral TFT. The subthreshold slope method validates the Suzuki method in the deep trap zone, and the Grünwald method can also show the accuracy of the Suzuki method in the DOS calculation. These methods provide an approach for DOS calculation independent of temperature-

related measurements, which may be advantageous in certain situations where temperature-dependent measurements are not possible [18].

Acknowledgement

This work was supported by the Natural Science Foundation of Jiangsu Province (BK20180762), and also sponsored by NUPTSF (Grant No. NY219099). The authors would like to thank Dr J. Lelannic for the realization of the SEM images of the devices. Members of the Microelectronics and Micro Sensors Department are also thanked for their contribution to the process and for their useful discussions.

Declaration of Interest Statement

There are no conflicts to declare.

References

- [1] Yueh-Hua Yu, Yuan-Jiang Lee, Yu-Hsuan Li, Chung-Hung Kuo, Chun-Huai Li, Yao-Jen Hsieh, Chun-Ting Liu, and Yi-Jan Emery Chen, *IEEE Transactions on Microwave and Techniques* 57(5), 1356 (2009).
- [2] Han Jin-Woo, Ryu Seong-Wan, Kim Dong-Hyun, Choi Yang-Kyu, *IEEE Transactions on Electron Devices* 57, 601 (2010).
- [3] Lu JP, Van Schuylenbergh K, Ho J, Wang Y, Boyce JB, Street RA, *Applied Physics Letters* 80, 4656 (2002).
- [4] Inoue Satoshi, Utsunomiya Sumio, Saeki Takayuki, Shimoda Tatsuya, *IEEE Transactions on Electron Devices* 49, 1353 (2002).
- [5] Park Kee Chan, Jeon Jae-Hong, Kimc YoungIl, Choi Jae Beom, Chang Young-Jin, Zhan ZhiFeng, ChiWoo Kim, *Solid-State Electronics* 52, 1691 (2008).
- [6] Olivier Bonnaud, Peng Zhang, Emmanuel Jacques, Régis Rogel, *ECS Transactions* 37 (1), 29 (2011).
- [7] P. Zhang, E. Jacques, R. Rogel, N. Coulon, O. Bonnaud, *Solid-State Electronics* 79, 26 (2013).
- [8] P. Zhang, E. Jacques, R. Rogel, O. Bonnaud, *Solid-State Electronics* 86, 1(2013).
- [9] A. Mercha, J. Rhayem, L. Pichon. M. Valenza, J. M. Routoure, R. Carin, O. Bonnaud, D. Rigaud, *Microelectronics Reliability* 40, 1891, (2000).

- [10] Wong HS, White MH, Krutsick TJ, Booth RV, Solid-State Electronics 30, 953 (1987).
- [11] B. Le Borgne, L. Pichon, M. Thomas, and A. C. Salaun, Physica Status Solidi A, 1 (2016).
- [12] J. G. Fossum, A. Ortiz-Conde, IEEE Transactions on Electron Devices 30(8), 933 (1983).
- [13] C. A. Dimitriadis, F. V. Farmakis, J. Brini, and G. Kamarinos, Journal of Applied Physics 88(5), 2648 (2000).
- [14] A. Aziz, O. Bonnaud, H. Lhermite and F. Raoult, IEEE transactions on Electron Devices, 41(2), 204 (1994).
- [15] Tetsufumi Kawamura, Hiroyuki Uchiyama, Shinichi Saito, Hironori Wakana, Toshiyuki Mine, Mutsuko Hatano, Applied Physics Letters 106, 013504 (2015).
- [16] Wolfgang L. Kalb, and Bertram Batlogg, Physical Review B 81, 035327 (2010).
- [17] M. Grünewald, P. Thomas, D. Würtz, Physica Status Solidi (b) 100, K139 (1980).
- [18] W. L. Kalb, F. Meier, K. Mattenberger, and B. Batlogg, Physical Review B 76, 184112 (2007).

Captions:

Figure 1: Images of the vertical TFT device, (a) the first vertical TFT configuration in previous works, (b) the improved vertical TFT configuration, (c) the SEM image of the sidewall with a 100 nm SiO_2 barrier layer, nonuniform etching results in a rugged sidewall, (d) the SEM image of the sidewall with a 200 nm Si_3N_4 barrier layer, the smaller etching selectivity results in a flatter sidewall, even though with a recess at the Si_3N_4 layer, and (e) the SEM image of the improved four-tooth device, source, drain, and gate are illustrated.

Figure 2: Electrical characteristics of the vertical TFTs, (a) transfer characteristics of the vertical TFT with SiO_2 barrier layer, (b) transfer characteristics of the vertical TFT with Si_3N_4 barrier layer, (c) access resistance deduction for vertical TFT with Si_3N_4 barrier layer, (d) second-derivative method to extract the threshold voltage for the vertical TFT with SiO_2 barrier layer, the threshold voltage is assumed to be 4.4 V, and (e) second-derivative method to extract the threshold voltage for the vertical TFT with Si_3N_4 barrier layer, the threshold voltage is also assumed to be 4.4 V.

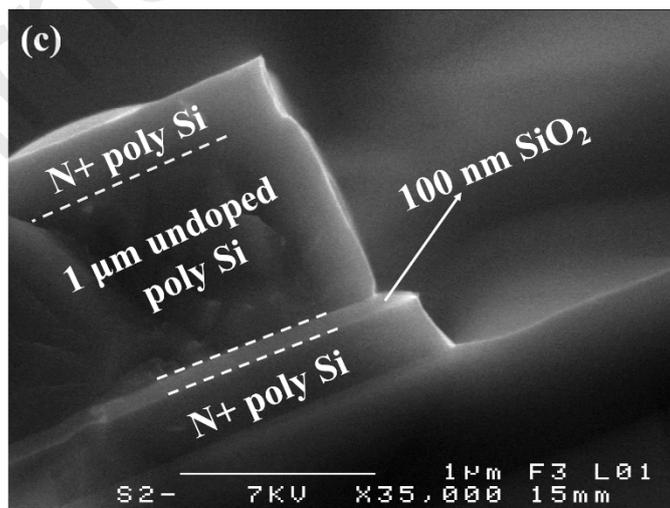
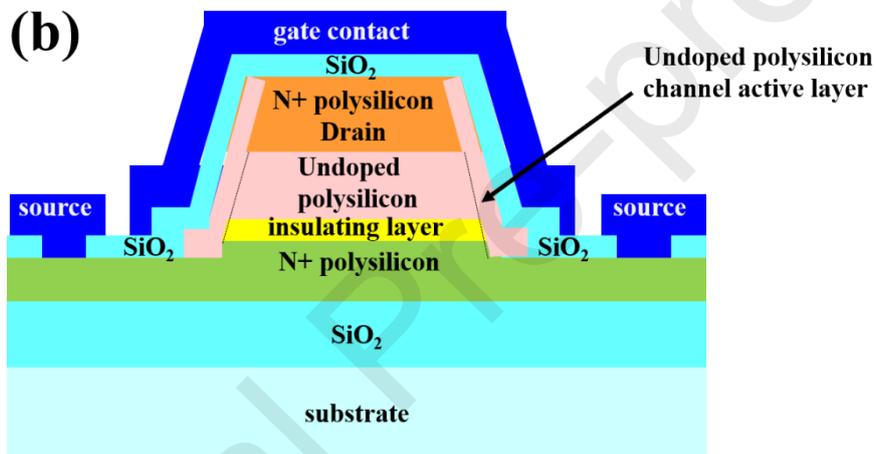
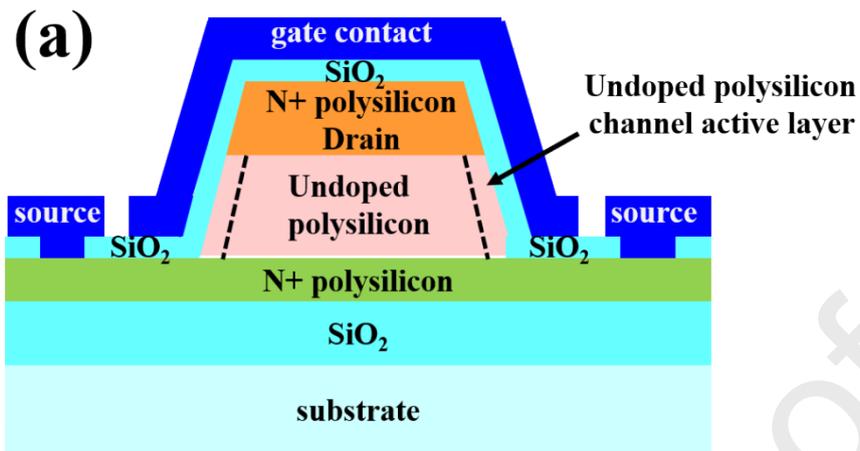
Figure 3: Transfer characteristics and DOS calculation by Suzuki method for the vertical TFTs, (a) transfer characteristics of the vertical TFTs (at

$V_{DS}=0.1V$) and lateral TFT (at $V_{DS}=1V$), (b) DOS calculation for vertical TFTs and lateral TFT by Suzuki method.

Figure 4: Subthreshold slope method for DOS calculation, (a) DOS calculated for the vertical TFT with SiO_2 barrier layer, (b) DOS calculated for the vertical TFT with Si_3N_4 barrier layer, (c) DOS comparison for vertical TFTs and lateral TFT.

Figure 5: Grünewald method for DOS calculation, (a) DOS calculated by two methods for vertical TFTs with SiO_2 barrier, (b) DOS calculated by two methods for vertical TFTs with Si_3N_4 barrier, (c) DOS calculated by two methods for lateral TFT.

Figure 1



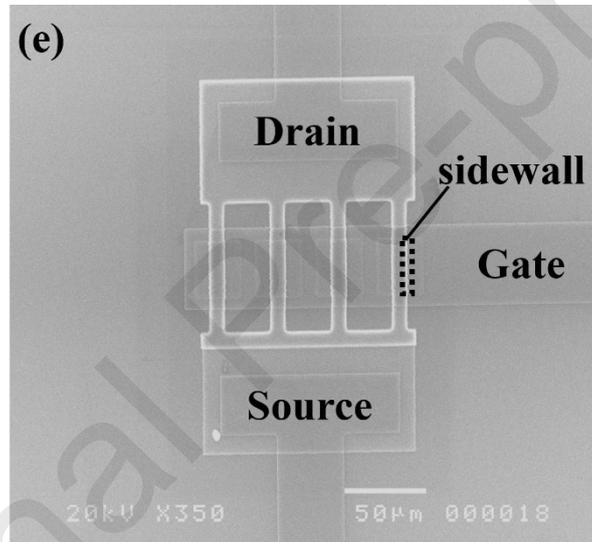
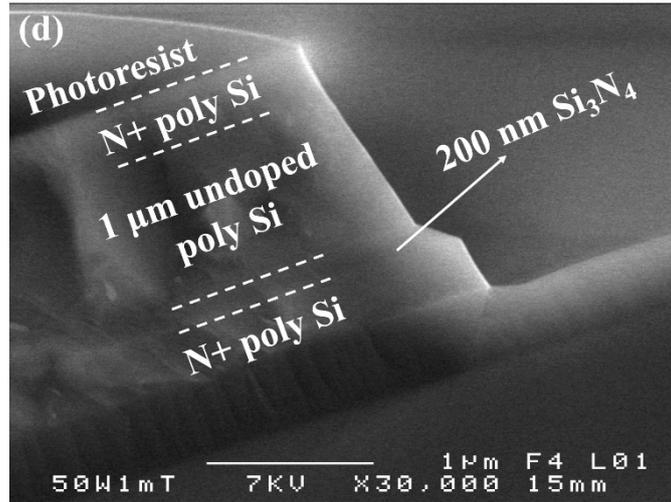
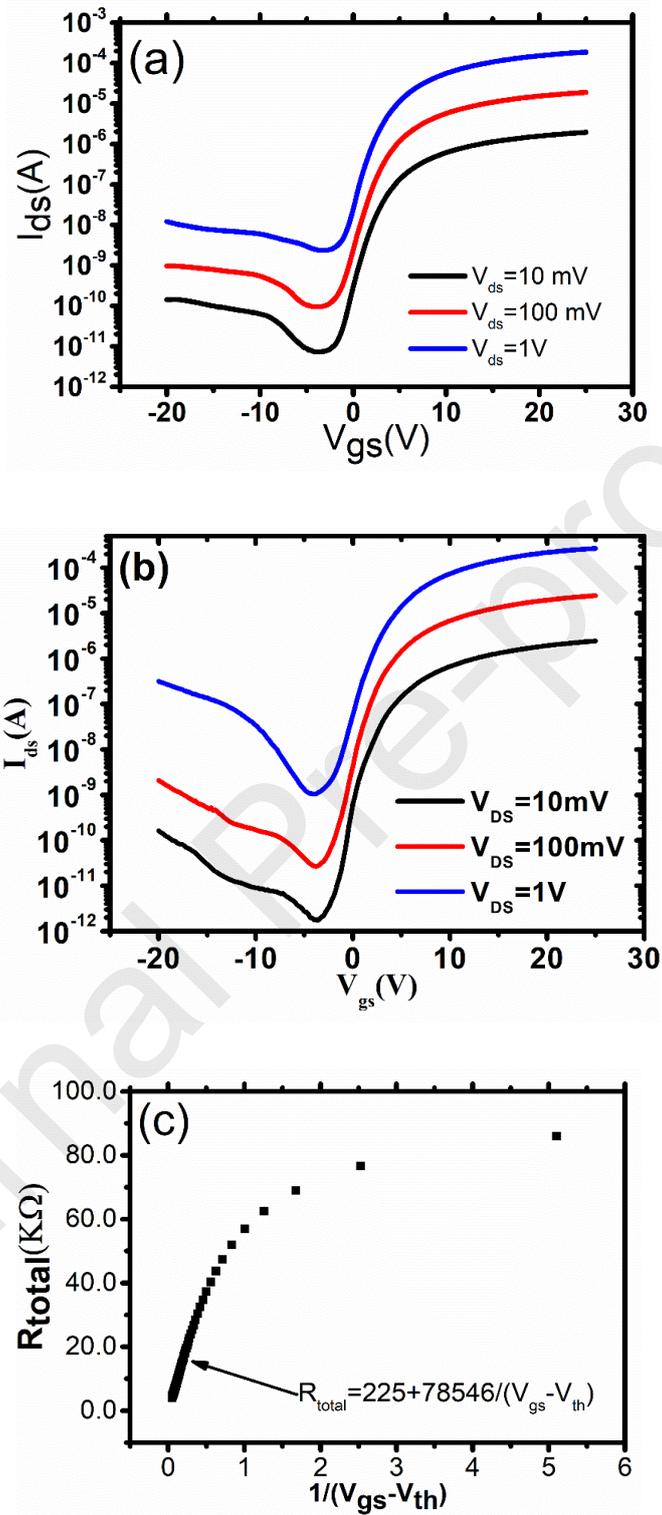


Figure 2



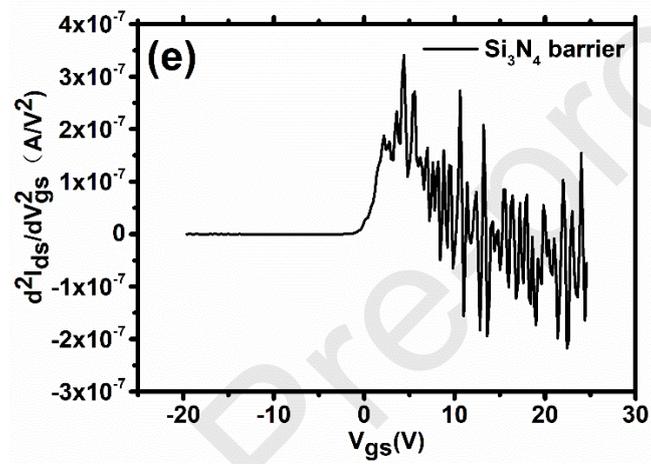
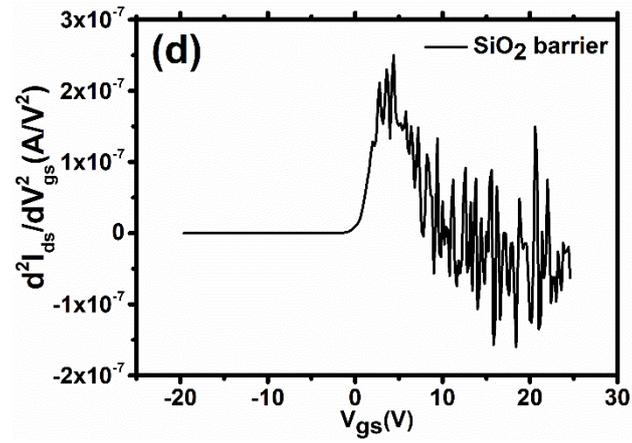


Table 1: Electrical parameters for vertical TFTs and lateral TFT deduced from transfer characteristics.

Type	V_{ds} (V)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	g_m (μS)	V_{th} (V)	SS (V/dec)	μ_{FE} ($cm^2/V \cdot s$)
SiO ₂ barrier layer	0.01	1.94×10^{-6}	7.30×10^{-12}	2.66×10^5	0.104	4.022	1.04	11.6
	0.1	1.88×10^{-5}	9.49×10^{-11}	1.95×10^5	0.984	4.085	1.18	11.0
	1	1.86×10^{-4}	2.35×10^{-9}	0.79×10^5	9.855	3.779	1.12	11.0
Si ₃ N ₄ barrier layer	0.01	2.44×10^{-6}	1.73×10^{-12}	1.41×10^6	0.124	4.369	0.79	15.1
	0.1	2.44×10^{-5}	2.67×10^{-11}	0.914×10^6	1.256	4.354	1.03	15.3
	1	2.67×10^{-4}	1.05×10^{-9}	2.54×10^5	14.27	4.133	1.27	17.4
Lateral TFT	1	1.26×10^{-4}	1.25×10^{-11}	1.01×10^7	5.615	3.675	0.87	81.1

Figure 3

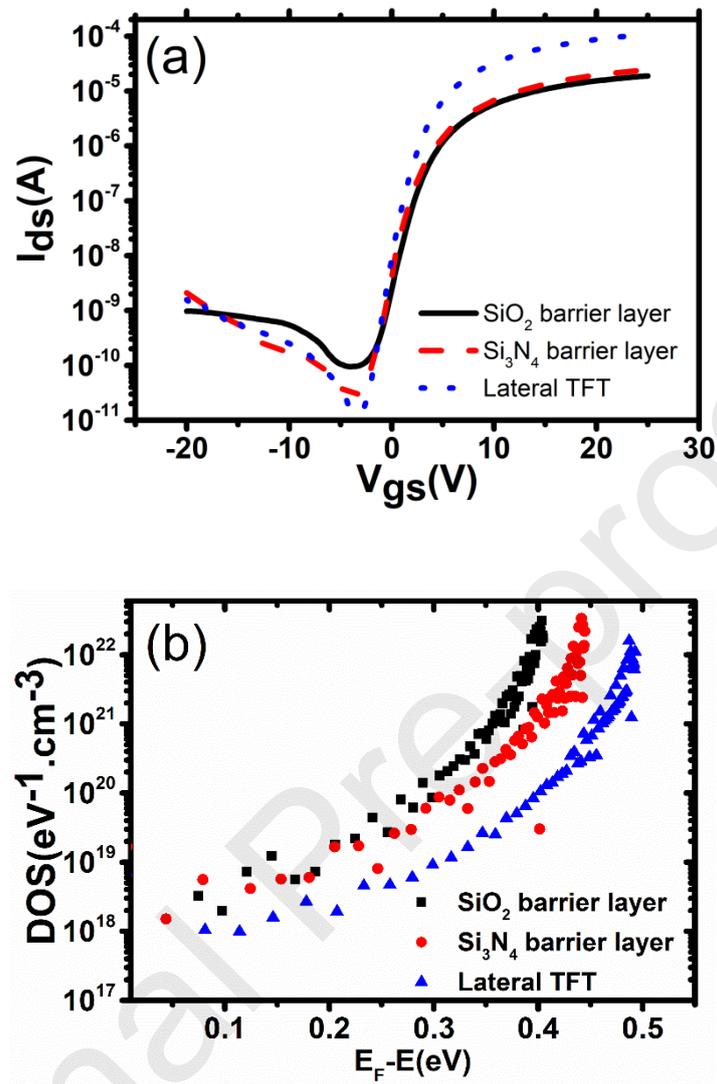


Figure 4

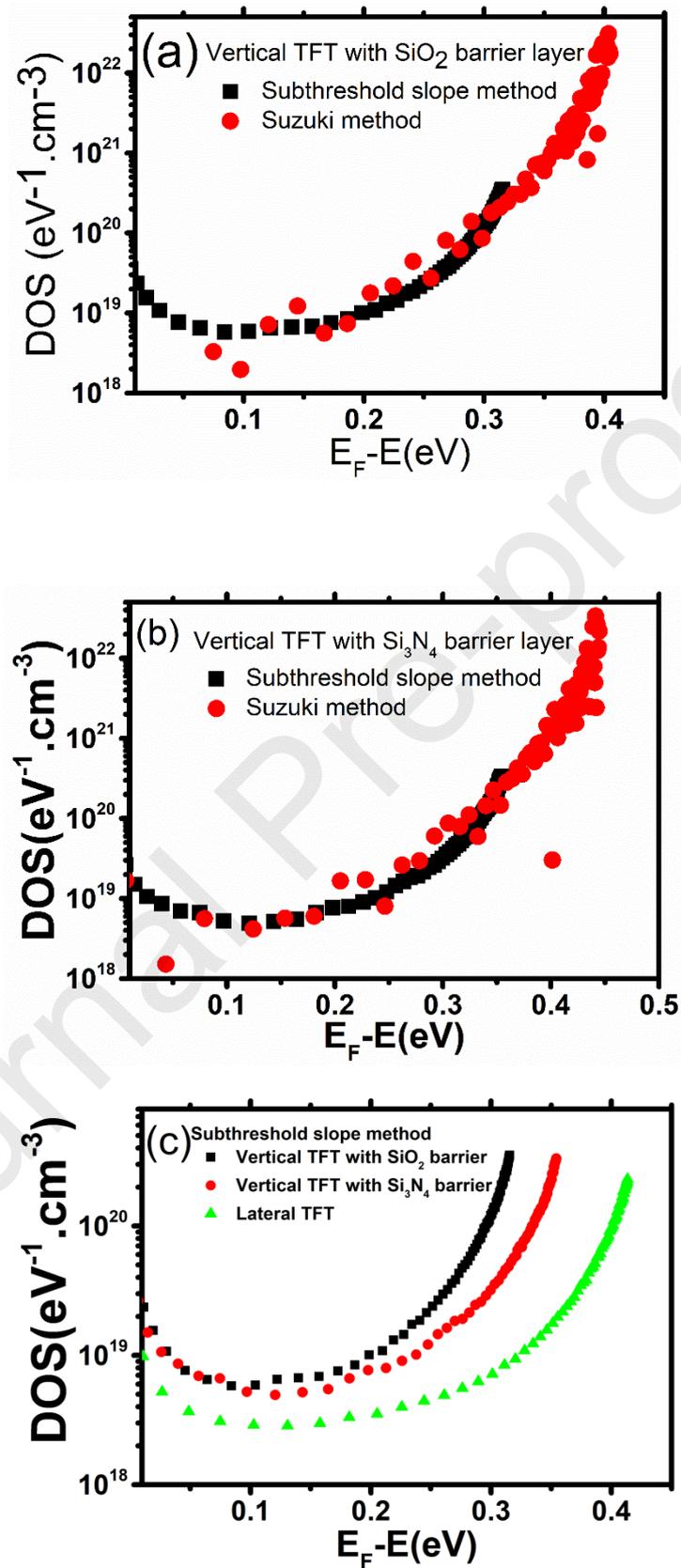
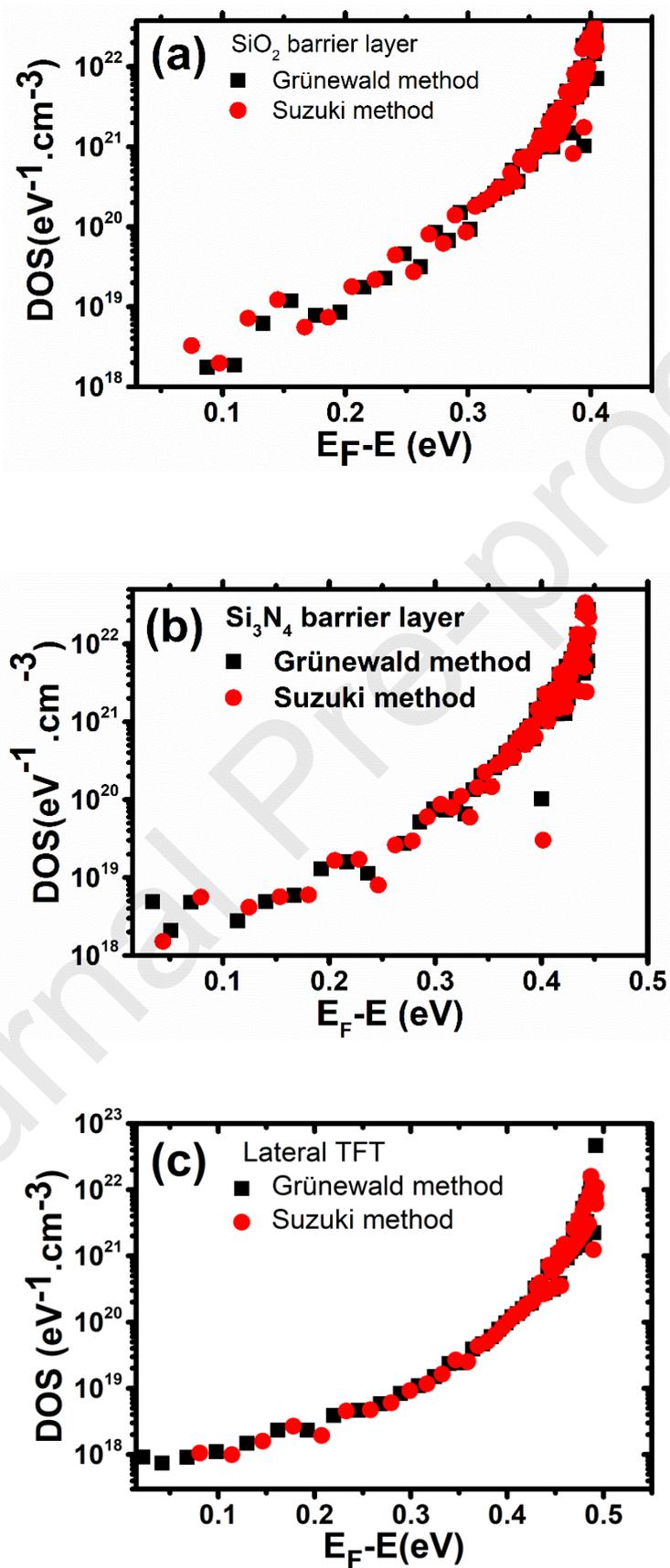


Figure 5



Dr. Peng ZHANG has received his bachelor of Science degree in School of Physics Science and Technology in Soochow University in 2006, and then he has received his master of engineering degree in the School of Electronic Science and Engineering in Southeast University in 2009, and he has pursued his study as a PhD student during 2009 to 2012 in Institut d'Électronique et de Télécommunications de Rennes (IETR) in University of Rennes 1, and since 2013 he has worked in the College of Electronic and Optical Engineering in Nanjing University of Posts and Telecommunications. His research fields include the inorganic and organic thin film transistors, the nonvolatile memory based on organic thin film transistors, and so forth.

1. The rough interface of the active layer and the rugged sidewall adversely affects the electrical characteristics of vertical TFTs;
2. The vertical TFT with Si_3N_4 barrier layer shows same threshold voltage and subthreshold slope, however, a larger transconductance and field effect mobility in comparison to the vertical TFT with SiO_2 barrier layer;
3. The electrical parameters of the vertical TFTs and lateral TFT are analyzed by density of states (DOS) using Suzuki method, subthreshold slope method, and Grünwald method.



Journal Pre-proofs