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Communication

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Abstract: This paper presents the first graphene radiofrequency (RF) monolithic integrated balun circuit. It is composed of four integrated graphene field effect transistors (FETs). This innovative active balun concept takes advantage of the GFET ambipolar behavior. It is realized using bilayer epitaxial graphene on advanced silicon carbide (SiC) based GFET technology having RF performances of about 20GHz. Balun circuit measurement demonstrates its high frequency capability. An upper limit of 6 GHz has been achieved when considering a phase difference lower than 10° and a magnitude of amplitude imbalance less than 0.5dB. Hence, this circuit topology shows excellent performances with large broadband performances and a functionality up to one third of the transit frequency of the transistor.

Keywords: graphene, microwave. MMIC, integrated circuits, active balun, 2D materials.

1. Introduction

Research in graphene electronics has been extensively directed to the development of RF transistors [1–9]. Transistors are the basic building blocks of integrated circuits; they determine their maximal operational frequencies and overall performances. Some RF and millimeter wave circuits based on graphene transistors have been reported with for example, a low noise amplifier (LNA) and a mixer working around 10 to 20GHz [10], ring oscillator [11,12], graphene radio frequency receiver integrated circuit [13] and a 200GHz integrated resistive subharmonic mixer based on a single chemical vapour deposition (CVD) G-FET [2]. One of the key concepts for circuit design at very high frequency is the use of differential electronic signals [14]. From a circuit design point of view, the differential topologies have very interesting properties, such as providing immunity to common mode noise couplings and crosstalk through the substrate and supply rails. In addition, at millimeter-wave frequencies, the differential topologies alleviate the negative impact of the bonding wire inductance or the flip-chip bump inductance on the gain, the output power, and the stability of amplifiers [14].

To take advantage of the differential topology concept, the device that is required is the balun or splitter circuit that transform the single-ended signals (unbalanced) into the differential signals (balanced) and vice versa. Thus, the balun is a device that consists of an unbalanced single-ended input port and two balanced output ports. The main figure of merit (FOM) of the balun are the phase

error and the amplitude difference between the output balanced ports. Finally, specifically for the active balun, the gain is also an important FOM. In [15], we proposed two balun architectures based on Graphene FET specificities. The basic working principle of these circuits cell were demonstrated but this demonstration was limited to very low frequencies (<10MHz). The circuit was tested by adding external elements such as lumped resistors, basic coaxial cables and DC probes; thus preventing the evaluation of the high frequency figures of merit (FOM) of the circuit cell.

In this paper and for the first time, we have designed and fabricated a RF monolithic integrated balun circuit using a SiC bilayer graphene FET technology. Our MMIC balun consists of four transistors, two of them split the single ended signal in to two differential signals, the other two acts as active loads, their role is to ensure optimal biasing of the other two transistors.

The SiC substrate is well suited for high-frequency applications: it is highly insulating ensuring low ohmic losses at high-frequency and has high thermal conductivity, that is advantageous for thermal management. Here we choose graphene bilayer graphene grown by CVD since this technique produce wafer scale graphene with uniform coverage of the substrate, and is generally more homogenous than single layer. First part of the paper describes the technology used and presents transistor performances. Second, the balun topology and layout is presented together with the measurement results. Finally, the FOM of the GFET balun is benchmarked and compared to the state of the art conventional baluns designed in Silicon, GaAs and GaN technologies.

2. Materials and Methods

2.1. Graphene growth and properties

Epitaxial graphene has been grown by chemical vapor deposition (CVD) on 500µm thick and high resistivity 6H-SiC (0001) substrate. Commercial horizontal CVD hot wall Aixtron VP508 reactor with RF generator for heating is used. Before the growth, in-situ etching of the SiC surface was carried out in hydrogen atmosphere at 1600°C and chamber pressure of 100 mbar. The epitaxial carbon films were deposited using propane gas as carbon precursor. The method used is based on high temperature and low argon pressure CVD by creating dynamic conditions of the laminar flow of argon which protect the SiC substrate against Si sublimation and enable mass transport of propane to the SiC surface, thus realizing graphene epitaxy as reported in [16–18]. Besides the large-scale fabrication, the main advantage of CVD on SiC is to avoid the transfer from copper and improve electronic properties of the material by using hydrogen intercalation as reported by Ciuk et al. [18]. One of the advantages of the bilayer graphene on SiC substrate is to overcome the lack of the band gap besides to other possibilities reported in the literature such as introducing defects, doping, strain and chemical bounding with substrate [Zhou2007-Xu2018]. Furthermore, the bilayer graphene field effect transistors GFET on SiC has demonstrated better performances than monolayer GFET [He2016].

The growth process was followed by in-situ hydrogen intercalation at 1000°C in 900mbar Ar atmosphere. The growth parameters are optimized to achieve a bilayer graphene. The initial carrier density and the mobility was extracted from non-contact Terahertz spectroscopic measurement and estimated around +8.3x10^{12}cm-2 and 850cm².V-1s-1 respectively [19].

Raman spectroscopy was performed using the HORIBA Jobin-Yvon lab system at a laser wavelength of 473 nm, using 1 µm laser spot size and filters to deliver power less than 0.1 mW and x100 objective lens to measure different position of the sample.

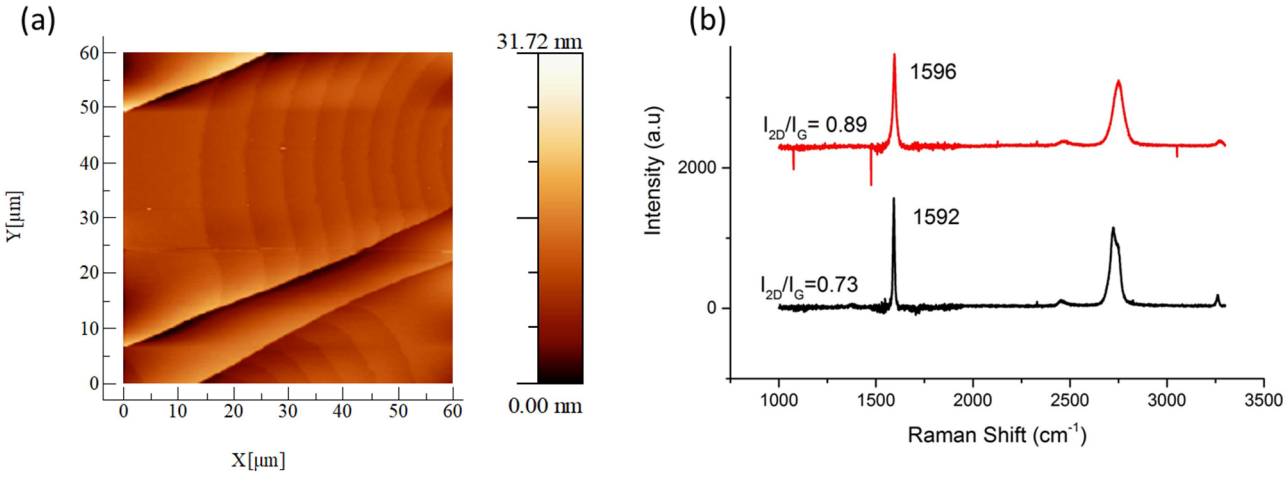
2.2. Circuit fabrication

Monolithically integrated balun circuits containing four graphene field effect transistors each were fabricated on a 15x15mm² SiC wafer. First, we define the alignment marks. Then we etch the graphene channel and holes in the contacts region for improving contact resistance, as reported previously [20,21]. The source and drain contacts are obtained by the e-beam followed by lift-off

process after evaporating 1.5nm of nickel and 30nm of gold. Here the 1.5nm thin layer of nickel is used to improve the metal adhesion on the surface. Then, dual T-gate with gate length (Lg) were defined by e-beam using a three layers poly-meta-methacrylate resist. After, the development of these multilayers' resists, the gate oxide is obtained by depositing four times 2 nm of evaporated aluminum, following by oxidation in ambient air during 24 hours. Finally, the coplanar access and interconnections between transistors are fabricated (Ni/Au 50nm/300nm). The fabricated circuits is presented in figure 2.

3. Results

We first discuss the graphene materials used in this work. In Figure 1a presents the atomic force microscopy (AFM) image of 60 x 60 μm² graphene surface on SiC. It shows the presence of SiC steps which are several tens of μm wide. Two typical Raman spectra measured on the sample are illustrated on figure 1b, after subtraction of the Raman signal coming from the SiC. The G and 2D peaks, a characteristic feature of graphene, are clearly visible (with G peak at 1596 and 1592 cm-1) [22]. The D peak intensity is either not detected or much smaller than our G peak, indicating that disorder or defects are absent or very present in very small mount [23]. The widths of 2D peak and the low value of the radio I2D/IG < 1 indicates that the graphene is mainly a bilayer.



4.

5. **Figure 1.** (a) 60 x 60 μm² AFM image of the graphene on SiC which we used for balun circuits (b) Two representative Raman spectra of our graphene, the SiC background Raman signal has been subtracted.

5.1. Circuit description

The GFET-Balun is realized using two active GFET transistors (T1 and T2) where the sources are connected together and two loads (transistors $T_{AL}1$ and $T_{AL}2$) are tied to the drains of T1 and T2, and connected to the power supplies VDD and VSS, respectively (see figure 2b). In comparison to [15], lumped resistors are replaced by integrated active loads using transistors where the gate is connected to the source. The input signal is applied to the gates of T1 and T2 (both gates are connected together). The gate-source voltage of the graphene transistors is hence equal to VGS0 + Vac, where VGS0 is the DC-offset voltage used for accurately setting the quiescent point. The balanced output signals are measured at the drains. The circuit has been simulated with the compact model described in [24,25] and also applying a mixed SPICE and electromagnetic simulation through ADS-Momentum. In the previous graphene simulated circuit [25] and considering the former available technology developed at University of Lille [15], circuit shows performances in the GHz range with a difference of phase lower than 10° up to 1.2GHz.

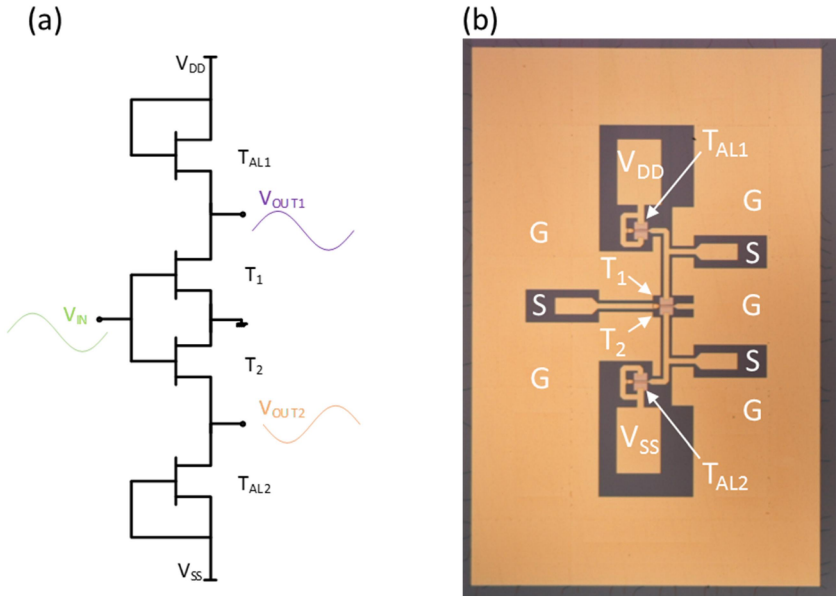


Figure 2. Schematic circuit diagram of the balun and photography of the balun highlighting its layout. Chip size is 0.19mm².

5.2. *GFET description*

The transistor channel is composed mainly of a bilayer graphene. The gate length is about 240 nm. A top gate is used with an insulator thickness of about 15 nm made of Al2O3. The width of each device 24 µm. The DC ID-VGS and its associated transconductance characteristics of a GFET, as well as the AC- characteristics were measured on a transistor situated at close proximity of the balun for minimal dispersion. The influence of the pads has been removed through appropriated test-structures and de-embedding. Maximum transconductance is about 5mS. The gate-source capacitance CGS is about 26fF while the gate-drain capacitance CGD is about 8fF. The device is characterized by a cut-off frequency of 19GHz and a maximum oscillation frequency of 6GHz.

5.3. *Balun circuit characterization*

First functionality tests have been performed thanks to time domain measurement using a RF source set at 100MHz and -10dBm. One single RF probes is used at the input while a differential probe is used at the output.

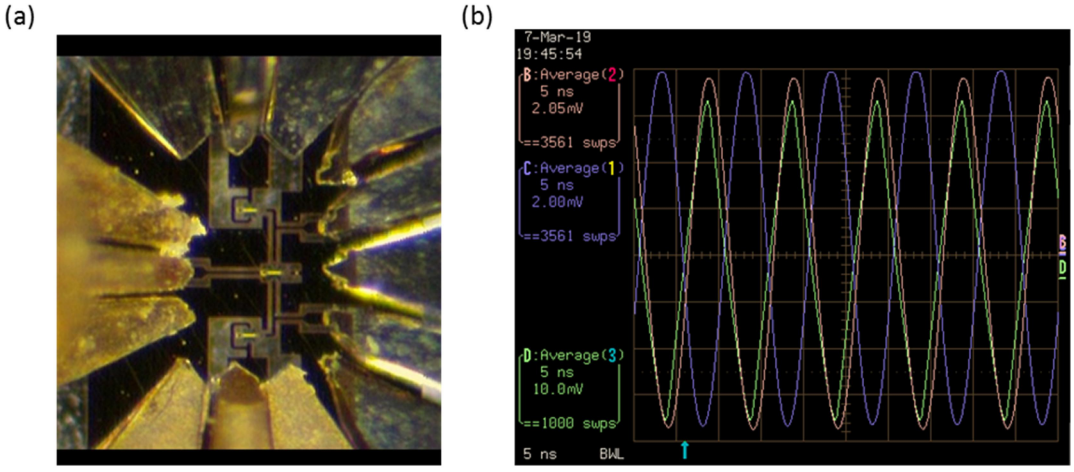


Figure 3. (a) Photography of the balun under measurement condition. (b) Oscilloscope measurement when applying a sinusoidal input voltage with an amplitude of 32mV at the input (channel D) and sensing the two outputs (channel B and C).

Two other RF probes are used for convenience to apply the DC bias. +2V and -2V are respectively applied on VDD and VSS. Also, 2V is applied on the input thanks to a bias tee. A photography of the balun under measurement conditions is shown in figure 3a.

Scope measurements are presented in Fig. 3b highlighting the functionality of the circuit with 180° phase shift between the two outputs. In that first measurement setup, the measurement is not calibrated and does not allow high frequency measurement. That's the reason why a 4 port PNAX vector network analyzer (VNA) is used in the following part to obtain calibrated data at the probe level. In order to perform the differential measurement with the VNA, the intermediate frequency is set to 100Hz and the input power is fixed to -10dBm.

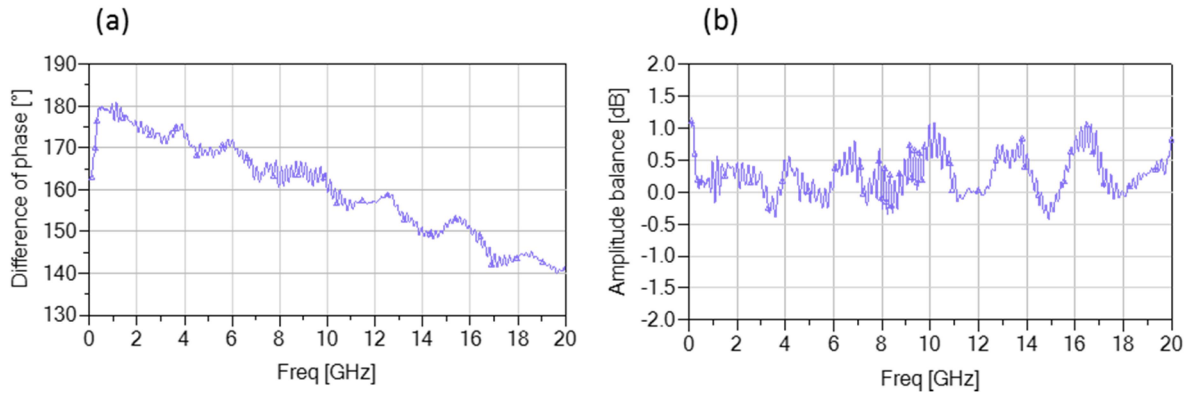


Figure 4. Three port S parameters measurement up to 20 GHz using a PNAX: (a) phase difference between the two outputs; (b) amplitude balance between the two outputs.

The setup is calibrated using a calibration kit dedicated to differential probes. Measurements reveals that the two outputs signal have a phase difference of 180° up to the GHz range (see Fig. 4a). This difference decreases to 170° at 6GHz. The output signals are attenuated of about 20dB with an amplitude imbalance lower than 0.5dB below 6GHz (see Fig. 4b). The bias current is 40 mA giving a power consumption of 160mW. The strong attenuation of 20 dB is directly correlated to the transistors' performances and especially to the high output conductance gDS, a specific weakness of graphene devices. Also, the power consumption can be optimized by reducing gate width to obtain the optimal tradeoff between power consumption and output impedance of the balun.

6. Discussion

6.1. Comparison with state of the art

Finally, the balun circuit is compared to the state of the art of active baluns made with different technologies such as silicon [26], SiGe [27], GaAs [28] and GaN [29]. These publications are chosen to have a similar technology gate length than the graphene technology used in this paper ranging from 0.18 to 0.5µm. The transit frequencies of these technologies are also in the same range spanning from about 20 and up to 40GHz. Moreover, the baluns are designed for broadband applications and below 16GHz. The graphene balun presented in this work have comparable performance in terms of phase difference and amplitude balance compared to the industrial technology despites its low maturity. As mentioned early, the major drawback is due to the losses in the graphene balun which is intrinsically correlated to the transistor performances and not to the circuit topology itself.

Table 1. Broad-band active balun state of the art, FBW=frequency bandwidth

	Technology	Phase difference	Amplitude balance	Loss/Gain	IC Area mm²
This work	Graphene 300nm fT=19 GHz	<10° FBW< 6GHz	<0.5dB	-20dB	0.16
[29]	GaN, 0.25µm (high power) typical fT=25 GHz	<10° FBW:2.4-6 GHz	<0.4dB	+7.4dB	
[26]	Si, 0.18µm	<3° FBW< 8GHz	2dB at 8 GHz	-	0.38
[28]	0.5µm GaAs fT=35 GHz fMAX=70 GHz [30]	<8° FBW:1-16 GHz-	1 dB FBW 1-16 GHz-	-1 to 2 dB	0.36
[27]	SiGe (0.8µm) fT=35 GHz	<0.9° FBW:0.6-4.1	0.1dB FBW:0.6-4.1	7 to 10 dB	1.44

7. Conclusion

A graphene-based broadband balun monolithically integrated circuit working up to 6GHz has based on SiC graphene bilayer technology has been demonstrated. The circuit contains four individual transistors. The graphene-based balun performances are compared to state of the art baluns on semiconducting technologies having similar RF-characteristics. This comparison accounts for frequency bandwidth, phase difference, amplitude balance and die area. Comparable performances are achieved except of gain. The circuit performances are intrinsically correlated to the transistor performances. For the graphene-based topology, the circuit works up to one third of the transistor's transit frequency which is suitable for the new 5G NR sub-6 standard.

The balun concept based on the ambipolar behavior of the GFET that has been demonstrated in this paper may be replicated on other promising materials such as TMDs materials, carbon nanotube FETs or other ambipolar FETs.

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