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2 **A broadband active microwave monolithically** 3 **integrated circuit balun in graphene technology**

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14 **Abstract:** This paper presents the first graphene radiofrequency (RF) monolithic integrated balun
15 circuit. It is composed of four integrated graphene field effect transistors (FETs). This innovative
16 active balun concept takes advantage of the GFET ambipolar behavior. It is realized using bilayer
17 epitaxial graphene on advanced silicon carbide (SiC) based GFET technology having RF
18 performances of about 20GHz. Balun circuit measurement demonstrates its high frequency
19 capability. An upper limit of 6 GHz has been achieved when considering a phase difference lower
20 than 10° and a magnitude of amplitude imbalance less than 0.5dB. Hence, this circuit topology
21 shows excellent performances with large broadband performances and a functionality up to one
22 third of the transit frequency of the transistor.

23 **Keywords:** graphene, microwave, MMIC, integrated circuits, active balun, 2D materials.
24

25 **1. Introduction**

26 Research in graphene electronics has been extensively directed to the development of RF
27 transistors [1–9]. Transistors are the basic building blocks of integrated circuits; they determine their
28 maximal operational frequencies and overall performances. Some RF and millimeter wave circuits
29 based on graphene transistors have been reported with for example, a low noise amplifier (LNA) and
30 a mixer working around 10 to 20GHz [10], ring oscillator [11,12], graphene radio frequency receiver
31 integrated circuit [13] and a 200GHz integrated resistive subharmonic mixer based on a single
32 chemical vapour deposition (CVD) G-FET [2]. One of the key concepts for circuit design at very high
33 frequency is the use of differential electronic signals [14]. From a circuit design point of view, the
34 differential topologies have very interesting properties, such as providing immunity to common
35 mode noise couplings and crosstalk through the substrate and supply rails. In addition, at millimeter-
36 wave frequencies, the differential topologies alleviate the negative impact of the bonding wire
37 inductance or the flip-chip bump inductance on the gain, the output power, and the stability of
38 amplifiers [14].

39 To take advantage of the differential topology concept, the device that is required is the balun
40 or splitter circuit that transform the single-ended signals (unbalanced) into the differential signals
41 (balanced) and vice versa. Thus, the balun is a device that consists of an unbalanced single-ended
42 input port and two balanced output ports. The main figure of merit (FOM) of the balun are the phase

43 error and the amplitude difference between the output balanced ports. Finally, specifically for the
44 active balun, the gain is also an important FOM. In [15], we proposed two balun architectures based
45 on Graphene FET specificities. The basic working principle of these circuits cell were demonstrated
46 but this demonstration was limited to very low frequencies (<10MHz). The circuit was tested by
47 adding external elements such as lumped resistors, basic coaxial cables and DC probes; thus
48 preventing the evaluation of the high frequency figures of merit (FOM) of the circuit cell.

49 In this paper and for the first time, we have designed and fabricated a RF monolithic integrated
50 balun circuit using a SiC bilayer graphene FET technology. Our MMIC balun consists of four
51 transistors, two of them split the single ended signal in to two differential signals, the other two acts
52 as active loads, their role is to ensure optimal biasing of the other two transistors.

53 The SiC substrate is well suited for high-frequency applications: it is highly insulating ensuring
54 low ohmic losses at high-frequency and has high thermal conductivity, that is advantageous for
55 thermal management. Here we choose graphene bilayer graphene grown by CVD since this
56 technique produce wafer scale graphene with uniform coverage of the substrate, and is generally
57 more homogenous than single layer. First part of the paper describes the technology used and
58 presents transistor performances. Second, the balun topology and layout is presented together with
59 the measurement results. Finally, the FOM of the GFET balun is benchmarked and compared to the
60 state of the art conventional baluns designed in Silicon, GaAs and GaN technologies.

61 2. Materials and Methods

62 2.1. Graphene growth and properties

63
64 Epitaxial graphene has been grown by chemical vapor deposition (CVD) on 500 μ m thick and
65 high resistivity 6H-SiC (0001) substrate. Commercial horizontal CVD hot wall Aixtron VP508 reactor
66 with RF generator for heating is used. Before the growth, in-situ etching of the SiC surface was carried
67 out in hydrogen atmosphere at 1600°C and chamber pressure of 100 mbar. The epitaxial carbon films
68 were deposited using propane gas as carbon precursor. The method used is based on high
69 temperature and low argon pressure CVD by creating dynamic conditions of the laminar flow of
70 argon which protect the SiC substrate against Si sublimation and enable mass transport of propane
71 to the SiC surface, thus realizing graphene epitaxy as reported in [16–18]. Besides the large-scale
72 fabrication, the main advantage of CVD on SiC is to avoid the transfer from copper and improve
73 electronic properties of the material by using hydrogen intercalation as reported by Ciuk et al. [18].
74 One of the advantages of the bilayer graphene on SiC substrate is to overcome the lack of the band gap besides
75 to other possibilities reported in the literature such as introducing defects, doping, strain and chemical bonding
76 with substrate [Zhou2007-Xu2018]. Furthermore, the bilayer graphene field effect transistors GFET on SiC has
77 demonstrated better performances than monolayer GFET [He2016].

78 The growth process was followed by in-situ hydrogen intercalation at 1000°C in 900mbar Ar
79 atmosphere. The growth parameters are optimized to achieve a bilayer graphene. The initial carrier
80 density and the mobility was extracted from non-contact Terahertz spectroscopic measurement and
81 estimated around $+8.3 \times 10^{12} \text{cm}^{-2}$ and $850 \text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ respectively [19].

82 Raman spectroscopy was performed using the HORIBA Jobin-Yvon lab system at a laser
83 wavelength of 473 nm, using 1 μ m laser spot size and filters to deliver power less than 0.1 mW and
84 x100 objective lens to measure different position of the sample.

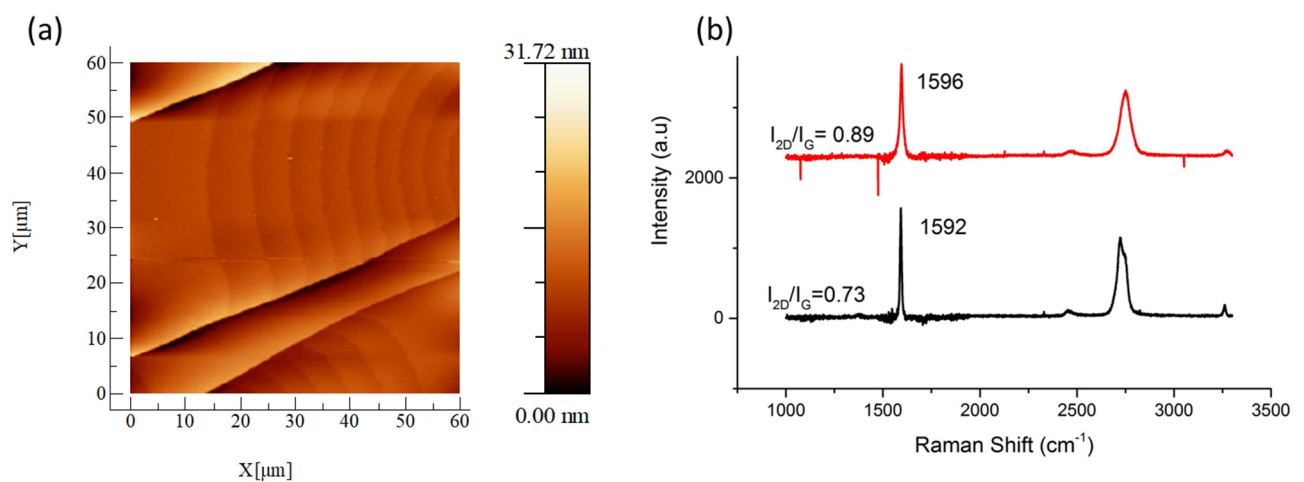
85 2.2. Circuit fabrication

86
87 Monolithically integrated balun circuits containing four graphene field effect transistors each
88 were fabricated on a 15x15mm² SiC wafer. First, we define the alignment marks. Then we etch the
89 graphene channel and holes in the contacts region for improving contact resistance, as reported
90 previously [20,21]. The source and drain contacts are obtained by the e-beam followed by lift-off

91 process after evaporating 1.5nm of nickel and 30nm of gold. Here the 1.5nm thin layer of nickel is
 92 used to improve the metal adhesion on the surface. Then, dual T-gate with gate length (L_g) were
 93 defined by e-beam using a three layers poly-meta-methacrylate resist. After, the development of these
 94 multilayers' resists, the gate oxide is obtained by depositing four times 2 nm of evaporated
 95 aluminum, following by oxidation in ambient air during 24 hours. Finally, the coplanar access and
 96 interconnections between transistors are fabricated (Ni/Au 50nm/300nm). The fabricated circuits is
 97 presented in figure 2.

98 3. Results

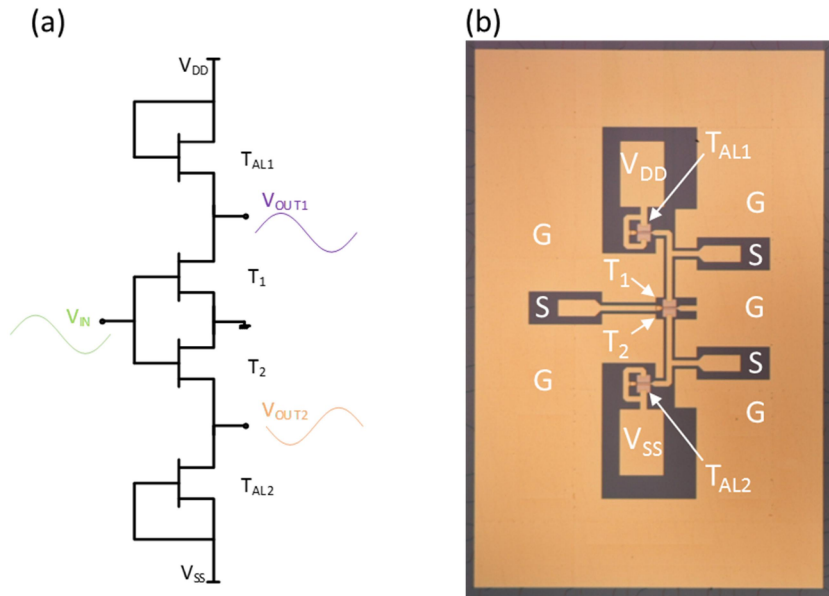
99 We first discuss the graphene materials used in this work. In Figure 1a presents the atomic force
 100 microscopy (AFM) image of $60 \times 60 \mu\text{m}^2$ graphene surface on SiC. It shows the presence of SiC steps
 101 which are several tens of μm wide. Two typical Raman spectra measured on the sample are illustrated
 102 on figure 1b, after subtraction of the Raman signal coming from the SiC. The G and 2D peaks, a
 103 characteristic feature of graphene, are clearly visible (with G peak at 1596 and 1592 cm^{-1}) [22]. The D
 104 peak intensity is either not detected or much smaller than our G peak, indicating that disorder or
 105 defects are absent or very present in very small amount [23]. The widths of 2D peak and the low value
 106 of the radio $I_{2D}/I_G < 1$ indicates that the graphene is mainly a bilayer.
 107



108 4.
 109 5. **Figure 1.** (a) $60 \times 60 \mu\text{m}^2$ AFM image of the graphene on SiC which we used for balun circuits (b) Two
 110 representative Raman spectra of our graphene, the SiC background Raman signal has been subtracted.

111 5.1. Circuit description

112 The GFET-Balun is realized using two active GFET transistors (T1 and T2) where the sources are
 113 connected together and two loads (transistors T_{AL1} and T_{AL2}) are tied to the drains of T1 and T2, and
 114 connected to the power supplies VDD and VSS, respectively (see figure 2b). In comparison to [15],
 115 lumped resistors are replaced by integrated active loads using transistors where the gate is connected
 116 to the source. The input signal is applied to the gates of T1 and T2 (both gates are connected together).
 117 The gate-source voltage of the graphene transistors is hence equal to $V_{GS0} + V_{ac}$, where V_{GS0} is the
 118 DC-offset voltage used for accurately setting the quiescent point. The balanced output signals are
 119 measured at the drains. The circuit has been simulated with the compact model described in [24,25]
 120 and also applying a mixed SPICE and electromagnetic simulation through ADS-Momentum. In the
 121 previous graphene simulated circuit [25] and considering the former available technology developed
 122 at University of Lille [15], circuit shows performances in the GHz range with a difference of phase
 123 lower than 10° up to 1.2GHz.
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Figure 2. Schematic circuit diagram of the balun and photography of the balun highlighting its layout. Chip size is 0.19mm².

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5.2. GFET description

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The transistor channel is composed mainly of a bilayer graphene. The gate length is about 240 nm. A top gate is used with an insulator thickness of about 15 nm made of Al₂O₃. The width of each device 24 μm. The DC ID-VGS and its associated transconductance characteristics of a GFET, as well as the AC- characteristics were measured on a transistor situated at close proximity of the balun for minimal dispersion. The influence of the pads has been removed through appropriated test-structures and de-embedding. Maximum transconductance is about 5mS. The gate-source capacitance CGS is about 26fF while the gate-drain capacitance CGD is about 8fF. The device is characterized by a cut-off frequency of 19GHz and a maximum oscillation frequency of 6GHz.

137

5.3. Balun circuit characterization

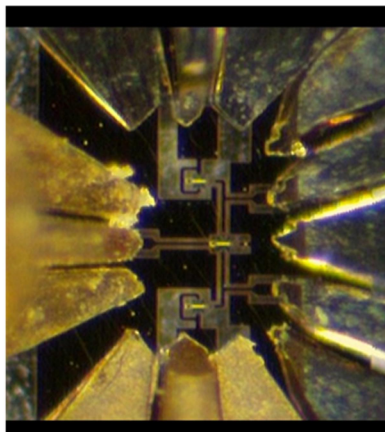
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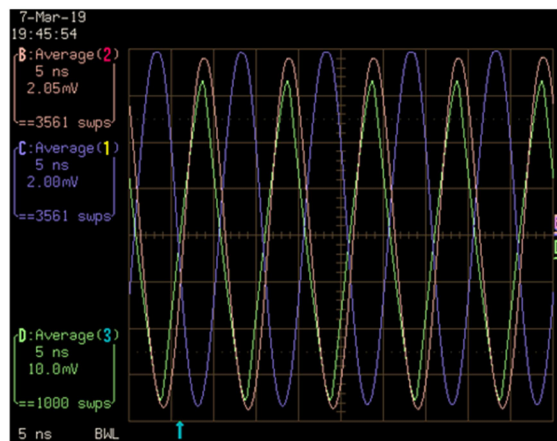
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First functionality tests have been performed thanks to time domain measurement using a RF source set at 100MHz and -10dBm. One single RF probes is used at the input while a differential probe is used at the output.

(a)



(b)



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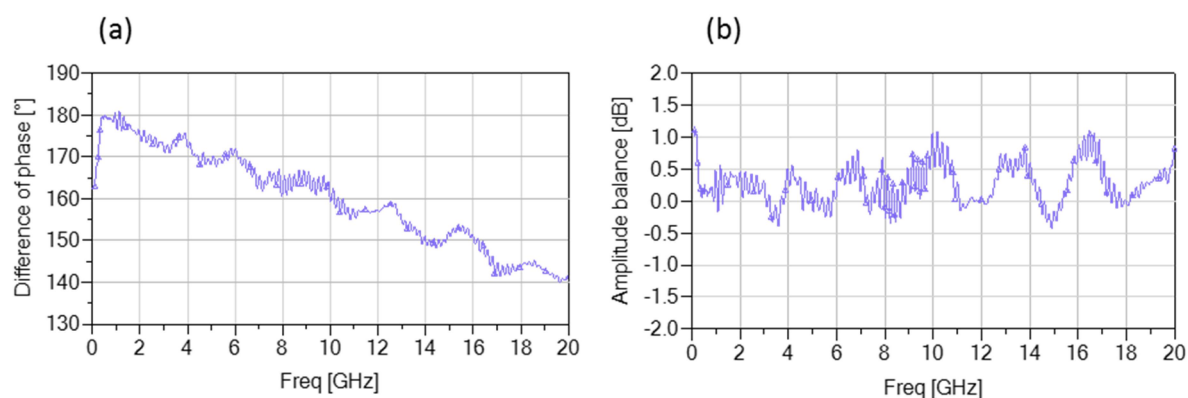
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Figure 3. (a) Photography of the balun under measurement condition. (b) Oscilloscope measurement when applying a sinusoidal input voltage with an amplitude of 32mV at the input (channel D) and sensing the two outputs (channel B and C).

145 Two other RF probes are used for convenience to apply the DC bias. +2V and -2V are respectively
 146 applied on VDD and VSS. Also, 2V is applied on the input thanks to a bias tee. A photography of the
 147 balun under measurement conditions is shown in figure 3a.

148 Scope measurements are presented in Fig. 3b highlighting the functionality of the circuit with
 149 180° phase shift between the two outputs. In that first measurement setup, the measurement is not
 150 calibrated and does not allow high frequency measurement. That's the reason why a 4 port PNAX
 151 vector network analyzer (VNA) is used in the following part to obtain calibrated data at the probe
 152 level. In order to perform the differential measurement with the VNA, the intermediate frequency is
 153 set to 100Hz and the input power is fixed to -10dBm.
 154



155

156 **Figure 4.** Three port S parameters measurement up to 20 GHz using a PNAX: (a) phase difference
 157 between the two outputs; (b) amplitude balance between the two outputs.

158 The setup is calibrated using a calibration kit dedicated to differential probes. Measurements
 159 reveals that the two outputs signal have a phase difference of 180° up to the GHz range (see Fig. 4a).
 160 This difference decreases to 170° at 6GHz. The output signals are attenuated of about 20dB with an
 161 amplitude imbalance lower than 0.5dB below 6GHz (see Fig. 4b). The bias current is 40 mA giving a
 162 power consumption of 160mW. The strong attenuation of 20 dB is directly correlated to the
 163 transistors' performances and especially to the high output conductance g_{DS} , a specific weakness of
 164 graphene devices. Also, the power consumption can be optimized by reducing gate width to obtain
 165 the optimal tradeoff between power consumption and output impedance of the balun.
 166

167 6. Discussion

168 6.1. Comparison with state of the art

169 Finally, the balun circuit is compared to the state of the art of active baluns made with different
 170 technologies such as silicon [26], SiGe [27], GaAs [28] and GaN [29]. These publications are chosen to
 171 have a similar technology gate length than the graphene technology used in this paper ranging from
 172 0.18 to $0.5\mu\text{m}$. The transit frequencies of these technologies are also in the same range spanning from
 173 about 20 and up to 40GHz. Moreover, the baluns are designed for broadband applications and below
 174 16GHz. The graphene balun presented in this work have comparable performance in terms of phase
 175 difference and amplitude balance compared to the industrial technology despite its low maturity.
 176 As mentioned early, the major drawback is due to the losses in the graphene balun which is
 177 intrinsically correlated to the transistor performances and not to the circuit topology itself.
 178
 179

180

Table 1. Broad-band active balun state of the art, FBW=frequency bandwidth

	Technology	Phase difference	Amplitude balance	Loss/Gain	IC Area mm ²
This work	Graphene 300nm fT=19 GHz	<10° FBW< 6GHz	<0.5dB	-20dB	0.16
[29]	GaN, 0.25µm (high power) typical fT=25 GHz	<10° FBW:2.4-6 GHz	<0.4dB	+7.4dB	
[26]	Si, 0.18µm	<3° FBW< 8GHz	2dB at 8 GHz	-	0.38
[28]	0.5µm GaAs fT=35 GHz fMAX=70 GHz [30]	<8° FBW:1-16 GHz-	1 dB FBW 1-16 GHz-	-1 to 2 dB	0.36
[27]	SiGe (0.8µm) fT=35 GHz	<0.9° FBW:0.6- 4.1	0.1dB FBW:0.6- 4.1	7 to 10 dB	1.44

181 7. Conclusion

182 A graphene-based broadband balun monolithically integrated circuit working up to 6GHz has
 183 based on SiC graphene bilayer technology has been demonstrated. The circuit contains four
 184 individual transistors. The graphene-based balun performances are compared to state of the art
 185 baluns on semiconducting technologies having similar RF-characteristics. This comparison
 186 accounts for frequency bandwidth, phase difference, amplitude balance and die area. Comparable
 187 performances are achieved except of gain. The circuit performances are intrinsically correlated to the
 188 transistor performances. For the graphene-based topology, the circuit works up to one third of the
 189 transistor's transit frequency which is suitable for the new 5G NR sub-6 standard.

190 The balun concept based on the ambipolar behavior of the GFET that has been demonstrated in
 191 this paper may be replicated on other promising materials such as TMDs materials, carbon nanotube
 192 FETs or other ambipolar FETs.

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196

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