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FPGA based fault-tolerant control on an interleaved DC/DC boost converter for fuel cell electric vehicle applications

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In recent years, the effects of high-frequency current ripple coming from DC/DC converters on Proton Exchange Membrane Fuel Cell (PEMFC) have gained a growing interest from the international scientific community. Currently, the durability is one of the major technical challenges to PEMFC commercialization. Basing on the existing literature, the high-frequency current ripple leads up to long-term degradations on PEMFC, particularly on its lifetime. Accordingly, in order to enhance the PEMFC lifetime, new DC/DC converter topologies have been developed, such as Interleaved DC/DC Boost Converter (IBC). Despite this topology can minimize drastically the current ripple, the loss of one leg in case of power switch fault leads up to the drastic increasing of the current ripple and consequently long-term degradations on the PEMFC. In order to cope with this issue, solutions have to be developed. Within the framework of this research work, an efficient Fault-Tolerant Control (FTC) implemented on an FPGA board has been developed to solve this issue. The latter consists in changing the PWM gate control signal according to the faulty leg given by a fault detection algorithm. The obtained experimental results between a PEMFC and an IBC to-pology allows demonstrating the ability of the FTC to reduce drastically the current ripple in case of power switch faults.

Introduction

Recently (i.e. 2011) [1], a survey on the industry regarding the reliability of power converters was carried out in order to

determine the needs of the industry and also reliability expectations. According to this survey, power switches ranked the most delicate components. Furthermore, this study has allowed emphasizing the causes of the main stresses of power switches, which are:

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Nomenclature

Acronyms

CCM	Continuous Conduction Mode
ECU	Electronic Control Unit
FC	Fuel Cell
FCEV	Fuel Cell Electric Vehicle
FIBC	Floating Interleaved Boost Converter
FPGA	Field Programmable Gate Array
FTC	Fault-Tolerant Control
IBC	Interleaved Boost Converter
OCF	Open Circuit Fault
PEMFC	Proton Exchange Membrane Fuel Cell
SCF	Short Circuit Fault
VHDL	VHSIC Hardware Description Language

- 1 Environment;
- 2 Transients (load, source, faults);
- 3 Heavy loads.

Due to the importance of power switches, many researchers have published many papers concerning fault-detection algorithm for power converters, including DC/DC converters [2–13]. The most common failures in power switch are Open Circuit Faults (OCFs), gating faults, and Short-Circuit Faults (SCFs) [14]. Furthermore, OCFs can be a consequence of SCFs if and only if the fuse melts before the short-circuit damages the system [15]. These faults may occur due to external or internal events such as incorrect gate voltage, driver failure, lifting of bonding wires due to thermal cycling, electrical over stress (i.e. voltage or current) [14]. In this study, only OCFs are considered.

Once the fault has been detected, DC/DC converter stop must be avoided. In order to ensure a continuity of service and/or reduce the undesirable effects of degraded operating modes, a fault-tolerant DC/DC converter topology or/and a Fault-Tolerant Control (FTC) must be used. Starting from the existing literature [16], only 36% of papers present a fault detection algorithm combined with an FTC. Different approaches have been introduced in the literature for fault-tolerant DC/DC converters. Some of them are based on dynamic redundancy with a control reconfiguration [2–9] representing 67% of the papers with FTC; whereas others use control reconfiguration without dynamic redundancy [10–12] (i.e. 25% of the papers) or modularity [13] (i.e. 8% of the papers). Generally, control reconfiguration without dynamic redundancy is preferred for automotive applications. Indeed, the use of dynamic redundancy goes back to increase the cost and the volume of the DC/DC converter which is not fit for automotive applications [17]. Additionally, 48% of the papers present a detection algorithm for OCFs; whereas 45% of the papers present a detection algorithm for OCFs and SCFs.

By comparison, fault-tolerance in Fuel Cells (FCs) has been studied through many papers available in the literature [18–29]. The major parts of these papers propose fault-tolerant FC system in order to ensure a continuity of service in case of failures. However, these papers do not present FTC to minimize the effects of degraded operating mode on the FC.

Within the framework of this research work, an Interleaved Boost Converter (IBC) is used in order to meet the Fuel Cell Electric Vehicle (FCEV) requirements in terms of compactness, efficiency, FC current ripple and reliability in case of power switch faults [17]. Despite the IBC continues to supply power to the load without any interruption in case of power switch faults, the loss of one leg leads up to the drastic increase of the FC current ripple. According to the existing literature [30–32], the high-frequency current ripple with a high peak-to-peak value could lead up to long-term degradations, particularly with the decrease of the active surface of platinum from catalysts. For this reason, it is crucial to apply an FTC in order to reduce drastically these degradations. Concerning the three-leg IBC topology, the FTC consists in changing the PWM gate control signal according to the faulty leg. Indeed, the FTC strategy depends strongly on the faulty leg. An unfit control reconfiguration could have undesirable effects on the system such as the FC current ripple increasing [17].

This paper is divided into 4 sections. After the introduction presenting a review on this topic, section Architecture of FCEV and IBC topology presents the architecture of the FCEV and the IBC topology. Then, in section Developed fault-tolerant control, the developed FTC is explained in details. Finally, the section Experimental test bench and results presents the experimental setup carried out for this work and the obtained experimental results. Besides, a discussion focused on a review of previous works regarding the minimization of current ripple and the advantage of the developed FTC on an FPGA board is provided.

Architecture of FCEV and IBC topology

Presentation of the architecture of FCEV

The powertrain of an FCEV needs a great deal of components as it is demonstrated in Fig. 1, among which the Proton Exchange Membrane Fuel cell (PEMFC), DC/DC and DC/AC converters, electrical motors and finally an auxiliary power unit (e.g. batteries or Supercapacitors). In this case under study, high-voltage batteries are used to assist the propulsion of the vehicle during transients and to absorb the kinetic energy during regenerative braking. Within the framework of this research work, only the PEMFC and DC/DC converters are considered.

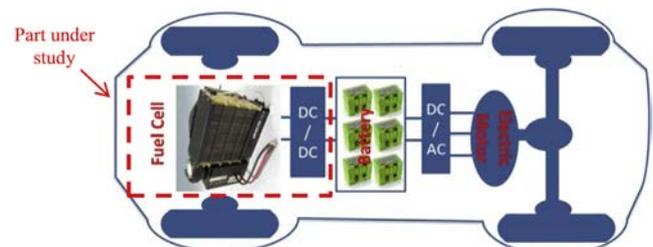


Fig. 1 – Example of architecture of the powertrain of the FCEV [33].

Presentation and advantages of the IBC topology

Starting from challenging issues in FCEV applications [17], it has been chosen to focus our present study on an IBC topology. The schematic representation of this topology combined with a PEMFC is depicted in Fig. 2. This topology presents several advantages compared with others topologies of DC/DC converters for FCEV applications [34], including compactness, high efficiency, reduced FC current ripple and adaptability for degraded operating mode in case of power switch faults. The choice of the number of legs (i.e. $N = 3$) is justified by a compromise between volume of inductors, efficiency, input current ripple, redundancy and cost [17].

Due to the architecture of the 3-leg IBC topology, if a power switch fault occurred on one leg, this could be compensated by the healthy legs. As a result, the IBC topology continues to supply power to the load without any interruption [3].

In order to satisfy the fault tolerance requirements, fuses (F1, F2, F3) have been added in series with each power switch, as illustrated in Fig. 2. The fuses allow isolating faulty leg in case of SCFs. Furthermore, the PEMFC has to be electrically protected (e.g. addition of a fuse series connected with the IBC) against possible SCF [17]. In order to make easier the study, the rest of FCEV powertrain is considered like a resistive load.

Developed fault-tolerant control

Fault-tolerant control principle

As it was mentioned in a previous work [17], the concept of interleaving of the IBC topology is guaranteed by the phase shifted control of the three switches (S1, S2, S3). In the case under study, each PWM gate control signal is shifted from each other with a time delay of $T_s/3$, where T_s is the switching period of the IBC topology. Under a degraded mode, the PWM gate control signals of the healthy power switch continue to be shifted from each other with a time delay of $T_s/3$. As a result, the FC current ripple increases compared to a healthy mode due to the OCF as depicted in Fig. 3.

As it was highlighted in Ref. [17], once the OCF occurs, the healthy legs allow compensating the faulty leg in order to avoid any power interruption to the load. However, the loss of one phase leads up to the increasing of the other inductor phase currents (i.e. the healthy leg current increase of 50% compared to a healthy mode), creating consequently

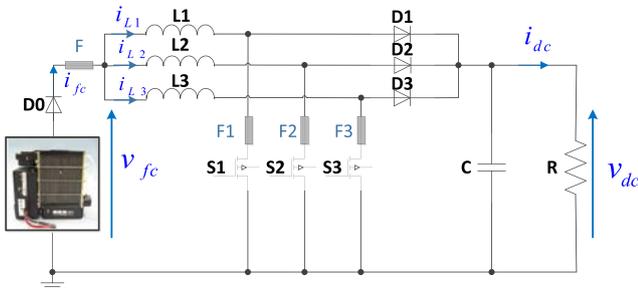


Fig. 2 – Pemfc and 3-leg IBC.

additional electrical stresses, particularly on the power switch and inductive component. Accordingly, in order to guarantee the reliability of the IBC topology in case of power switch fault, the power switches should be oversized. Indeed, the electrical over stress (i.e. current) could lead up to power switch failures [14,17]. Regarding the inductors, their sizing must be optimized in order to minimize their volume and weight, particularly for automotive applications.

Over the last decade, many researchers have investigated the effect of low and high-frequency current ripple coming from power converters on PEMFCs. Although the impact on the PEMFC lifetime is so far not well understood, some observations have been already reported in the literature. Generally, DC/DC converters generate high-frequency current ripple (i.e. >10 kHz); whereas DC/AC converters produce low-frequency current ripple (i.e. 100–120 Hz) depending strongly on the load and the type of DC/AC converter used [17]. Up to the present, the effects of high-frequency current ripple have been analyzed using an electronic load combined with a signal generator, allowing simulating FC current ripple coming from DC/DC converters. However, the use of a signal generator limits the scope of investigation up to a frequency current ripple equal to 10 kHz. The use of a DC/DC converter could broaden the scope of investigation for FC current ripple frequencies higher than 10 kHz [17,35]; where the new topologies of DC/DC converter (e.g. topologies including soft-switching and/or Silicon Carbide (SiC) semiconductors) for PEMFC applications operate. This will allow having a better understanding of the real impact of high-frequency current ripples on PEMFC lifetime; which is one of the major challenges to FC commercialization [36]. According to a brief review of this topic of emerging interest [17], high-frequency current ripple can lead up to long-term degradations, particularly with the decrease of the active surface of platinum from catalysts.

It is important to apply an FTC once the fault has been detected in order to reduce drastically the degradations introduced in the literature [30–32]. Concerning the 3-leg IBC topology, the FTC consists in changing the PWM gate control signal according to the faulty leg given by a fault detection algorithm [17]. Indeed, the FTC depends strongly on the faulty leg. An unfit control reconfiguration could have undesirable

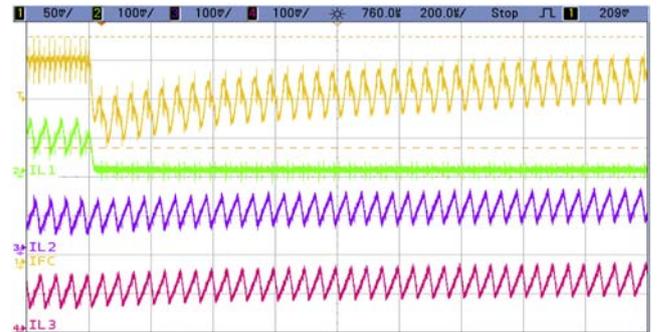


Fig. 3 – FC current ripple increasing after an OCF, obtained for $D = 0.72$: channel 1: FC current [5A/div], channel 2: leg 1 current (faulty) [10A/div], channel 3: leg 2 current [10A/div], channel 4: leg 3 current [10A/div].

effects on the system such as the FC current ripple increasing. The flow diagram of the FTC has been introduced in Ref. [17].

Within the framework of this research work, each PWM gate control signal is shifted from each other by means of an FPGA board. A VHDL programming code has been implemented on the FPGA board through the Quartus II software. The code uses the first PWM gate control signal (Matlab/Simulink) as reference, then it creates the missing PWM gate controls signals shifting them correctly compared with the reference. For a healthy mode, the time delay is equal to $T_s/3$. On the other hand, for a degraded mode, the time delay between two PWM is given by the faulty leg. An accurate knowledge of the faulty leg allows determining the fit time delay. The Table 1 gives the FTC to apply according to the faulty leg. The advantage of this FTC is that it can be fitted whatever the number of legs of interleaved DC/DC converter topologies.

Experimental test bench and results

Experimental test bench description

In order to carry out a thorough investigation on the efficiency of the FTC proposed, experimental tests have been carried out between a PEMFC and a 3-leg IBC. The experimental test bench is depicted in Fig. 4. The PEMFC is supplied using hydrogen from tank under pressure, and with clean and dry air from a compressor. In order to supply the Electronic Control Unit (ECU) of the PEMFC with the necessary power to start the FC system, it has to be connected with an external power supply. The IBC topology has a TAMURA L03S050D15 current sensor per leg and an MTX 1032-B voltage sensor at the output for feedback control. The developed Matlab-Simulink control system has been transferred through the real time board dSPACE DS 1104. Additionally, the control of the IBC has been designed so that the PEMFC works in the ohmic region in order to avoid the high and low voltage region for prolonging the PEMFC lifetime [17]. The three PWM gate control signals are generated by a PWM signal generator block provided by dSPACE library in Matlab-Simulink environment. However, these PWM signals are not shifted from each other. In order to guarantee the interleaving concept and to minimize the FC current ripple, the three PWM gate control signals of the three switches (i.e. S1, S2, S3) must be shifted from each other. In the case under study, each PWM gate control signal is shifted from each other with a time delay of $T_s/3$, where T_s is the switching period of the IBC topology. These three PWM gate control signals are transferred to an Altera Cyclone FPGA board in

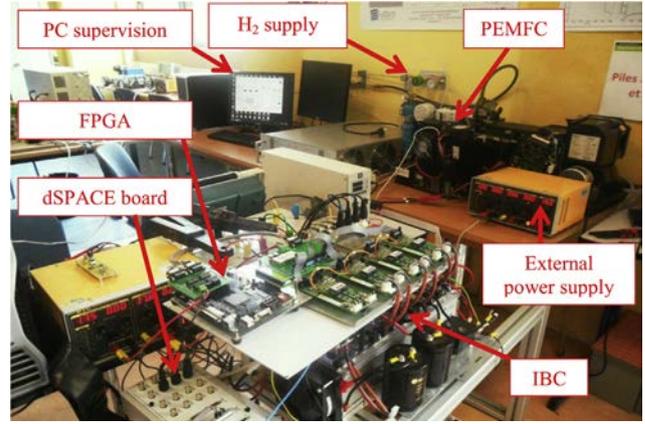


Fig. 4 – Experimental setup carried out for this study.

order to shift them correctly from each other [17]. The system specifications are summarized in Table 2.

In order to simulate an OCF, a failure is introduced in the PWM gate control signals of the power switches using the push-button available on the FPGA board. The FPGA device will see a logic signal ‘0’ when the push-button is pressed (Fault); whereas the device will see a logic signal ‘1’ when the push-button is not pressed (no fault). The flow diagram is given in Fig. 5. On the other hand, the push-button can be used to simulate SCFs. In this case, the PWM gate control signal must be forced to “1” instead of “0” for an OCF.

Experimental results obtained

Starting from the FTC principle, experimental tests have been performed in the laboratory. The purpose is to show and analyze the effects on FC current ripple applying the proposed FTC. Once the OCF has been detected on the faulty phase, the FTC is applied to the PWM gate control signal through the VHDL programming code implemented on the FPGA board. The results are depicted in Figs. 6, 7.

According to the faulty leg and the Table 1, a fit FTC is applied to the control of the IBC topology. This allows minimizing drastically the fuel cell current ripple and consequently the long-term degradations reported in the literature (Fig. 6). Besides, the application of the FTC does not have impact on the regulation of the DC bus voltage (Fig. 7). It is important to highlight that it is crucial that for specific architectures of FCEV [33], the DC/DC converter provides directly the power to inverters through the DC bus voltage. For this reason, it is essential to provide the constant inverter DC link

Table 1 – FTC to apply according to the faulty leg.

Faulty leg	FTC to apply
Leg 1	Reconfigure the leg-shift of leg 3 ($2T_s/3 \rightarrow 5T_s/6$)
Leg 2	Reconfigure the leg-shift of leg 3 ($2T_s/3 \rightarrow T_s/2$)
Leg 3	Reconfigure the leg-shift of leg 2 ($T_s/3 \rightarrow T_s/2$)

Table 2 – System specifications.

Parameters	Values
PEMFC rated power, P_{fc}	1 kW
PEMFC rated current, i_{fc}	42A
PEMFC current ripple, Δi_{fc}	2A
PEMFC voltage range, v_{fc}	25 –32V
Inductor value, L	150 μ H
DC bus voltage, V_{dc}	100 V
Switching frequency, f_s	20 kHz
Duty cycle range, D	0.68–0.74

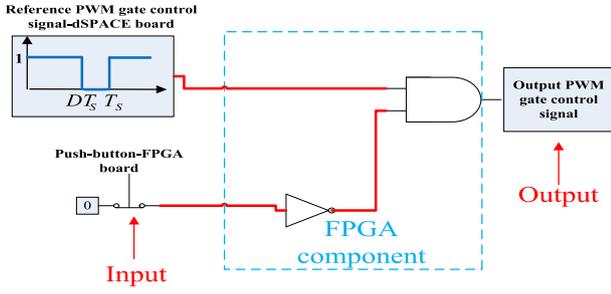


Fig. 5 – Generation of an OCF using the push-button from the FPGA board.

power. Fig. 8 depicts the evolution of FC current ripple expressed as percentage of FC rated current according to the duty cycle. The evolution is focused on three different operating modes such as healthy mode, degraded mode without and with FTC.

It has been suggested in the literature that the FC current ripple should be restricted to less than 10% of the rated FC stack current [37, 38]. In our study, the FC current ripple is set to be 5% of the rated FC current, which means ($\Delta i_{fc} = 2A$). This restriction is achieved by sizing the three inductors of the IBC topology. As it can be observed in Fig. 8, the FC current ripple value remains lower than the limit of Δi_{fc} for a healthy mode. However, for a degraded operating mode without FTC, the FC current ripple remains higher than the limit of Δi_{fc} for all values of duty cycle range. On the other hand, applying the FTC, FC current ripple value remains lower than the limit of Δi_{fc} .

If another leg was faulty, a fit FTC would be always applied according to the faulty leg and the Table 1. In short, the FTC proposed is efficient and powerful for reducing drastically the fuel cell current ripple whatever the faulty leg.

Discussion

In order to reduce the high-frequency current ripple, different solutions have been introduced in the literature. The major part of solutions consists in using specific topologies of DC/DC converters or current ripple reduction techniques. Some authors employ conventional current-fed push-pull DC/DC

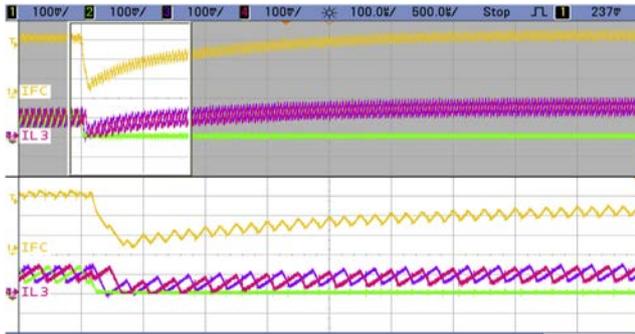


Fig. 6 – Application of the FTC and effect of the FC current ripple: channel 1: FC current [10A/div], channel 2: leg 1 current (faulty) [10A/div], channel 3: leg 2 current [10A/div], channel 4: leg 3 current [10A/div].

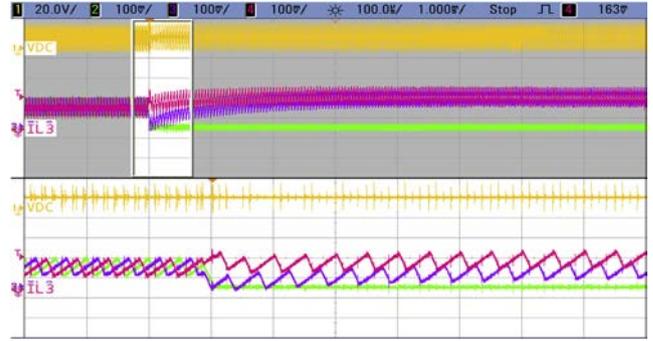


Fig. 7 – Impact on the DC bus voltage once the FTC has been applied: channel 1: DC bus voltage [200 V/div], channel 2: leg 1 current (faulty) [10A/div], channel 3: leg 2 current [10A/div], channel 4: leg 3 current [10A/div].

converters, which are limited for high-frequency applications. The main drawback of this topology is the number of components, which leads up to energy efficiency reduction. Besides, this topology is not fault-tolerant in case of power switch fault. It is important to point out that this topology has the input current ripple switching extremely low at duty cycles around 0.5 [35, 39]. On the other hand, other authors use isolated DC/DC converter topologies proposing zero-current switch or zero-voltage switch techniques with input filter in order to increase the switching frequency. Hence, this allows reducing the current ripple but the topology contains an isolating transformer [40]. Moreover, other topologies such as half-bridge DC/DC converters can also be considered. Indeed, they are deduced from an IBC topology by introducing a transformer and a diode bridge at its output. However, in order to gain this topology, the duty cycle must be greater than 0.5 and the leakage inductance of the transformer is the main drawback of this topology, which can generate voltage spikes [41, 42]. Other authors employ coupled inductance in the power converter combined with a hybrid filter. However, a thorough design of the coupled inductance is crucial [43]. IBC and Floating Interleaved DC/DC Boost Converter (FIBC) topologies are also considered in the literature [17, 34, 44], to minimize the high-frequency current ripple. In Ref. [45], the authors propose a zero input current ripple boost converter by using a mirror ripple circuit. In order to avoid circulating current, a capacitor bank is inserted between the mirror ripple and the output of the boost converter. This technique presents the drawback to be only efficient in steady state and under

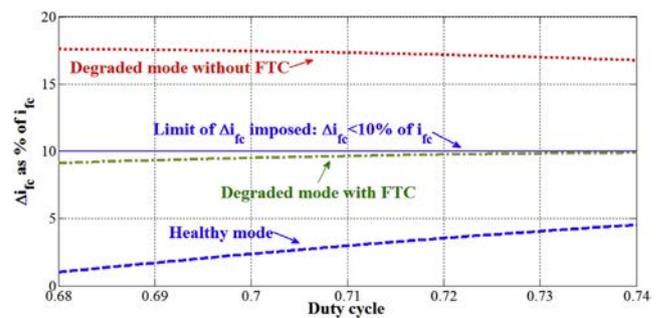


Fig. 8 – Δi_{fc} as percentage of i_{fc} according to the duty cycle.

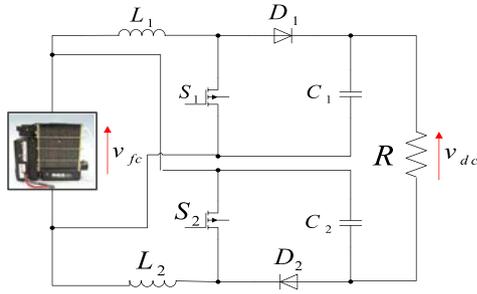


Fig. 9 – Architecture of a 2-leg FIBC.

Continuous Conduction Mode (CCM). In Ref. [46], the authors propose an active filtering method to actively damp the current ripples generated by DC/DC converters. However, such a solution increases the system components and complexity which is not fit for automotive applications. A second order low pass filter is proposed in Ref. [47] in order to minimize the current ripple generated by a FIBC. However, the passive components have been sized to filter the high-frequency current ripple for a healthy mode (i.e. no power switch faults). Consequently, the proposed second order low pass filter would not be efficient if one of the legs was faulty due to the drastic increasing of current ripple [48]. Finally, in Ref. [49], the authors propose a two-leg IBC with current ripple cancellation whatever the desired duty cycle value without increasing the number of components. This architecture presents a main drawback in terms of fault-tolerance despite the presence of static redundancy. Indeed, if one of the legs was faulty, this architecture would lose its advantage of the current ripple cancellation. The same architecture could be developed into a four-leg IBC in order to cancel current ripple in case of power switch faults, but this would go back to increase the complexity and cost of the converter.

The main contribution of this paper compared to other research papers presented above, is the development for interleaved converter topologies of an FTC without adding additional components to reduce drastically the current ripple in case of operating degraded mode (i.e. loss of one leg). This FTC is implemented on a FPGA board, which over the last years has demonstrated high performances for many power electronic applications [9, 14]. An other crucial research work is remaining for interleaved DC/DC converter topologies, namely the reliability of the latter in case of power switch faults.

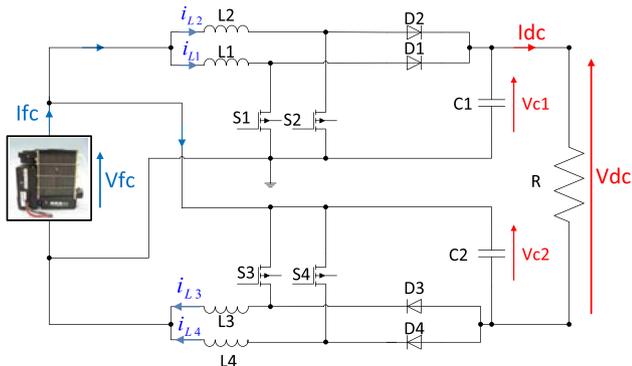


Fig. 10 – Architecture of a 4-leg FIBC.

Indeed, as it has been demonstrated in this paper, the current of the healthy legs increase of 50% compared to a healthy mode in case of the loss of one leg, creating consequently additional electrical and thermal stresses. For specific interleaved converter topologies (e.g. FIBC), the electrical stresses are higher than an IBC topology. The interleaving concept of this topology is guaranteed by the parallel connection of the non-floating and floating version of the boost converter (Fig. 9) [48]. The number of legs of this topology must be necessarily pair in order to keep a balance between the non-floating part (i.e. upper part) and the floating part (i.e. lower part). Generally, a four-leg FIBC (Fig. 10) is preferred for fault-tolerance purpose since a power switch fault in a 2-leg FIBC will lead up to an unsteadiness between the non-floating and floating part. On the other hand, the loss of one leg located either in a non-floating or floating part for a four-leg FIBC, could be compensated by the other leg located in the faulty part. Despite the FIBC keeps the balance between the two parts, this leads up to the overload of a leg, creating consequently more additional electrical and thermal stresses (i.e. the current of the healthy leg increase of 100% compared to a healthy mode) on power switches and inductive components. In summary, critical cases of operating degraded mode must be avoided by developing efficient FTC in order to guarantee the reliability of the converter in case of power switch faults.

Conclusion

The main purpose of this paper was to present a FPGA based fault-tolerant control of an interleaved DC/DC boost converter for fuel cell electric vehicles. Basing on a thorough bibliographical study, it was shown that power switches ranked the most delicate components in DC/DC converters. In this paper, open-circuit faults have been investigated. The loss of one leg in case of open-circuit fault leads up to the drastic increase of the fuel cell current ripple, responsible to long-term degradations on the fuel cell. In order to minimize the undesirable effects on the fuel cell, a fault-tolerant control without using additional components is applied to the interleaved DC/DC converter topology when the fault has been detected on the faulty leg. The fault-tolerant control consists in modifying the PWM gate control signals according to the faulty leg. The results obtained by experimental tests have demonstrated that the FC current ripple decreases drastically compared with a degraded operating mode without applying a fault-tolerant control. The current ripple reduction allows improving the fuel cell performance while reducing hydrogen consumption and optimizing its lifetime. In order to guarantee the reliability of the interleaved DC/DC boost converter in case of power switch faults, a fault-tolerant control consisting in acting on the control of the latter will be implemented on a FPGA board.

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