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Cooperative Operation of Parallel Connected Boost Converters for Low Voltage-High Power Applications: An Experimental Approach

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Abstract

Modern power conversion devices have realized several significant attributes such as high efficiency and reliability for high power (HP) applications. Traditionally, boost converters (BC) are required to operate as an intermediate interface to drive high power loads through available low voltage (LV) sources such as a fuel cell (FC), photovoltaic or battery based energy system. This paper addresses the complementary operation of parallel connected boost converters (PCBC) for high power applications considering wide spectrum of low voltage source conditions. The mutual sharing of load current between parallel connected converters is guaranteed by the appropriate placement of LC based passive equalization filter (LCEF) therefore offloading stress from individual converter and increasing efficiency and reliability drastically. To validate the performance of proposed topology in real-time scenarios, an experimental setup consisting of programmable source, electronic load, boost converters and filter circuit has been synthesized and studied in various operating conditions such as FC energy system based HP and LV application. The experimental results clarifies and validates the necessity of parallel connected converters based power splitting strategy and LC equalization filter topology for high power loads especially with low voltage source conditions.

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Keywords: High power application; Low voltage source; Fuel cell; Boost converter; Equalization filter

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1. Introduction

The influx of high power applications is gradually rising in energy sector especially at domestic level. Some of the prime examples of such applications are the backup power supply, traction devices used in electric vehicles and de-centralized heating-cooling systems [1-4]. Mostly, low voltage battery based sources and sustainable generation systems with high power provision capabilities such as FC and photovoltaics are the driving essence to power these applications [5-9]. Modern power electronics devices such as boost converters are extensively utilized for efficient interfacing of HP loads with LV power sources [6,10-12].

Nomenclature			
APP	Active power conversion	D	Duty cycle of boost converter
BC	Boost converters	$G(t)$	External control signal to change D
CAP	Filter capacitor	I_c	Capacitor current (A)
CF	Conversion factor	I_L	Inductor current (A)
DC	Duty cycle	I_o	Load/output side current (A)
FC	Fuel cell	I_{in}	Input side current (A)
FWD	Freewheeling diode	P_L	Power consumed by load (W)
HP	High power	P_S	Power provided by source (W)
HV	High voltage	P_R	Power losses (W)
LV	Low voltage	R_o	Load equivalent resistance (Ω)
LC	Inductor capacitor	T_S	Periodic sample/switching time
LCEF	Inductor capacitor based equalization filter	V_L	Inductor voltage (V)
OCF	Over current protection	$V_o=V_{Lo}$	Load/output side voltage (V)
PCBC	Parallel connected boost converters	$V_{in}=V_s$	Input side/source voltage (V)
PWM	Pulse width modulation	V_D	Voltage drop (V)
RBD	Reverse blocking diode	η	Conversion efficiency
SL	Self-inductor		
UVP	Under voltage protection		

Efficiency and reliability are the two most important concerns during active power processing (APP) especially in aforementioned LV-HP applications [13]. Both of these concerns are partially correlated to power losses in various components of power converters such as in switching devices and passive filters [14]. Associated operation of PCBC can be a preferred choice to reduce the large power processing stress on any individual converter, thus reducing power losses in filter components and drastically improving working efficiency [15,16]. On other hand, mutual sharing of power by PCBC can also mitigate thermal throttling of individual converter.

However, guaranteed and secure sharing of load power in interconnected parallel operation of BC is itself a difficult task. PCBC are subjected to unequal power sharing and various protection problems [15]. Therefore, this matter has been addressed rigorously in literature. Voltage droop method is one of the most common and simplest method for stabilized operation of PCBC [17,18]. However, efficient mutual sharing of power in this method is dependent on output voltage regulation that is rather inadequate approach. Another current-sharing approach is the dedicated master-slave control scheme, where, all slave converters follow the reference current/voltage of the master converter. In [19,20], current sharing is addressed based on direct manipulation of duty cycle without dedicated voltage regulation which provides weak and questionable current sharing. However, in [21,22] dedicated regulation controller is employed to keep the voltages regulated and constant for stable sharing, which is rather complex and costly solution. All discussed topologies are somehow dependent on constricted and equal regulation of output voltages/currents of PCBC, which directly links to tight matching of duty cycles of interconnected converters. Any minor mismatch can negatively effects the sharing capacities and therefore triggers inefficient operation, waste of resources and stress on either converter leading to thermal throttling and poor performance. Therefore, this paper addresses mutual sharing of load currents between PCBC using on circuit closed loop regulation coupled with minor manual tuning of DC to individually regulate the output voltage of each converter in close vicinity. Furthermore, to support power sharing, controlling the power flow and enhancing the protection of converters during various operating conditions LCEF with RBD is proposed and properly placed after power conversation phase.

Fig. 1 presents a typical example of FC based LV-HP traction application. This example is the manifestation of FC/Battery based electric vehicle. Efficient power conversion has witnessed a lot of applications particularly in this

research area [12,23]. Major attributes concerning this typical application are highlighted in Table 1. Driving HP load through single boost converter in this particular example will stress the converter thus increasing power losses and negatively effecting the system efficiency. Thus, to address this problem, in this paper, an interface of PCBC is suggested to share currents in HP application coupled to LV source. A smart on circuit close loop regulator coupled with minor manual tuning strategy is utilized to tightly regulate the output voltages. The appropriate placement of LCEF is proposed to support the power sharing and furthermore, RBD are incorporated in filter topology to enhance the protection of converters. The current sharing capabilities and superior performance of proposed topology is appraised by an experimental setup consisting of programmable source, an electronic load, three converters connected in parallel and equalization filter circuit. Various real-time LV source and variable current, HP loading conditions are artificially simulated by programmable components. Results obtained with experimental setup validates the adequacy of proposed topology in ensuring equivalent sharing of currents by PCBC with acceptable efficiency and protection in various low voltage and varying high power loading conditions.

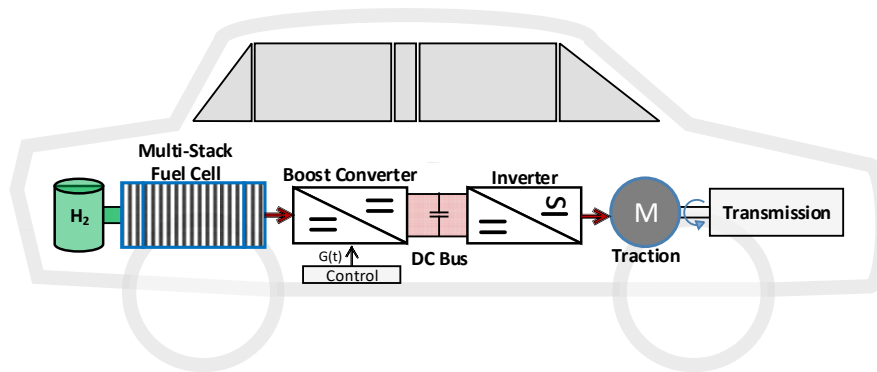


Fig. 1. Multi-stack FC energy system based LV-HP application.

Table 1. Major attributes concerning FC setup.

FC based energy system	
LV applications=>0.7V-0.8V per cell experimentally=>Stacking in series (Multi-stack) to provide higher voltages.	
Variable high currents=>High power=>Capability to drive high power load.	
Problems	Solutions
LV/High currents=> Bigger size is required for conducting elements especially the inductance in boost converter. Size↑ weight↑ price↑ Efficiency↓	Splitting currents/power in parallel connected boost converters.

The rest of manuscript is organized as follows: Problem formulation is presented in Section 2. Experimental setup, components description and procedure are accessible in Section 3. Experimental results leading to critical discussions are presented in Section 4. Finally, conclusions with important remarks are drawn in Section 5.

2. Problem formulation

Stressing single converter under LV-HP application can deteriorate the efficiency and reliability of operation due to power losses, therefore, LCEF based strategy to split power between PCBC is proposed to cater with this problem.

2.1. Operation of individual boost converter

Applications of boost converters to interface LV sources to variable HP loads are rapidly rising. Boost converter's generic internal circuitry along with PWM control signal is displayed in Fig. 2(a) and Fig. 2(b) respectively. The

converter's operation during whole switching horizon (T_s) is categorized in two parts as DTs and D'Ts, where $D+D'=1$ and D corresponds to duty cycle (DC). Fig. 2(c) and Fig. 2(d) serves the purpose of unique representation of this later statement.

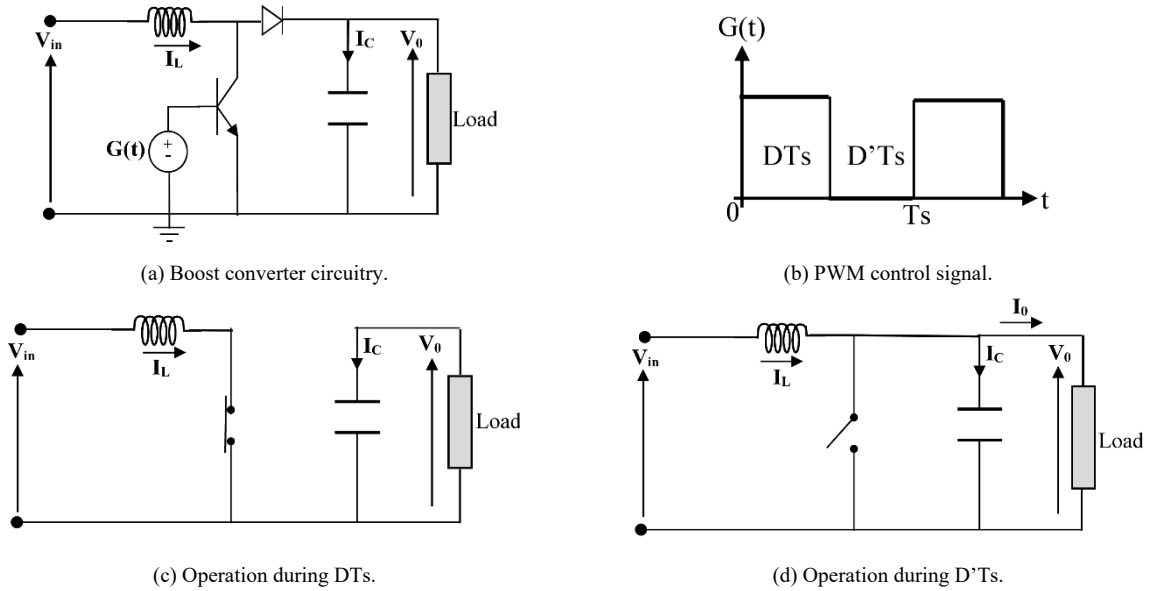


Fig. 2. Operation of individual boost converter.

The mathematical operation of boost converter during whole categorized switching period and APP is governed by Eq. (1-3). Here, Eq. (1) and Eq. (2) jointly explains the volt-sec and charge-sec balance for DTs and D'Ts duration respectively. Volt-sec and charge-sec balance are graphically depicted in Fig. 3(a) and Fig. 3(b).

$$DTs \Rightarrow \begin{cases} V_L = V_{in} \\ I_C = -\frac{V_0}{R_0} \end{cases} \quad (1)$$

$$D'Ts \Rightarrow \begin{cases} V_L = -(V_{in} - V_0) \\ I_L = I_0 + I_C \end{cases} \text{ where, } I_0 = \frac{V_0}{R_0} \quad (2)$$

$$APP \Rightarrow \begin{cases} \int_0^{T_s} V_L(t) \cdot dt \cong 0 \Rightarrow V_0 = \frac{1}{D'} V_{in} \\ \int_0^{T_s} I_C(t) \cdot dt \cong 0 \Rightarrow I_{in} = I_L = \frac{1}{D'} I_0 \end{cases} \quad (3)$$

A crucial point that can be concluded from Eq. (3) is the dependency of V_0 and I_{in} on conversion factor CF ($1/D'$) and DC. To keep the V_0 tightly regulated with steady decrease in V_{in} , DC has to increase steadily resulting in consequent increase in I_{in} , therefore, causing unwanted increment in power losses and decreasing the efficiency of conversion. This process is portrayed in Fig. 3(c), where, increment in DC triggers increment in V_0 , causing increment in power losses in filter winding, therefore, decreasing the efficiency. So, for HP application under the circumstances of LV source conditions such as FC setup, PCBC are preferred instead of one converter to cater against excessive power loss conditions. The boost converter considered here has on circuit regulation system to keep the V_0 regulated under variable source voltages. The converter can also be manually tuned with the help of three external control parameters as shown in Fig. 3(d). UVP: under voltage protection to strict the operation of converter below threshold voltages. OCP: over current protection or saturation to strict the operation if input current exceeds certain threshold and DC: duty cycle for manual tuning and setting the output voltages as desired.

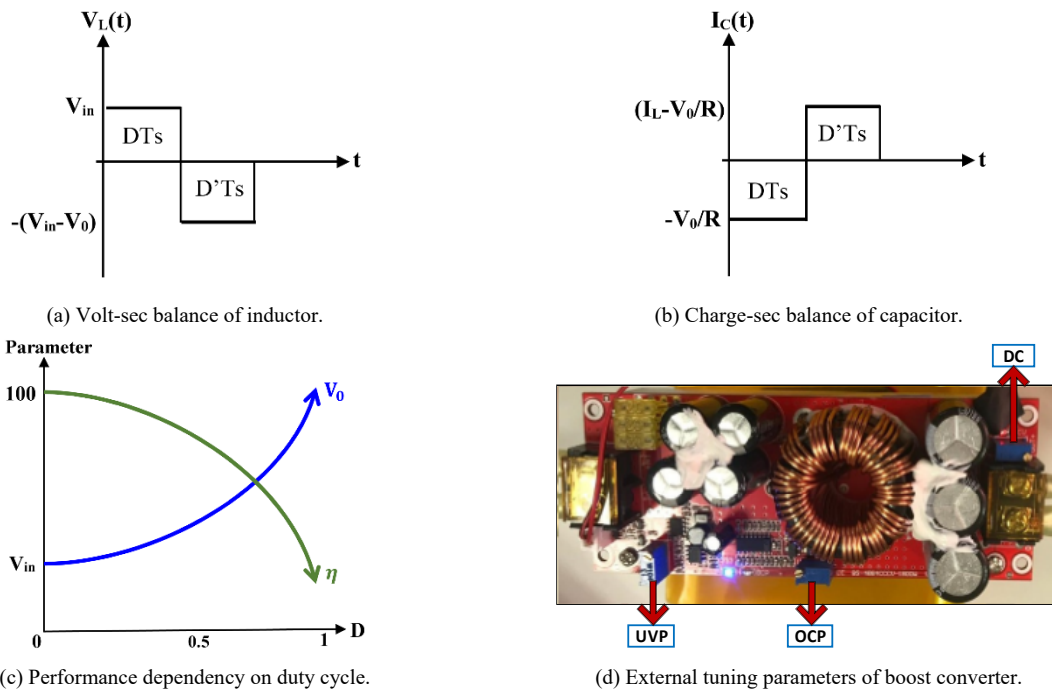
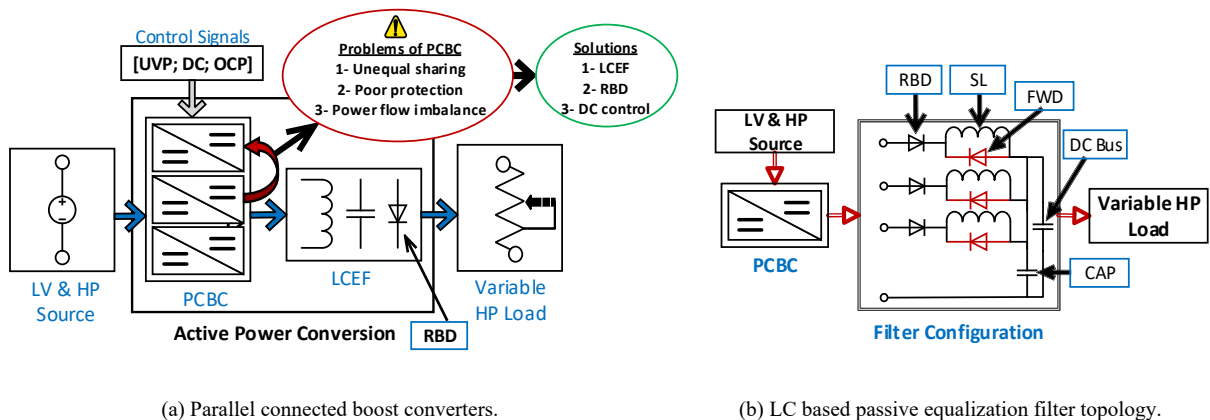


Fig. 3. Boost converter topology.

2.2. Operation of parallel connected boost converters

PCBC are preferred for HP application to share current and therefore offload stress from one converter, decrease the power losses and increase efficiency. On other hand, the splitting of current and controlling the sharing procedure is difficult task. Moreover, the operation of PCBC is also prone to unbalance power flow and deterioration of protection as in case of any DC mismatch unwanted power can flow from one converter to other converter as portrayed in Fig. 4(a). In this paper, on circuit regulation and minor manual tuning procedure are utilized in conjunction to tune the sharing capacities of three parallel connected converters. Furthermore, equalization filter is proposed with appropriate placement of passive elements and RBD to enhance the sharing capacities and protection of power converters under LV and HP source conditions.



(a) Parallel connected boost converters.

(b) LC based passive equalization filter topology.

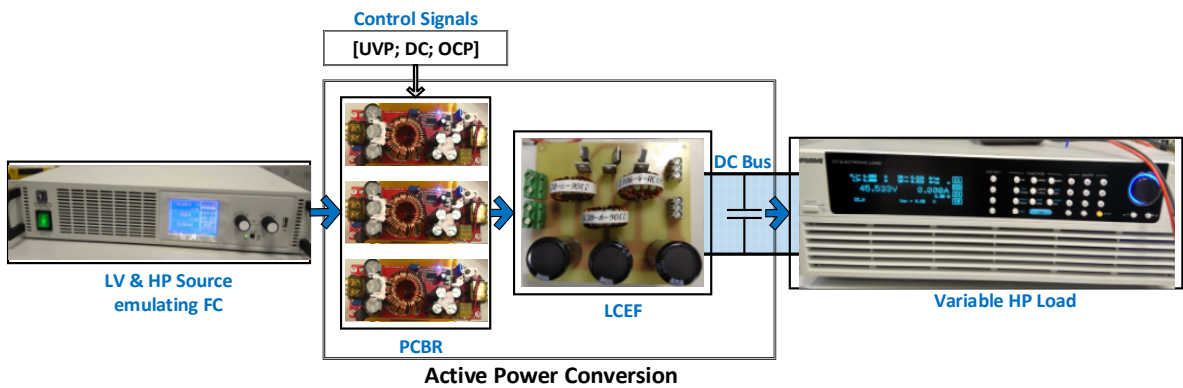
Fig. 4. Schematic diagram of PCBC and LCEF topology.

2.3. Passive equalization filter

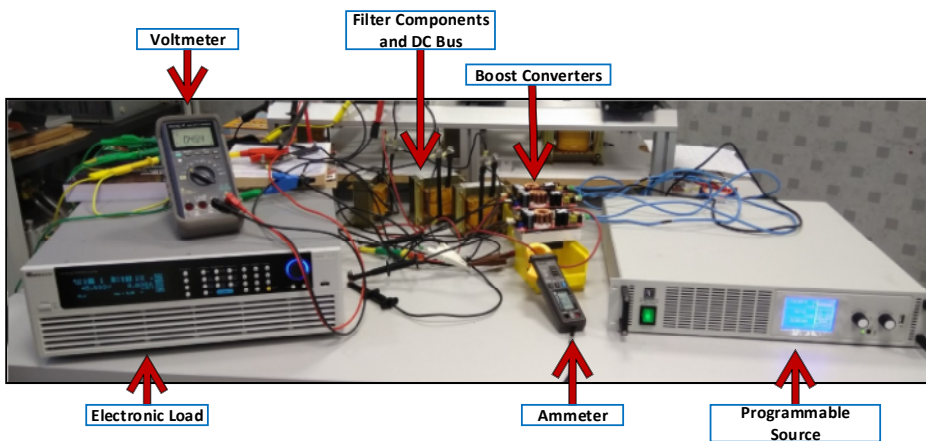
An equalization filter based on passive LC components is proposed and optimally placed after converters to assist the sharing and splitting of power between converters. The topology is displayed in Fig. 4(b) and consists of self-inductor (SL), filter capacitor (CAP), a DC bus and freewheeling diodes (FWD). RBD are also incorporated in equalization filter to enhance the protection of converters by diligently blocking the faulty current to flow from one converter to other converter in case of any DC mismatch or any other unwanted scenario.

3. Experimental setup and Procedure

Experimental setup consists of programmable source, electronic load, boost converters and filter circuit. Various real-time LV-HP loading scenarios are synthetically experimented in close resemblance to FC based setup using programmable components. Sequence of components is graphically expressed in Fig. 5 (a) while their description is tabulated in Table 2. The real-time experimentation results provides the authenticity of proposed parallel converters configuration and filter topology to keep the operation reliable and efficient under various conditions.



(a) Graphical sequence of components.



(b) Complete experimental setup.

Fig. 5. Experimental setup and relevant components.

Table 2. Description of components for experimental setup.

Stage	Components	Rating/Model
LV and HP Source	Programmable power supply	EA-PSI 9080 (80V-120A)
Power Processing	Boost converters	1800W, 40A
	Power diodes (FWD and RBD)	RHRP 3060D
	Self-inductors	2700uH
Filter circuit	Filter capacitors and DC bus	4700uF
	Electronic load	Chroma 63203A

Fig. 5(b) portrays the whole setup under procedural experimentation. The sequential procedural steps in setting up the experimental setup, completion of experiment, recording and analyzing the results are as follows:

Step-1: Boost converters are tuned individually using control signals to produce regulated 45V at output and the protection triggers above 6A saturation and below 8V source voltage.

Step-2: Boost converters are connected together in parallel and filter consisting of LC passive elements and RBD is placed after converters. Various variable current conditions are practically simulated using electronic load and mutual sharing of power by converters is prudently checked and recorded. During any mismatch, protection is provided using RBD inside filter topology. This mismatch is carefully remedied by minor tuning of individual duty cycle of converter under stress.

Step-3: Afterwards, various LV situations are emulated to drive HP load effectively mimicking the behavior of FC setup by manipulating the programmable source. Under these scenarios, load sharing capacity of converters is confirmed and recorded.

Step-4: The recorded readings are tabulated and analyzed to provide the feasibility of proposed topology to offload stress from one converter therefore, increasing the working efficiency under LV-HP conditions.

Note: It has been observed that the performance of converters in parallel is very sensitive to external adjustment of duty cycle of either converter and can be bottlenecked by wrong placement of filter. Furthermore, the presence of RBD enhances the protection required for reliable operation of PCBC.

4. Experimental results and Discussions

The composition of experimental tests is described in Table 3. The first set of tests virtually simulates LV conditions of variable voltage source while keeping load power constant. In essence, when source voltage decreases, consequently, source current increases to accommodate HP load. The second set of tests try to simulate variable loading conditions with constant voltage source. These set of tests are carefully constructed to emulate the behavior of real-time systems e.g. fuel cell based LV and HP sources coupled to high power applications. The results and discussion corresponding of each set of tests is carried out in following sections.

Table 3. Composition of experiments/tests.

	LV programmable source		HP electronic load
	State	Variable	Constant
Test-1 conditions	Variation/Value	16V→8V	6A
	State	Constant	Variable
Test-2 conditions	Variation/Value	16V	2A→12A

4.1. Test-1: Variable low voltage source conditions (at constant load current)

Test-1 constitutes a variable voltage source condition, gradually decreasing from 16V to 8V and fix electronic load of 6A and 45V (constant 270W), correspondingly. The readings recorded during Test-1 are compiled in Table A1. As the source voltages gradually decreases, to accommodate the constant load power, source currents in correspondence increases as shown in Fig. 6(a) (which relates to rise in cumulative DC and CF as shown in Table A1). During the whole procedure, mutual sharing of current is guaranteed by the inclusion of equalization filter and performance of on circuit regulation effectively. Due to gradual rise in source currents, the voltage drop and hence

power losses in filter winding also increases manifesting decrement in overall system efficiency, displayed in Fig. 6(b). It is very important to mention that processing of large power through one converter only is lesser efficient and reliable compared to splitting of power between PCBC. Because, each converter is processing much less power and therefore, the power losses during conversion process are comparatively low, offering much efficient solution.

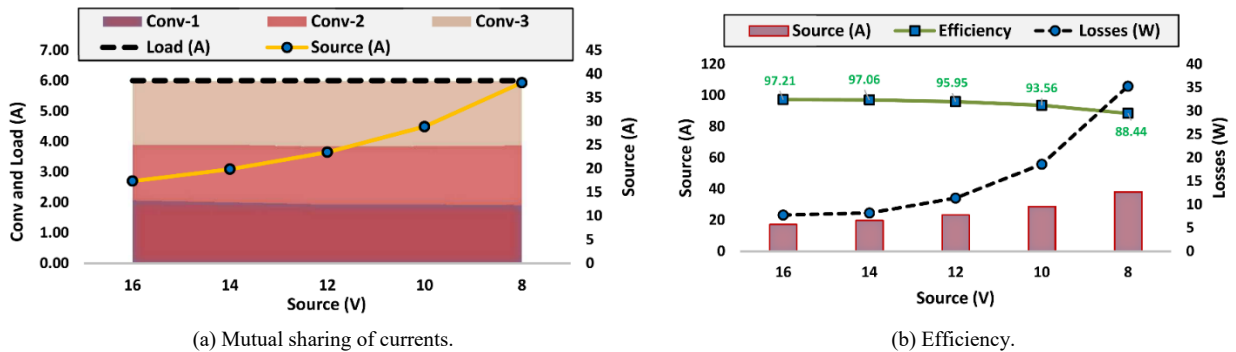


Fig. 6. Performance trend for Test-1.

4.2. Test-2: Variable current, high power loading conditions (at constant source voltage)

In Test-2, virtual environment is emulated with variable loading conditions and constant source voltage. The source is fixed to 16V and load is systematically programmed to draw 2A-12A with constant regulated 45V at output as depicted in Table A2. This corresponds to variable high power loading condition. During Test-2, the load power varied from 90W to 540W. To meet the rising demand of load, cumulative DC and CF both increase due to on circuit regulation. This increment results in ramping up the source currents as shown in Fig. 7(a), to balance the power conversion. However, more the source currents, more the losses are during the conversion process. Therefore, with gradual increment in load demand, the efficiency of system decreases, by Fig. 7(b). During high power variable loading, power is ingeniously distributed among converters.

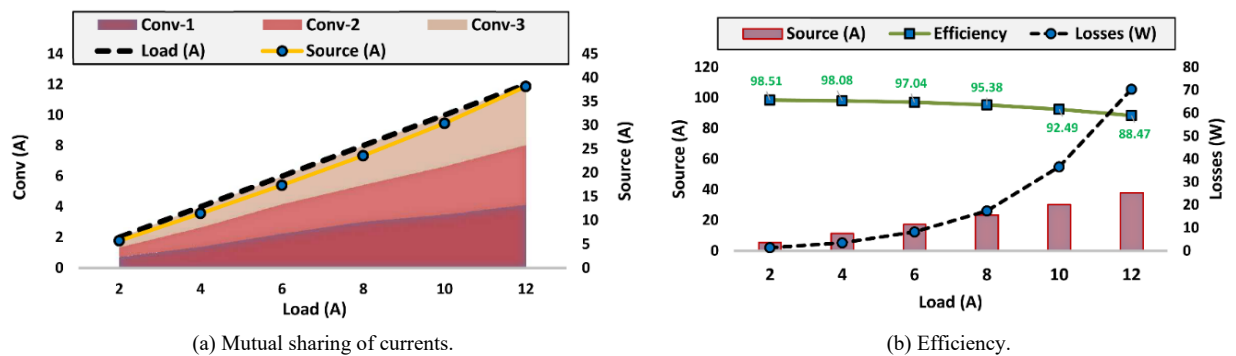


Fig. 7. Performance trend for Test-2.

5. Conclusions and Remarks

To address the efficiency and reliability-concerned problems especially in LV-HP applications, this paper contributes an ingenious interface of PCBC along with proper placement of equalization filter with RBD to enhance the mutual/safe sharing of load power. The topology is appropriate for applications with high power loads such as traction motors derived through low voltage sources such as FC and photovoltaic based energy systems. An experimental setup with programmable devices, boost converters and passive filter elements is utilized to mimic the

behavior of FC and HP load at the same time. Furthermore, various real-time environments are emulated by manipulating programmable devices and readings have been recorded and critically analyzed in variable experimental conditions. The main remarks and recommendations concerning this setup are: *i)* the appropriate working of PCBC is dependent on tight matching of duty cycle of individual converter and accurate design/placement of equalization filter. *ii)* RBD play an important role in the filter circuit to enhance the protection and sharing capacity of converters. *iii)* Moreover, on circuit regulation coupled with minor manual tuning are required to work in conjunction to keep the converters working in vicinity to meet constant load voltages. The results obtained clearly portrays reliable and efficient operation of parallel-coupled converters under HP loading conditions with the proposed converter's connection and filter topology.

Appendix

Table A1. Recorded readings of Test-1.

Voltage (V)			Current (A)					Adaptive Cumulative		Power (W) and Efficiency			
V _S	V _{LO}	V _D	Source	Conv1	Conv2	Conv3	Load	CF	DC	P _L	P _S	P _R	Efficiency
16	45	1.29	17.36	2.07	1.83	2.10	6	2.893	0.654	270	278	8	97.21
14	45	1.36	19.87	2.01	1.89	2.10	6	3.312	0.698	270	278	8	97.06
12	45	1.90	23.45	1.94	1.90	2.16	6	3.908	0.744	270	281	11	95.95
10	45	3.10	28.86	1.94	1.92	2.14	6	4.810	0.792	270	289	19	93.56
8	45	5.88	38.16	1.91	1.96	2.12	6	6.360	0.843	270	305	35	88.44

Table A2. Recorded readings of Test-2.

Current (A)					Adaptive Cumulative		Power (W) and Efficiency				Voltage (V)		
Load	Source	Conv1	Conv2	Conv3	CF	DC	P _S	P _L	P _R	Efficiency	V _S	V _{LO}	V _D
2	5.71	0.74	0.62	0.64	2.855	0.650	91	90	1	98.51	16	45	0.68
4	11.47	1.4	1.26	1.34	2.868	0.651	184	180	4	98.08	16	45	0.88
6	17.39	2.25	1.92	1.83	2.898	0.655	278	270	8	97.04	16	45	1.37
8	23.59	3.04	2.4	2.56	2.949	0.661	377	360	17	95.38	16	45	2.18
10	30.41	3.5	3.15	3.35	3.041	0.671	487	450	37	92.49	16	45	3.66
12	38.15	4.14	3.9	3.96	3.179	0.685	610	540	70	88.47	16	45	5.87

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