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# Sleep Transistors to Improve the Process Variability and Soft Error Susceptibility

Alexandra L. Zimpeck<sup>1,2</sup>, Cristina Meinhardt<sup>3</sup>, Laurent Artola<sup>2</sup>, Guillaume Hubert<sup>2</sup>, Fernanda L. Kastensmidt<sup>1</sup>, Ricardo Reis<sup>1</sup>

<sup>1</sup> Instituto de Informática, PPGC/PGMicro, Universidade Federal do Rio Grande do Sul (UFRGS), Porto Alegre, Brazil

<sup>2</sup> ONERA/DPHY, Université de Toulouse, Toulouse, France

<sup>3</sup> Departamento de Informática e Estatística, Universidade Federal de Santa Catarina (UFSC), Florianópolis, Brazil

alzimpeck@inf.ufrgs.br, cristina.meinhardt@ufsc.br, {laurent.artola, guillaume.hubert}@onera.fr, {fglima, reis}@inf.ufrgs.br

**Abstract**—This paper evaluates the potential of using the sleep transistor in FinFET logic cells to mitigate the process variability effects and the soft error susceptibility. The insertion of a sleep transistor improves up to 40.6% the delay variability and up to 12.4% the power variability. Moreover, the design with a sleep transistor became all logic cells investigated free of faults, independently of the supply voltage applied in the design.

**Keywords**—FinFET; reliability; soft error; process variability; mitigation; microelectronics.

## I. CIRCUIT DESIGN FOR IMPROVE THE RELIABILITY

Typically, the lithography step uses ultra-violet light to transfer the geometric patterns to the thin wafers of silicon. FinFET technologies tried to adopt extreme ultra-violet (EUV) for all of the layers to provide simple and cost-effectiveness designs. However, the wavelength has not kept up with the device scaling, introducing challenges to print the small standards required when the technology nodes reach 14nm and beyond [1]. Multiple patterning is a method used to overcome some lithography limitations and ensure enough resolution in the manufacturing process [2]. The complexity arises because the regular mask is broken up into four incremental mask levels (or two in case of double patterning) where each of them has variations which do not correlate with each other [3]. Also, it is necessary to align the mask layers accurately on top of each other, obeying the overlay requirements.

For these reasons, FinFET technologies are more prone to suffer from process variations such as the line edge roughness (LER) and metal gate granularity (MGG) [4]. These sources of variation generally maintain the chip functioning correctly, but it fails to meet some performance or power criteria increasing the parametric yield loss. In general, nanometer technologies tend to be more susceptible to soft errors (SE) due to higher-frequency operation, low supply voltages, and reduced intrinsic capacitances. The 3D structure of FinFET minimizes the volume of silicon exposed to the charge collection process, decreasing the soft error susceptibility. However, the process variability can change the linear energy transfer (LET) to induce a soft error. Then, even FinFET circuits can become less robust due to transient faults [5]. The impact of these issues intensifies even more as technology scaling advance more in-depth in the nanometer regime, decreasing the reliability of the circuits and increasing the need to devise techniques to effectively deal with these controversies [6].

The most effective approaches for mitigating the process variability and transient faults are commonly related to use different structures and material during the fabrication process, or hardware replication, respectively. However, manufacturing changes have an expensive cost and high complexity involved, as well as the hardware redundancy introduces large overhead. Circuit-level mitigation techniques can be explored in the design, modifying logic cells to achieve more robust solutions. These adjustments can be related to the insertion of some components, transistor reordering or sizing, scaling up the supply voltage, or generating different gate topologies that implement the same function.

Some related works investigate the replacement of traditional inverters by Schmitt Triggers in FinFET full-adders showing up to be 37% more robust to the process variability impact [7]. Also, the concept of strengthening was applied in a FinFET inverter and compared with classical methods. The results show a considerable increase in the charge needed to upset the node [8]. In another work, the dual-interlocked logic family demonstrates to be more robust to single event transient (SET) propagation even for dual-node strikes with a beneficial tradeoff in area and power [9].

However, there is a lack of works applying circuit-level techniques to reduce the process variation effects, even less to decrease the SE susceptibility in FinFET technologies. Complex gates implemented with multi-level design improves the robustness of gates to process variations and soft error susceptibility. Multi-level topologies improve by up to 50% the fault masking from SET effects and mitigate more than 50% the delay variability [10]. Recently, the adoption of decoupling cells in the gate output showed to attenuate at least 3% of delay variability independently of the levels of variation, but only with levels of variation above 4%, this technique is suitable for power variability control [11]. The SET weakness decreases by around 10% using decoupling cells in the design [12].

In this regard, the investigation of circuit-level approaches as a manner to attenuate soft errors and process variations can be an interesting solution for the semiconductor industries. Thus, this paper explores one more circuit-level technique, called sleep transistor, for increasing the robustness of a set of FinFET logic gates under these challenges. This approach already was studied in [13] for process variability mitigation in planar technologies. The technical drawbacks about area, performance and power consumption are briefly reported in this work.

## II. SLEEP TRANSISTOR TECHNIQUE

The power-gating is one strategy widely employed in low power designs to shut off the circuit blocks that are not in use, improving the overall power on a chip [13]. The difference among the power-gating designs is the granularity of the blocks. This work focuses on a fine-grained model where a sleep transistor is added to every FinFET cell. However, for larger circuits, the block-grained style is more indicated to avoid the area overhead [13].

Fig. 1 illustrates a generic logic block (a) and the AOI21 gate (b) as an example with a sleep transistor placed between the pull-down network and the ground rail. The sleep signal is used to control the ‘active’ (sleep = 0) and ‘idle’ (sleep = 1) states of the transistor. When the sleep transistor is in active mode, it guarantees a typical connection from logic gate to the ground rail acting as a supply voltage regulator that improves the process variability effects in the circuits. In the standby mode, the sleep transistor is turned off, disconnecting the virtual ground ( $V_{GND}$ ) from the physical ground. This behavior aims to reduce the leakage currents, transient faults, and negative bias temperature instability (NBTI) effects [14].

However, two fundamental points must be considered to the sleep transistor technique to be successfully applied: (1) the correct control of the sleep signal; and (2) the adoption of proper sizing. The main disadvantage of this technique is performance degradation when the sleep transistor is in the active mode, leading this path to become the worst-case delay.

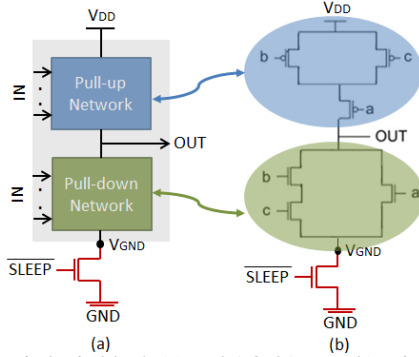


Fig. 1 Generic logic block (a) and AOI21 gate (b) using sleep transistor

## III. METHODOLOGY

For evaluating the sleep transistor technique potential, this work considers as case-study a set of basic and complex cells presented in the first column of Table II. The design of each cell was changed, as described in Fig. 1 to improve the circuit robustness against process variability and radiation-induced soft errors.

For scaling the channel width of FinFETs, it is necessary to increase the number of fins connected in parallel using a discrete sizing. All transistors of logic cells use the symmetric transistor sizing. The number of fins is equal to three to avoid overly difficult routing and poor density [15]. The design with a sleep transistor was tested considering different sizing, with a number of fins ranging from three to five fins.

All layouts were implemented based on the design rules of the 7-nm FinFET predictive PDK developed by ASU in collaboration with ARM Ltd [16]. The standard cell height is

set as 7.5 tracks of metal 2 (M2). The Virtuoso tool was adopted for physical design. After, all layouts were submitted to the verification flow, and the parasitic extraction using the Calibre from Mentor. Table I summarizes the main layout layers and the characteristics of the regular threshold voltage (RVT) devices. First, all these steps were executed for the standard version of the gates, i.e., without sleep transistors. After, the sleep transistor is inserted in the design to verify its effectiveness in mitigating the process variability and soft errors susceptibility. Fig. 2 shows an example of the standard layout and the layout with sleep transistor applied to the AOI21 gate to illustrate the difference in area inserted by the technique. In this work, the cell height is the same for all cells. The extra transistor alters the layout width, increasing the area about 16% on average and adding at least an extra metal 1 (M1) segment and also a gate layer.

Process variability is verified through the 2000 Monte Carlo (MC) simulations performed in SPECTRE from Cadence [17], using the netlist of gates after the parasitic extraction and the RVT electrical model from ASAP7. A Gaussian function with 3-sigma varying from 1% to 5% models the work-function (WF). The variability database provides the minimum (min) and maximum (max) values, the mean ( $\mu$ ), the standard deviation ( $\sigma$ ), and the skewness for all timing arcs and power consumption. In the propagation delay analysis, it is used the worst-case as a reference.

Table I. Device parameters and layout layers from ASAP7 [16]

Device Parameters		Layout Layers (nm)		
Gate length	21nm	Width	Pitch	
Fin thickness	6.5nm	Fin	6.5	27
Fin height	32nm	Active	54	108
Oxide thickness	2.1nm	Gate	21	54
Channel doping	$1 \times 10^{22} \text{ m}^{-3}$	SDT/LISD	25	54
S/D doping	$2 \times 10^{26} \text{ m}^{-3}$	LIG	16	54
Work-Function	4.3720eV	VIA0-3	18	25
Function	PFET	M1-3	18	36

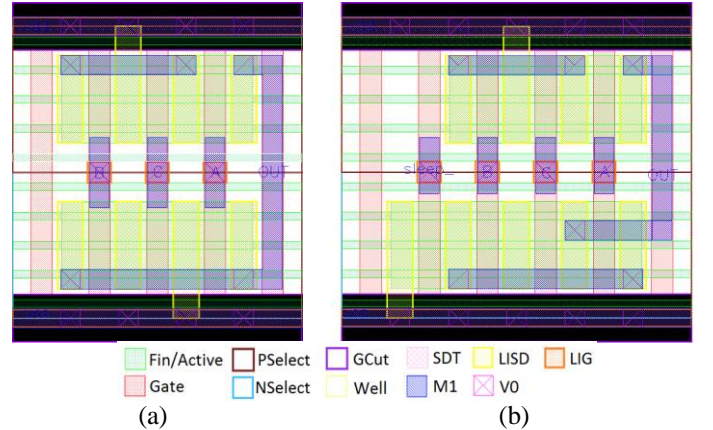


Fig. 2 AOI21 standard layout (a) and AOI21 layout with sleep transistor technique ( $N_{FIN} = 3$ ) (b)

The soft error estimation is done using the MUSCA SEP3, a prediction platform developed by ONERA [18]. This tool is based on a Monte Carlo approach that deals with the targeted radiation environment (space, avionics, ground), the layout characteristics, and with the electrical properties of devices.

The front end of line (FEOL) report extracted from the layout in the geometric data stream (GDS) format determines the charge collection mechanism. The SET database is generated considering the radiation environment features, core voltage, and temperature conditions. Once done, it is composed of a set of current sources to be injected in the sensitive drains through the SPICE simulations. This work focuses in low LET values (from 5 to 15MeV.cm<sup>2</sup>.mg<sup>-1</sup>), heavy ion irradiation at a normal angle of incidence, room temperature (27°C), and with the supply voltage varying from 0.7V to 0.3V. These LET values have been targeted because corresponds to secondary particles induced by neutrons at avionic and ground applications. A fault is detected/considered if the voltage amplitude of the output node exceeds the gate threshold voltage ( $V_{DD}/2$ ).

This work considers two figures of merit for evaluating the capability of sleep transistors in the variability mitigation: 1) the normalized standard deviation ( $\sigma/\mu$ ), which indicates the sensitivity of gates to the process variability; and 2) the delta relation ( $\Delta$ ) to specify how much one gate is more robust to process variability when sleep transistors are adopted in the design. Otherwise, the sensitivity of logic gates exposed to ionizing radiation is described in terms of the cross-section. This metric quantifies the probability of an energetic particle crossing the area of 1cm<sup>2</sup> and to produce a transient event. A design is pointed out as the best choice to mitigate the process variability and the SE susceptibility if it has the lowest values for  $\sigma/\mu$  relation and cross-section, respectively.

#### IV. PROCESS AND RADIATION MITIGATION WITH SLEEP TRANSISTORS

The results show that, in general, the insertion of sleep transistors with three fins is an effective technique to attenuate the effects of process variability, as shown in Table II. Except for the inverter, the power variability of the evaluated logic gates is improved, i.e., the  $\sigma/\mu$  relation reduces when the sleep

transistor is added in the design. The gains, which are represented by delta relation, can reach until 9.6% and 12.4% with the NOR4 gate under 3% and 5% of the variation, respectively. Higher levels of WF variation intensifies power variability mitigation. Moreover, the basic (NAND/NOR) and complex (AOI/OAI) gates with a larger number of inputs present more benefits regarding power variability reduction.

The NAND2 gate can obtain until 15.2% and 17.1% of attenuation with 3% and 5% of the variation, respectively. The NAND gate with three and four inputs has fewer gains. The major improvement in the delay variability can be observed in the AOI21 and OAI gates. The mitigation is 37.5% and 36.4% for 3% and 5% of WF variation on average, respectively. Nevertheless, the sleep transistor technique introduces some drawbacks in the delay variability for the inverter, NOR gates, and the AOI211 gate. This worsening can be related to how the transistors in the pull-down network are arranged together with the sleep transistor.

Depending on the application, a trade-off needs to be done to evaluate the sleep transistor adoption. The comparison between a standard design and one using sleep transistors with three fins ensures interesting reductions in the  $\sigma/\mu$  relation, despite the increase of 16.6% in the area of all gates evaluated. The penalty in the delay and power due to the use of sleep transistor is around 22.6% and 79.2% on average, respectively. The significant impact on power needs to be better analyzed.

Fig. 3 shows the detailed AOI21 gate results as an example of the influence of the sleep transistor sizing in the process variability mitigation. All the other logic gates presented a similar behavior adopting different sleep transistor sizing. Because of that, the results for other gates were omitted for compactness. Independently of the level of variation, larger sleep transistors contribute less than 2% both for power and delay mitigation, if compared with the lower version (3 fins). In this way, the best alternative is to use a smaller sleep transistor, ensuring favorable process variability mitigation and avoiding even more penalties in area, power, and delay.

Table II. The sensitivity of logic gates considering the standard version and applying the sleep transistor technique

Logic Gates		Nom. Delay (ps)	Delay Variability						Nom. Power (nW)	Power variability					
			3%			5%				3%			5%		
			$\mu$ (ps)	$\sigma/\mu$ (%)	$\Delta$ (%)	$\mu$ (ps)	$\sigma/\mu$ (%)	$\Delta$ (%)		$\mu$ (nW)	$\sigma/\mu$ (%)	$\Delta$ (%)	$\mu$ (nW)	$\sigma/\mu$ (%)	$\Delta$ (%)
INV	Std	6.3	6.6	18.01	-47.9	7.2	34.02	-24.1	427	442	11.92	-11.1	485	51.83	1.0
	Sleep	6.4	16.0	34.60		18.7	44.85		631	713	13.25		786	51.32	
NAND2	Std	9.6	10.0	15.93	15.2	10.7	29.10	17.1	540	547	10.22	2.7	596	49.19	7.8
	Sleep	16.0	16.9	13.51		18.0	24.13		757	851	9.95		922	45.33	
NAND3	Std	14.2	14.9	18.26	14.1	16.0	31.35	15.8	591	624	12.18	6.8	689	56.05	10.6
	Sleep	21.0	22.3	15.68		23.9	26.39		849	954	11.35		1043	50.11	
NAND4	Std	19.2	20.4	19.44	12.8	21.8	32.05	13.6	663	689	13.79	8.6	769	61.97	11.6
	Sleep	26.4	28.3	16.95		30.2	27.67		904	1035	12.60		1141	54.74	
NOR2	Std	12.6	13.7	23.68	-2.9	14.8	39.90	-3.0	777	865	10.36	8.0	936	49.20	10.1
	Sleep	12.9	14.0	24.37		15.2	41.09		773	868	9.96		937	44.81	
NOR3	Std	19.9	21.8	24.70	-2.3	22.7	40.64	-2.6	626	645	13.20	8.2	711	53.28	10.8
	Sleep	19.5	21.5	25.27		24.0	41.69		870	981	12.11		1069	47.51	
NOR4	Std	28.1	30.8	24.64	-2.0	32.9	40.60	-2.3	691	722	15.24	9.6	803	57.51	12.4
	Sleep	27.9	31.4	25.13		33.7	41.54		949	1075	13.78		1181	50.40	
AOI21	Std	14.1	15.2	23.10	39.8	16.4	39.53	37.3	615	658	10.79	4.1	718	49.89	8.5
	Sleep	14.4	15.6	13.91		16.8	24.79		892	993	10.35		1075	45.63	
OAI21	Std	14.2	15.3	23.25	40.6	16.5	39.80	38.4	576	589	10.52	4.3	646	55.40	7.9
	Sleep	17.5	18.4	13.82		19.6	24.53		779	883	10.08		962	51.00	
AOI211	Std	21.9	23.9	24.12	-1.9	25.6	40.45	-2.0	649	670	13.22	7.6	743	58.03	11.5
	Sleep	22.3	24.5	24.54		26.3	41.24		893	1006	12.21		1102	51.36	
OAI211	Std	15.7	16.9	23.23	32.0	18.1	40.02	33.4	605	621	11.50	5.0	689	62.20	8.6
	Sleep	20.5	22.0	15.80		23.7	26.67		805	910	10.93		1003	56.83	

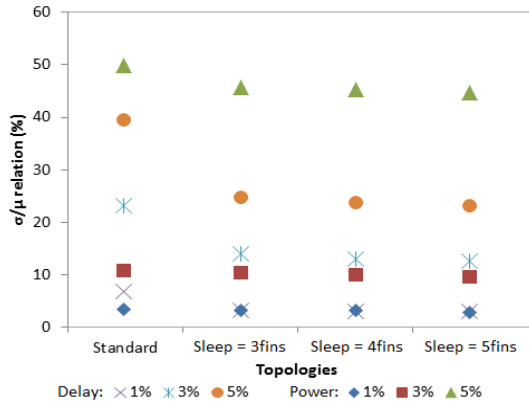


Fig. 3 Impact of sleep transistor sizing in the process variability mitigation of AOI21 gate

The SE susceptibility of some logic gates designed using the standard version were evaluated considering different core voltages and LET values. For all LETs investigated, the logic gates are free of faults at 0.6V and the core voltage. For a LET of  $5\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , soft errors were only seen in the output of gates at 0.3V. On the other hand, with higher LET ( $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ) is possible to observe some transient faults at 0.5V.

Fig. 4 shows the SET cross-section of AOI21, NAND2 and NOR2 cells at near-threshold regime (0.3V) considering low LET values. The AOI21 cell is most susceptible to soft error. However, the increased LET from 10 to  $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$  does not impact the cross-section significantly. On the other hand, the cross-section of basic cells increases almost linearly with the LET. The NOR2 cell is around 17.4%, 21.7%, and 25.5% more robust than NAND2 cell to soft error impact for LETs equal to 5, 10, and  $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ , respectively. The error bars are defined as one divided by the square root of the number of SETs that represent the statistical error induced by MC simulations.

The robustness of logic gates against soft error is estimated when a sleep transistor was added to the design considering low LET values (5, 10 and  $15\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ ), and varying the core voltage from 0.7V to 0.3V. This technique increases the capacitance at the nodes and decreases the leakage currents, improving, even more, the critical charge. The results obtained with designs adopting sleep transistors are promising for soft error mitigation. For all logic gates investigated, no events are seen at the output, independently of the LET or core voltage applied in the design.

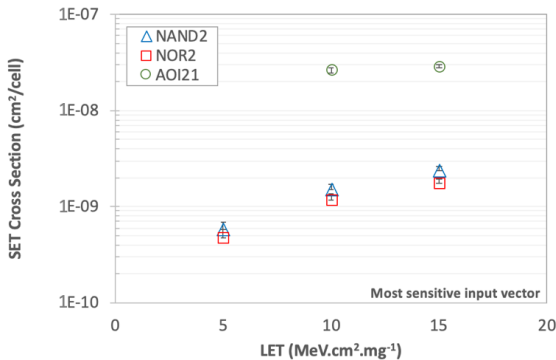


Fig. 4 SET cross-section of standard logic gates operating at near-threshold regime (0.3V) for low LET values

## V. CONCLUSIONS

This work investigates the use of sleep transistors, a power-gating method, as a manner to decrease the impact of process variability and the SE susceptibility in logic gates designed using the 7-nm predictive FinFET PDK. Except for inverters, this technique is very hopeful for power variability with improvements up to 9.6% for 3% of variation from nominal values. These gains increase even more when higher levels of WFF are evaluated, reaching up to 12.4% for the NOR4 gate. For delay variability, the AOI21 and OAI gates are at least 32% more robust as well as the NAND gates becomes at least 15.2% less sensitive. The adoption of sleep transistors for the gates with many transistors in parallel in the pull-down network is not advantageous for the delay variability. Finally, the use of a design with a sleep transistor allows that all gates studied become free of faults even at the near-threshold regime.

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