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Abstract

Monolithic optoelectronic integrated circuits, OEICs are seen as key enabling technologies to minimal power loss criteria. Monolithic OEICs combine, on the same die, cutting-edge optical devices and high speed III-V electronics able to generate terahertz signal targeting beyond-5G networks. Computationally efficient compact models compatible with existing software tool and design flow are essential for timely and cost-effective OEIC achievement. The analog nature of photonic devices wholly justifies the use of methodologies alike the ones employed in electronic design automation, through implementation of accurate (and SPICE-compatible) compact models. This multidisciplinary work, describes an efficient compact model for Uni-Traveling Carrier photodiodes (UTC PD) which is a key component for OEICs. Its equations feature the UTC PD electronic transport and frequency response along with its photocurrent under applied optical power. It also dynamically takes into account the device junction temperature, accounting for the self-heating effect. Excellent agreement between model and measurements as well as model scalability (several geometries have been validated) has been achieved that marks the first demonstration of a multi-physics, computationally efficient and versatile compact model for UTC-PDs.

Keywords: Compact model, Optoelectronic integrated circuits, Terahertz communication, Uni-traveling carrier photodiode.

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1. Introduction

In the current age of information technology, the demands for high-speed communication technologies continue to grow as the next generation systems emerge to support a wide range of applications including social, medical, security, space and internet of things (IoT). These systems already serve rapidly growing sectors such as internet which has become an integral part of our daily life or even collision avoidance systems for automobile safety and are working their way to internet of everything (IoE). To meet the meet the speed requirements, the minimum bandwidth requirement for a communication system is expected to reach several tens of GHzs, which in turn mandates an even higher carrier frequency in the THz range (0.1–10 THz) as one of the best potential solutions [1]. This has been the main motivation behind the rapidly growing research in THz wireless communication in the last few years alone. Design of robust and intelligent systems, capable of supporting billions of devices, is mandatory for the upcoming 'Beyond-5G'e networks. Anticipating the evolution of communications systems in the upcoming years (2020-2025) [1-3], photonic and nanoelectronic technologies have captured the attention of a majority of the technology developers. This is greatly motivated by the record levels of integration and communication capacity achievable for heterogeneously integrated photonic integrated circuits on silicon platform [4]. While electronic circuits have already attained a significant degree of integration density over the years, the integration density of photonic circuits is also growing rapidly, having realized the need for high-speed integrated communication technologies. This so-called trend of growth in photonics has been described as the photonic "Moore's Law" [5]. In terms of on-chip integration, opto-electronic integrated circuits have become one of the key enabling terahertz technologies that are achievable through monolithic integration (Fig. 1). Such monolithic integrated circuits typically consist of photonic (such as Uni-Traveling Carrier photodiodes) and electronic modules (such as trans-impedance amplifiers) on InP substrate along with the transmitting antenna in the same die, as illustrated in the schematic in Fig. 1(a) and (b). The principal goal behind design of such circuits is to minimize the losses as well as to enhance the speed of operation as far as possible [6-9]. Monolithic integration has the advantages to (i) optimize the epitaxial design of each device independently, (ii) minimize the distance and the intra-device electronic propagation losses even at very high operating frequencies while (iii) limiting the mutual heat coupling. Hence, optoelectronic integrated circuits (OEIC) are being seen as one of the efficient high-speed solutions to go beyond 5G connectivity due to cost-effective on-chip integration, state-of-the-art photodiodes for photomixing and the potential to integrate the system transparently to an optical network, cutting-edge III-V electronics for high speed and power-handling capacity and power efficient on-chip antennas with high-directivity [1, 10].

Due to the low level of maturity, designing these emerging hybrid photo-electronic circuits would heavily rely on computationally efficient and physics-based models. In addition, due to the increased complexity in synchronising domain-

2

specific design tools for individual circuit blocks, a unified co-designing solution is essential for optimizing design time and costs. Such co-designing requires the model to ensure computational efficiency while meeting a specific set of multidisciplinary criteria that include as physics-based description of carrier transport in both electrical and photonic parts. Other major design requirements include interconnect modelling at high frequency of operation using electromagnetic simulation and reliability modelling that mainly includes modelling of thermal behaviour at extreme operating powers as well as elevated temperatures. Thermal issues are particularly severe due to the high inherent heat dissipation in UTC-photodiodes which is worsened by the self-heating effects in electronic circuits. Therefore, the model also needs to provide accurate description of the thermal effects. Hence, from a design point of view, a multi-disciplinary approach is mandatory in order to unify the electrical and electromagnetic, photonic as well as reliability aspects using either additional design/software tools or through a systematic assembly of existing software tools [11].
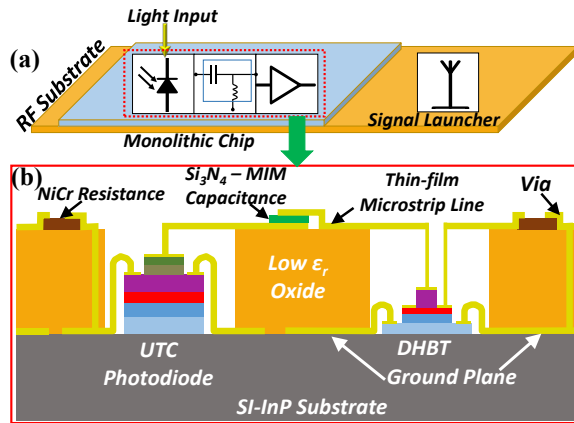

FIG. 1: (a) Schematic of future Optoelectronic Monolithic chip; (b) Monolithic integration of the photodiode and the DHBT based amplifier on the same InP substrate.

In communications systems, photodetectors play a pivotal role in optical detection. It is required that they be sensitive to the wavelength used and have a fairly high bandwidth compared to the data rate. The condition necessary for absorption at a wavelength of 1.55 μm is that the absorption layer of the photodetector has a narrow energy band gap (less than 0.8 eV). Among the available photodetector

technologies the most noteworthy are PIN photodiodes and Uni-Traveling Carrier photodiodes (UTC-PD). In PIN photodiodes, photo-generated electron and holes are swept away towards the contacts by the drift field in the space charge region. The carrier transit time through the structure is thus limited by hole transport. To circumvent this problem, Ishibashi *et al*. in the NTT Lab had developed a novel photodiode structure, the UTC photodiodes [12]. UTC photodiodes operate on the separation principle of the absorption and the space charge region, thus allowing only diffusion of photo-generated electrons in the space charge zone. As a result, UTC photodiodes demonstrate better performance in speed and power handling than the conventional PIN photodiodes. In addition, the bandwidth of the UTC photodiode may reach a value greater than 600 GHz [9] thereby making them one of the most promising photomixing candidates that have potential Terahertz applications, and especially for optoelectronic integrated circuits [1, 7, 9-10, 13-17]. Owing to their analog nature, photonic devices also urgently require methodologies equivalent to those employed in matured electronic design automation, utilizing accurate circuit-level (SPICE-compatible) compact models and simulation. At present, no such equivalent software tools truly exist in the field of optoelectronics. However, there are many reports on the efforts of analysis and modelling of static and dynamic as well as optical behaviour of UTC photodiodes [18-20]. A few noteworthy works include characterization and analysis of the electrical, optical and thermal properties of the UTC-PD technology [10, 15-16], electrical equivalent circuit consisting of distributed resistive, capacitive and inductive elements for UTC-PDs [20] and even an electrical equivalent circuit incorporating a current source to represent photocurrents for UTC-PDs [19]. Hence, the recent trend of research on UTC-PDs indicates that the optoelectronics community is looking for an efficient mean to model elementary components in the context of their systems. Yet, there is still a lack of integrated modelling approach towards simulation, validation, and optimization of the individual building blocks of an optical link as well as the entire optical network-on- chip.

As a first step towards developing such a unified modelling solution, the first multi-physics and versatile compact model written using Verilog-A and compatible with the methodology/tool/design flow for electronic circuits, is developed and validated for UTC-PDs, based on the equations of its carrier transport. The analytical model equations capture the electronic transport and frequency response of the photodiode without illumination as well as the behaviour of photocurrent as a function of different applied optical power and its optical criteria. For simulation of thermal effects, the model dynamically recalculates the internal device temperature to describe temperature dependence of UTC-PD characteristics using an additional fictitious node. This implementation describes the effect of self-heating at higher optical power and applied bias considering that the major heat flow within the device is through the InP substrate. Model validation has been performed on three available UTC-PD geometries from a technology developed by University College London, and good model accuracy and scalability have been achieved.

This rest of this paper is organized as follows: section 2 details the model development which includes the analytical model equations for the current and capacitance, including temperature dependence and self-heating effect, with and without illumination. Section 3 provides validation of the scalable model against measurement under various operating conditions, followed by the conclusion.

2. Compact Model Development

In the realm of electronics, the development of compact models has overcome the hindrances in the way of technology design and towards designing at circuit and system levels. Compact models are configured by circuit designers to accurately predict transistor operation, in particular, their carrier transport and electronic properties into circuit simulators. The opportunity to simulate simultaneously UTC-PD devices in a real OEIC design will allow to (i) evaluate the potential improvement in circuit performance compared to conventional non-monolithic design, (ii) develop novel OEIC designs, in particular for beyond 5G applications and (iii) evaluate its integration within system architectures.

2.1 Model Organization

Per standard practice in compact modeling, the model is represented as a black box that contains the analytical model equations based on the UTC-PD physics while the input/output ports are the anode, cathode as well as the optical (Light) signal. The model equations simultaneously incorporate basic semiconductor diode physics as well as the photo-current generation under illumination in UTC-PDs [12, 21-22]. In order to facilitate model scalability, we have used photodioe area-normalized quantities for currents and capacitances throughout the model description. As depicted in the intrinsic part of the equivalent circuit in Fig. 2 (a), parallel to the diode current source, I_D, and the junction capacitance, C_{j0}. the DC photocurrent, I_{photo}, is represented as a voltage dependent current source controlled by the input optical power coupled at the light port. To take the resistance of the reverse biased P-N junction into account, a shunt resistance R_{sh} is added in parallel to the junction capacitance. Lastly, due to the absence of de-embedding test-structures, the parasitic capacitances /inductances due to the RF pads external to the UTC-PD test structures were removed using a lumped element network in the extrinsic part of the model. The extrinsic circuit elements also include a series resistance, R_{series}, for the access lines at the anode terminal as well as the parasitic lumped inductance, L_p, and capacitance, C_p, to represent the RF pads in dynamic simulation. Additionally, the effect of self-heating has been taken into account using an additional fictitious node within the compact model (Fig. 2 (a)) to recalculate the junction temperature dynamically as a function of the applied bias. Note that, in absence of measurement data under such operating conditions that could lead to a steep rise in temperature, model accuracy has not been validated in such cases. Fig. 2 (b) shows a schematic of the UTC-PD structure depicting different epitaxial layers. In order to offer a better visualization of the different elements of the equivalent circuit representation, Fig. 2 (c) shows the placement of Fig. 2(a) as well as the composition of the diode current superimposed within the UTC-PD structure.
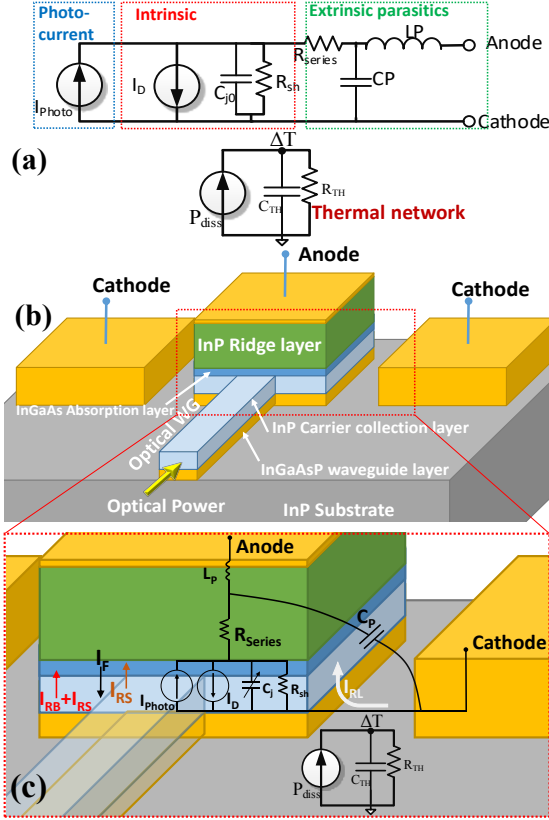
Fig. 2: (a) Equivalent circuit representation for the compact model; (b) Schematic of the UTC-PD structure; (c) elements of the equivalent circuit and diode current contributions within the UTC-PD structure.

2.2. Diode Current

The total UTC-PD current can be macroscopically represented by,

$$I = I_S \left(e^{qV_d / k_B T} - 1 \right) - I_{ph} \tag{1}$$

Where I_S is the reverse saturation or dark current, V_d is the diode voltage and I_{ph} is the photocurrent in reverse bias under illumination. The first term on the right side of the equation is the classical intrinsic diode current, I_D, which has been decomposed in five components (Fig. 2 (c)):

$$I_D = I_F + I_{RS} + I_{RB} + I_{BV} + I_{RL} \tag{2}$$

The current under forward bias, I_F, is given as

$$I_F = Area \cdot J_S(T) \left[\exp\left(\frac{V_d}{NV_t(T)} \right) - 1 \right], V_d > -5NV_t \tag{3}$$

Here N is the emission coefficient, J_S is the reverse saturation current (dark current) density, V_d is the applied forward bias across the photodiode and V_t is the thermal voltage. The diode current under reverse bias, that is the dark current, can be further represented by four contributions which include the reverse saturation current I_{RS}, reverse breakdown current I_{RB} and I_{BV} and reverse leakage current I_{RL}. The reverse leakage current component is specific to this UTC–PD technology under test and it has an expression similar to that of interface generation leakage current in SOI PIN diodes [23]. The individual expressions for the dark current components are as follows [24]:

$$
\left.
\begin{aligned}
& I_{RS} = -Area \cdot J_S(T), V_d \leq -5NV_t, \quad I_{RB} = -I_{BV}, V_d = -BV, \\
& I_{BV} = -Area \cdot J_S(T) \left[\exp\left(-\frac{BV + V_d}{V_t(T)} \right) - 1 \right], V_d < -BV \\
& I_{RL} = -Area \cdot J_R \cdot (T)^{1.5} \exp\left(-\frac{qE_g(T)}{2K_B T} \right) V_d^2 \sqrt{V_{bi} - V_d - V_t(T)}, V_d < V_{ref}
\end{aligned}
\right\} \tag{4}
$$

Here, BV is the reverse breakdown voltage, and E_g is the bandgap of the InGaAs absorption layer, V_{bi} is the junction built-in potential and V_{ref} is the threshold value of reverse bias that governs the dominance of the component I_{RL}. The depletion/junction capacitance of the photodiode is written as,

$$C_{dep} = Area \cdot C_{j0}(T) \left(1 - \frac{V_d}{V_j(T)} \right)^{-M} \tag{5}$$

With C_{j0} being the zero bias junction capacitance per unit area, V_j being the junction potential and M being the grading coefficient of the P-N junction. Note that the temperature dependence of the parameters is already incorporated within the equations (3), (4) and (5), while as mentioned earlier, formulations of current and capacitance use area-normalized quantities such as J_S and C_{j0}. In addition to the model parameters such as C_{j0}, J_S and V_j, temperature dependence of the energy band-gap E_g has also been taken into account, as the following set of equations governing the temperature dependence depict [24],

$$
\left.
\begin{aligned}
& C_{j0}(T) = C_{j0} \left[1 + M \left\{ 4 \times 10^{-4} \times (T - T_0) - \frac{(V_j(T) - V_j)}{V_j} \right\} \right], \\
& J_S(T) = J_S \left(\frac{T}{T_0} \right)^{\frac{X_{ti}}{N}} \exp\left[-\frac{E_g(T_0)}{V_t(T)} \left(1 - \frac{T}{T_0} \right) \right] \\
& V_j(T2) = \left(\frac{T}{T_0} \right) V_j(T_0) - 2V_t(T) \ln\left(\frac{T}{T_0} \right)^{1.5} - \left[\frac{T}{T_0} E_g(T_0) - E_g(T) \right]
\end{aligned}
\right\} \tag{6}
$$

Here T_0 is the nominal temperature, usually considered to be the same as ambient temperature.

2.3. Self-heating Effects

In addition to the temperature dependence of the model parameters included in (4)-(6), accurate

calculation of the junction/device temperature, T, should also account for dynamic self-heating at elevated temperatures as well as high electrical and optical power. This is module is crucial for improving the model accuracy at more extreme operating conditions due to the high inherent heat dissipation in the UTC-PDs [26-27]. As depicted in the equivalent circuit of Fig. 2 (a) the model utilizes an additional thermal node similar to the implementation of self-heating in bipolar transistors [25], which is employed to dynamically recalculate the junction temperature as the operating conditions change. The R-C thermal network consists of a thermal resistance, R_{TH} and a thermal capacitance, C_{TH}, to represent the dynamic behaviour of thermal impedance depending on the operating frequency. The calculation of the junction temperature, T_j, uses the following expressions

$$T = T_j = T_{dev} + R_{TH} P_{diss}, \quad \text{with } Pdiss = I_{Total} V_d \quad (7)$$

The temperature dependence of the thermal resistance is governed by the following equation with its temperature coefficient α [25],

$$R_{TH}(T) = R_{TH}(T_0)\left(1 + \alpha(T - T_0)\right) \quad (8)$$

The temperature coefficient α is a material dependent parameter that governs a power law signifying the temperature dependence of the thermal conductivity which has also been taken into account in the UTC-PD compact model. The expression of the junction temperature in (11) is used to dynamically recalculate the temperature dependence of all model parameters. Lastly, R_{TH} is implemented as scalable in the model governed by the expression, $R_{TH}(T) = R_{TH,norm}(T)/Area$, where $R_{TH,norm}$ is the normalized value of thermal resistance.

2.4. Photo Current

The photocurrent, I_{photo}, is represented as an external current source parallel to the diode current under reverse operating conditions , which is controlled by the input optical or impinging power, P_{opt}. Similar to the diode current scaling equations, to incorporate photocurrent scalability, area-normalized DC photocurrent or the DC photocurrent density, J_{ph}, is used throughout the photocurrent module, which is represented by the following expression,

$$J_{ph} = P_{opt} \times \text{Responsivity}/\text{Area} \quad (9)$$

Where, the *Responsivity* is a measure of the external quantum efficiency of the photodiode, in A/W, and is used as a model parameter for simplicity, even

though it is a function of the optical wavelength. This approach does not affect model accuracy in this study since we have used a fixed wavelength of 1.55 μm (corresponding to the minimum wavelength dispersion) throughout this work. The total photocurrent density can subsequently be decomposed into three components, the absorber layer current densities J1, J2 and the collection layer current density J3, which are written as [21-22],

$$J1 = J_{ph} \frac{W_A}{W_A + W_C} \frac{1}{1 + j\omega\tau_A}, \quad J2 = -J1\left(1 - \frac{q\mu_n n_0 E_{ind}}{J_{ph}}\right) \frac{j\omega\tau_R}{1 + j\omega\tau_R}$$

$$J3 = J_{ph} \frac{W_C}{W_A + W_C} \frac{1}{1 + j\omega\tau_A} \sin(\omega\tau_C/2) \frac{\exp(-\omega\tau_C/2)}{\omega\tau_C/2}$$

(10)

Here, W_A and W_C are two model parameters denoting the widths of the absorber and collection layers, respectively, τ_A is the electron traveling time and τ_R is the dielectric relaxation time in the absorption layer, whereas τ_C is the transit time in the collection layer. E_{ind} is the self-induced field in the absorption layer responsible for change in electron transport from diffusive to drift, μ_n is the electron mobility and n_0 is photo-generated minority electron concentration. The expressions for the time constants, τ_A, τ_C and τ_R implemented in the model are written as [12],

$$\tau_A = \frac{W_A^2}{3D_n} + \frac{W_A}{v_{th}}, \quad \tau_C = \frac{W_C}{v_{sat}}, \quad \tau_R = \frac{\varepsilon_s}{q\mu_h p_0}$$

(11)

Where, D_n is the diffusion coefficient of electron, v_{th} is the thermal velocity in the absorption layer, v_{sat} is the saturation velocity in the collection layer, μ_h is the hole mobility and p_0 is the doping hole density in the absorption layer. Using (9) (11) , the final expression of the total photocurrent can be written as,

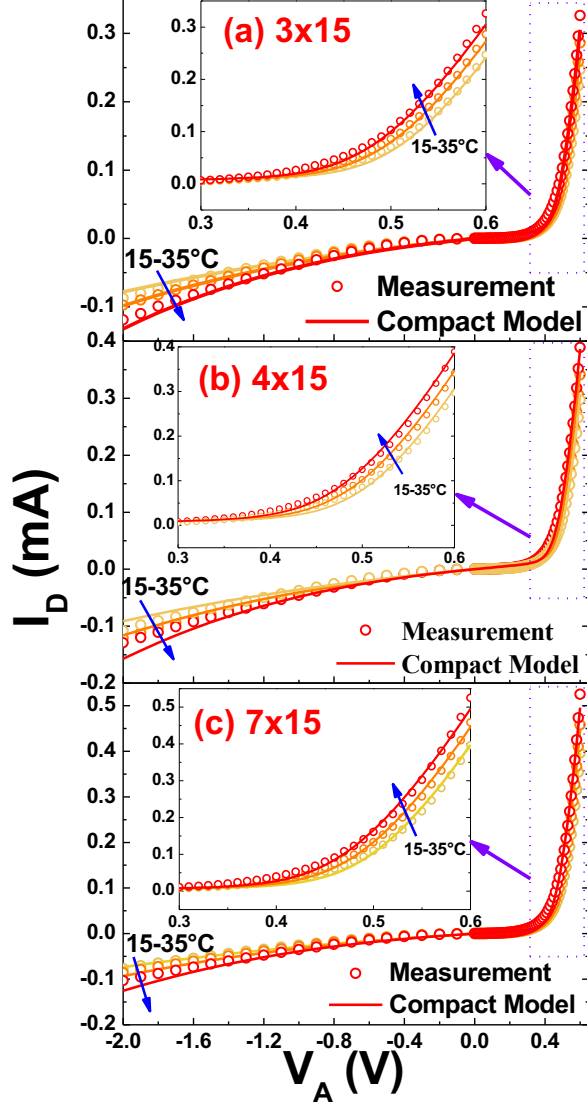$$I_{photo} = Area \cdot (J1 + J2 + J3) \quad (12)$$

6

Fig. 3: Scalable model comparison: I-V characteristics of the UTC-PD geometries with the active are of (a) 3×15 (b) 4×15 and (c) 7×15 μm² at 15 (yellow), 25 (orange) and 35ºC (red). Inset: Forward operating regime

3. Model Validation

The DC and RF measurements at three different ambient temperatures (15, 25 and 35ºC) for both illuminated and dark UTC-PDs under test were performed at the ultrafast photonics laboratory of University College London, which have been used for model validation in this study. Three UTC-PD geometries have been characterized featuring the device areas of 3×15, 4×15 and 7×15 μm². The

epitaxial structure of the photodiodes consists of a 120 nm thick p-doped $In_{0.53}Ga_{0.47}As$ absorption and a 300 nm thick n-doped InP collection layer [28]. The first set of validation was performed against the measured I-V characteristics depicted in Fig. 3 for the three photodiode geometries under forward and reverse bias at 15, 25 and 35ºC (temperature is maintained using a Peltier system). It can be observed from Fig. 3 that the model demonstrates excellent accuracy and scalability at all operating conditions and temperatures. Note that, under bias, the equation of I_{RL} in (4) is crucial for model accuracy.
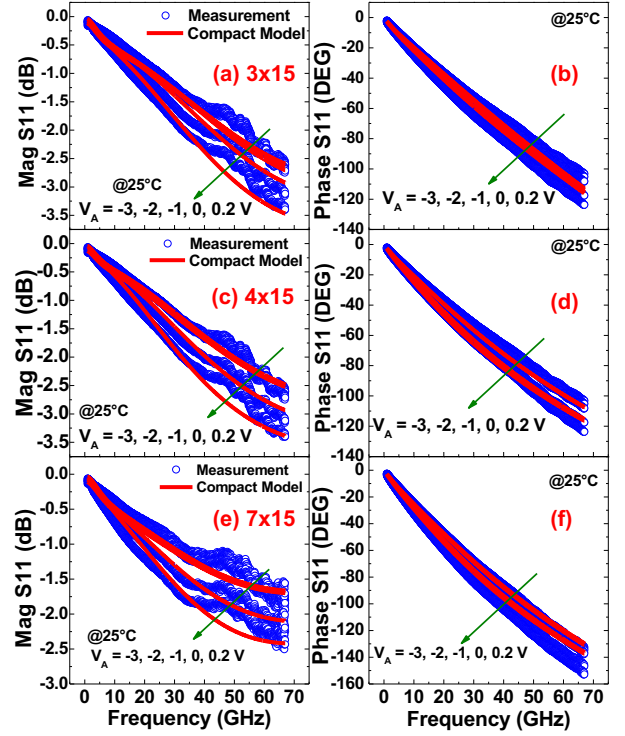

Fig. 4: Measured (symbol) and simulated (line) S11 showing the magnitudes (a)-(c) and the phase (d)-(f) for the three UTC-PD geometries at 25ºC under different bias conditions.

The magnitude and phase of the measured one-port S-parameter (S11) up to frequency of 67 GHz are shown in Figs. 4 (a)-(f) for the three UTC-PD geometries in comparison with the UTC-PD compact model results, further affirming model accuracy under dynamic operating conditions. Due to the absence of de-embedding structures, the Short-Open-Load calibrations were done till the probe tips and the contributions of the pad parasitics were taken into

account by the series access resistance, R_{series}, the lumped parasitic inductance and capacitance, L_P and C_P, into the external sub-circuit of the model. Reference values of these three parameters are reported in [19]. Having these extrinsic parameters extracted with sufficient confidence, the frequency behavior of the intrinsic circuit elements is further analyzed. A good description of the depletion capacitance including its scalability is captured in the model, especially in the entire bias range (-3 to 0.2 V) used during the measurement. However uncertainty in the measurements around 50 GHz is present for all three transistor geometries indicating a calibration issue. Nonetheless, the bias dependence of the junction capacitance is captured fairly well.
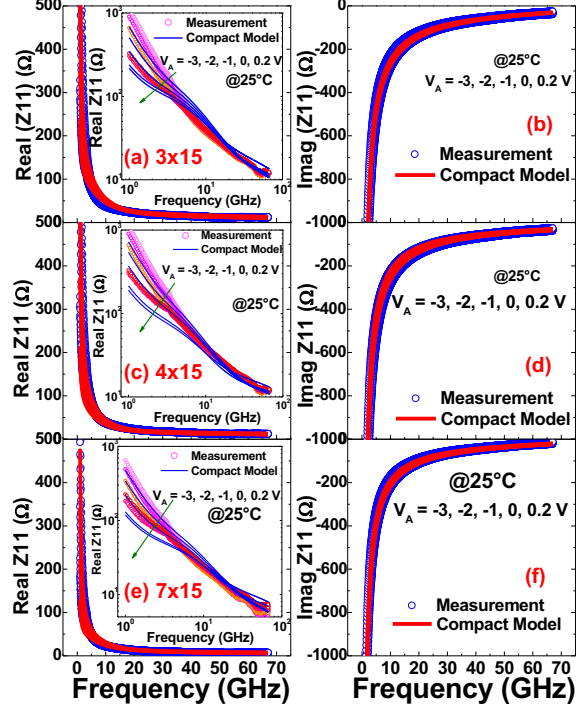

Fig. 5: Measured (symbol) and simulated (line) input impedance (Z11) showing the real (a)-(c) (insets showing the real part in log-log scale) and the imaginary parts (d)-(f), for the three UTC-PD geometries at 25ºC under different bias conditions.

Furthermore, the real and imaginary parts of the one port Z-parameter, *i.e.* the input impedance, Z11, are extracted from the measured one-port S-parameters and are shown in Figs. 5 (a)-(f) for the three UTC-PD geometries. The real part represents the resistive part of Z11 while the imaginary part represents the capacitive reactance of the input impedance. At higher frequencies, the asymptotic nature of the real

part converges to the series resistance value, characteristically 5-10 Ω, while the reactance becomes more inductive. For all the geometries, our compact model accurately describes these effects and provides a precise description of the UTC-PD input impedance throughout the entire frequency range.

Once model accuracy is affirmed for DC and RF characteristics of the UTC PD under unilluminated operating conditions, the compact model is further validated against measurements carried out under illumination for a wide range of optical power (6 to 15 dBm). For the whole set of measurements carried out under optical illumination of the UTC-PDs, a CW Laser of wavelength 1.55 μm (line width 100 kHz) had been used that was guided through an optical fiber.. With a lens at the end of the optical fiber, the optical signal is focused on the absorption layer of the UTC-PD through the optical wave guide (trench) located on the edges of the test structures. Fine adjustments of the fiber locus were done to achieve maximum photocurrent intensity for each optical power.

Fig. 6 compares the measured and simulated photocurrents under optical powers in the range 6 to 15 dBm for all UTC-PD geometries. It can be observed that model simulation shows an excellent agreement with the measurement under the entire range of reverse bias voltages and optical powers, thus validating the accuracy of the implemented physics-based photocurrent equations through (9)-(12). The frequency responses of the UTC-PDs were measured using a lightwave component analyzer (LCA) that records the electrical S-parameters at the output of the photodiode as a result of optical input power. Fig. 7 shows the measured frequency responses under a P_{opt} of 6 dBm compared with model simulation for the three UTC-PD geometries, again demonstrating excellent agreement between the model and the experimental data. .As observed from fig. 7, the 3 dB cut-off frequencies are also well described by the model. Interestingly, it can be verified that the 3 dB cut-off frequency and therefore the bandwidth of the photodiode is proportional to the photodiode geometry: larger area implies bigger capacitance thus increasing the RC delay product and thus resulting in a smaller bandwidth. These results are quite consistent with the results reported in [19].
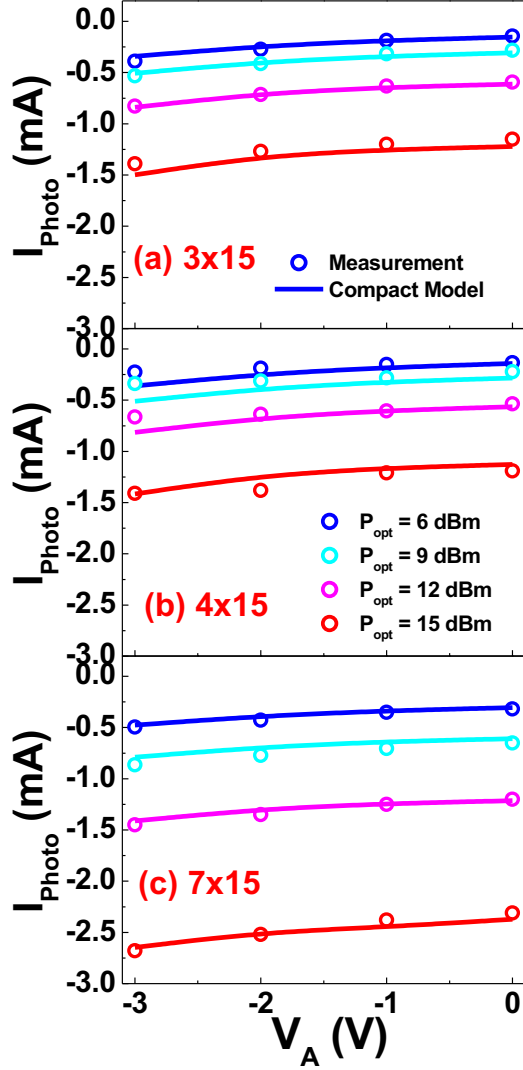
Fig. 6: Scalable model comparison: Measured (symbol) and simulated (line) Photocurrent of the UTC-PD geometries with the active are of (a) 3×15 (b) 4×15 and (c) 7×15 μm² as a function of reverse bias at different optical powers, measured at 20ºC.
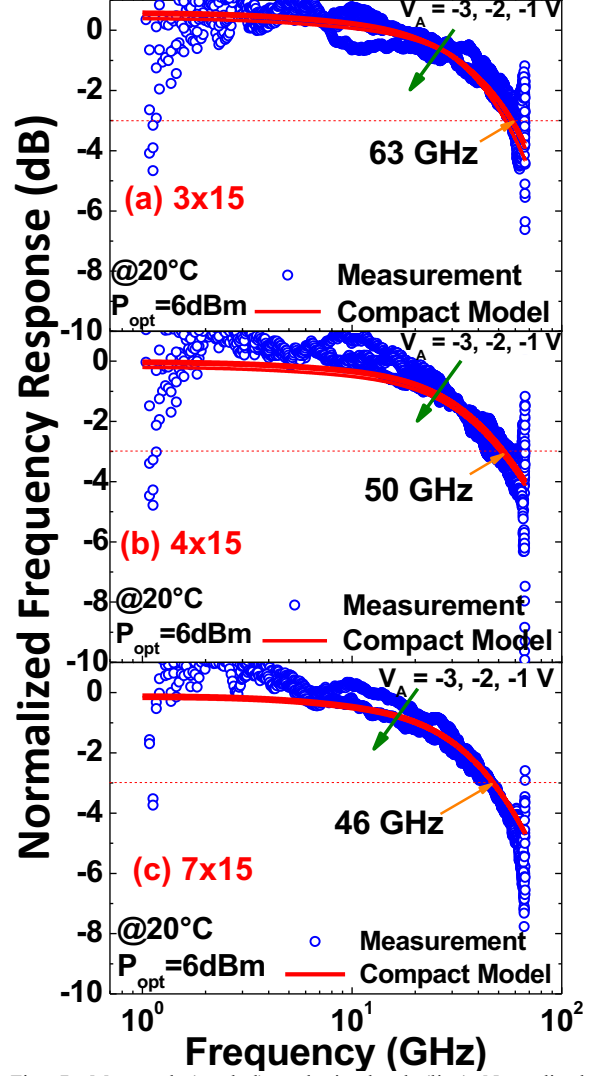
Fig. 7: Measured (symbol) and simulated (line) Normalized Frequency Response of the UTC-PD geometries with the active are of (a) 3×15 (b) 4×15 and (c) 7×15 μm² measured at 20ºC and an optical power of 6 dBm showing the 3 dB cut-off frequencies.

Finally, Fig. 8 (a)-(c) shows the thermal simulation results performed using COMSOL under a high optical power of 150 mW at a bias of -2V, depicting the heat generation source (Fig. 8 (a)) within the UTC-PD area, the cross section (Fig. 8 (b)) that shows the heat distribution contours (Fig. 8 (c)) within the diode structure. The simulation ignores convective heat transfer as well as insignificant radiative heat transfer. The impact of self-heating can

be observed dominantly from model simulation at higher bias (>-2V) and optical power (>12dBm). Fig. 8 (d) shows the thermal resistance extracted from the compact model simulation as a function of the device widths (for a fixed length of 15 µm). A very good geometry scalability of the thermal impedance is also observed. Also, temperature dependence of the thermal conductivity is taken into account through the coefficient α that gives an accurate description of the thermal effects at elevated temperatures due to pronounced self-heating.
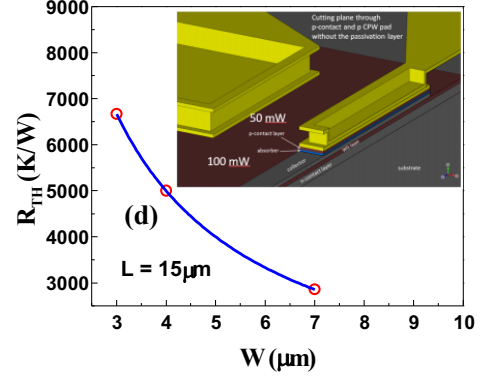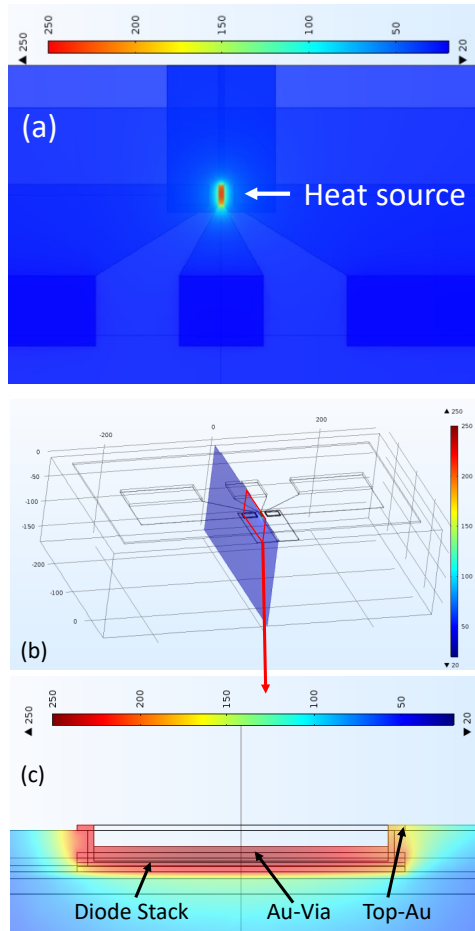

Fig. 8: (a) Thermal simulation of UTC-PD structure showing the location of the heat source; (b) a cross section showing the 2D plane of analysis within the UTC-PD geometry; (c) Distribution contours of heat generation; (d) Thermal resistance as a function of the UTC-PD width for a fixed length of 15 µm (inset showing the complete simulated structure).

4. Conclusion

In this work we elaborate the first electrical compact model for UTC-PDs compatible with the existing design infra-structure of the electronic circuits. The compact model is developed based on the UTC-PD transport physics and the model equations accurately capture the behavior of the photocurrent as a function of the input optical power and temperature. Model scalability is also demonstrated which is essential for circuit designers. Moreover, the developed compact model is fully compatible with commercial verilog-A circuit simulation tools. With the growing demand for high-speed communication systems and 5G networks, design of phonics based systems needs a straightforward approach similar to the well-established industry-standard process flow for electronics-only systems. The benefit of developing this electrical compact model for UTC-PDs is that it facilitates single simulator based co-designing of multi-physics photo-electronic systems. This marks the first step towards realizing a unified and holistic (electronic, photonic, thermal) design environment for optoelectronic monolithic integrated circuits which will ultimately aid designers of next generation communication technologies.

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