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Abstract— **This paper presents a low-noise M&NEMS microphone. The resistive accelerometer and the electronic interface are respectively a silicon nanowires and a fourth-order single-bit Continuous-Time (CT) ΔΣ modulator. The study and analysis of the M&NEMS microphone noise is carefully reported. To eliminate the offset and 1/*f* noise of the first integrator, Chopper Stabilization (CHS) technique is implemented around this block. The CT ΔΣ modulator is implemented in a 65-nm CMOS technology. The supply voltage is 1.2-V while the power consumption is 370-µW and the core area is 0.4-mm^2. The circuit was fabricated and measured. From measurement results over a signal bandwidth of 20-kHz, it achieves a peak signal-to-noise ratio (SNR) of 103-dB, a peak signal-to-noise and distortion ratio (SNDR) of 102-dB and a dynamic range (DR) of 108-dB.**

Keywords—MEMS, ΔΣ modulator, chopper stabilization, low-noise, amplifier.

I. INTRODUCTION

Audio applications use multibit ΔΣ modulators as analog-to-digital converters (ADC). These modulators are based in a switched capacitor circuit [1-3]. On the other hand, the increasingly popular analog-to-digital converter in low bandwidth applications become the continuous-time modulators. Due to their low power consumption, low noise and high resolution, CT ΔΣ modulator is widely used for audio applications [4-6]. Digital circuits are widely used in the CMOS technology. Therefore, the CMOS transistor size is continuously scaling-down. As a result, the CMOS technology also follows this scaling-down. In the last few years, the deep-submicron CMOS technology is below 28 nm. Therefore, the supply voltage becomes lower than one Volt. The signal swing is reduced because the low supply voltage limits the analog design. As a result, the major building block used by the mixed-signal circuits is the analog-to-digital converter.

The ΔΣ ADC has a high linearity. Therefore, it is most suitable for high-resolution audio systems. The oversampling technique combined with the intrinsic linear single-bit quantizer allows to obtain a high linear ΔΣ ADC. However, its performance is strongly affected by its building block non-ideality. As a result, reducing the building block non ideality as small as possible allows to design a ΔΣ ADC with high performance. The performance becomes even worse if a nanometer CMOS technology is used. Active devices are affected by the limitation of their headroom operation caused by the supply voltage reduction [7]. In addition, the figure-of-merit (FOM) is affected. Moreover, for the same dynamic range, the ΔΣ ADC in this technology requires a low noise floor. Therefore, the performance is affected and the power consumption is increased [8]. The linearity of the converter is the most important parameter to design a high-resolution ΔΣ ADC. Distortion problem increase with decreasing supply voltage as well as the degradation of the CMOS transistor characteristics [9]. The ΔΣ ADC is integrated with the digital circuit on the same chip. It is strongly required to implement the low voltage ΔΣ ADC in nanometer CMOS technology. Moreover, a restricted power consumption ΔΣ ADC is imposed. As a result, the design of a low-power low-voltage ΔΣ ADC in nanometer CMOS technology is highly desirable. Recently, the design of the ΔΣ ADC is very attractive for many companies like Texas Instruments and Analog Devices. Therefore, ΔΣ ADC is widely used in audio applications which they request a high precision circuit [10-12]. The ΔΣ ADC ensures many operations as the signals digitation at IF stage, the out-of-band noise suppression and the selection of the channel [13][14]. Moreover, the ΔΣ ADC is used in many applications like the switching audio amplifier [15], the polar modulation power amplifier [16] and the fractional-N phase-locked loops [17][18].

The objective of this paper is to implement an M&NEMS microphone with a CT ΔΣ modulator, which has a very low FOM, high peak-SNR and peak SNDR. The architecture of the modulator is carefully selected and some circuit innovations are explored. The complete system is fabricated in 65-nm CMOS process and measurement results are discussed. The rest of the paper is organized as follows. Section II presents an overview of our fabricated M&NEMS microphone. Then, Section III provides the CT ΔΣ modulator details. Section IV presents the proposed delay-time CHS technique. Section V presents the measurement results of the CMOS circuit and discussion. Finally, Section VI concludes the paper.

II. M&NEMS MICROPHONE DESIGN

Nanowire microphones exploit piezo-resistivity to capture acoustic vibrations. They represent the latest innovation and the latest generation of piezoresistive sensors already developed at CEA-Leti. The advantage of this M&NEMS sensor is the use of silicon nanowires to achieve electrical response. Like other M&NEMS sensors, the nanowire microphone integrates a mechanical block with moving parts. The design of this mechanical part is carefully established to develop a significant mechanical stress on the silicon nanowires. The fabrication of the M&NEMS sensor is done in the CEA-Leti clean room as described in Fig. 1. The

microphone consists of two stacked wafers as shown in Fig. 2. The upper wafer has outlet vents. These events form acoustic ducts or guides in which the incident acoustic wave propagates. The lower wafer includes electrical contacts for access to the nanowire resistors, microstructures that put under tension-compression silicon nanowires, and inlet vents. The M&NEMS sensor concept is based on an invention made by the CEA-Leti [19]. In this invention, microphone is a diaphragm enclosed between the two-stacked wafers. The top wafer is used as a lid for M&NEMS fabrication and the bottom wafer is used as a base. To ensure a good sound pressure propagation and a perfect static pressure equalization, acoustic vents must be etched in both wafers. If a sound appears, the microphone works as follow; the pressure actuations propagate through the inlet vents located in the bottom wafer and reach the diaphragm. Then, the pressure actuations deflects proportionally to the pressure difference between inlet and outlet vents located in the top wafer. To design a sophisticated M&NEMS sensor with higher performances, the diaphragms and the acoustic inlet and outlet vents can be multiplied.

On the occurrence of sound pressure at the inlet vents, piezorestive effect allows to vary the silicon nanowire resistance according to the applied stress. The doped crystalline silicon has a piezoresistive effect. Consequently, this effect is commonly used as a detection mechanism in M&NEMS sensors. The integration of piezoresistors into silicon membranes allows to create a piezoresistive effect to detect the acoustic sound pressure by the microphone. Piezoresistors can be integrated into silicon membranes by the method of selective deposition of doped silicon layer. In addition, they can be integrated by the method of selective doping of silicon membrane in diffusion or in implantation process [20]. As the applied stress is distributed over the whole membrane surface, therefore, the optimization of the sensor takes into account to maximize the inside piezoresistors stress. Piezoresistors must be placed in the maximal stress regions [21]. In addition, the microphone membrane thickness and the piezoresistors thickness must have a high ratio [22]. Therefore, maximal stress named tensional longitudinal stress occurs in the middle point of the membrane edge and another maximal stress named compressional stress occurs in the center of the membrane.

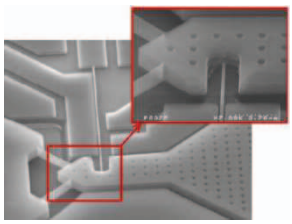

Fig. 1. SEM image of M&NEMS nanowire sensor.

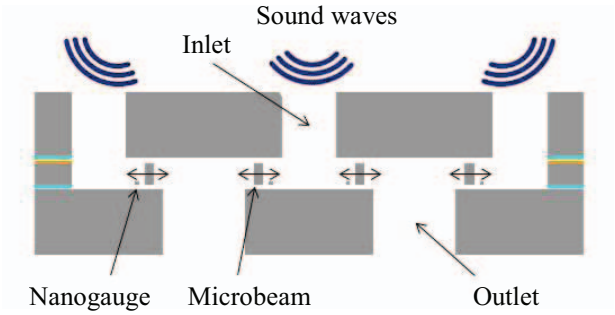

Fig. 2. Microphone cross-section with sensing elements and acoustic configuration.

The suspended silicon nanowires are used to design the piezoresistive sensor. They are served as a piezoresistors to detect the acoustic sound pressure. The p-type silicon nanowires piezoresistive effect has been studied [23]. The piezoresistive effect significantly increases at nanoscale compared with bulk silicon. Therefore, the silicon nanowires are very effective for more efficient MEMS sensors. The overall dimension of the M&NEMS sensor has 1.5 x 1.5 x 0.6 mm^3. The sensor is composed by four micro beams placed between the inlet and the outlet vents. Each micro beam moves rotationally in plane of a silicon wafer according to the applied stress.

III. ΔΣ MODULATOR IMPLEMENTATION

Two topologies are used to implement the ΔΣ modulator namely the distributed feedforward topology or the distributed feedback topology. The loop filter of the feedback topology has the input signal component. Therefore, this input signal component generates large swings into the integrator. As a result, a high linearity is required for the amplifier. In low-voltage design, this problem is very difficult because the drain-source saturation voltage and the threshold voltage are unable to follow the same rate of the external supply voltage. On the other hand, the feedforward topology has a different behavior [24]. There is only the shaped quantization noise in the loop filter input. This advantage is realized by the direct feeding of the input signal and the integrators outputs to the quantizer. Moreover, the input of the first integrator is feeding back by the quantizer output.

The internal voltage swings of integrators are reduced if the input signal component does not exist. Therefore, the amplifier linearity and slew rate are both increased and the current consumption is decreased. Therefore, the feedforward topology becomes a well solution for the low-power and low-noise modulator. The modulator uses a single-bit quantizer for quantification. Due to the inherent linearity of the single-bit quantizer, the DAC does not need dynamic element matching circuit. The modulator integrates two DAC and one comparator. Therefore, its area is reduced. In the other hand, the quantization noise requirement allows to determine the oversampling ratio (OSR) as well as the modulator order. In order to decrease the power consumption of the amplifiers, the dominant component is the modulator thermal noise.

For the non-dominant quantization noise, it can be fixed under the total noise modulator by 10-dB. For the order of the modulator, a topology of fourth-order integrator is selected. As far as, an OSR of 64 is fixed. The modulator has a sampling frequency of 3.072-MHz and an audio signal bandwidth of 20-kHz. Due to the insensitivity of the non-return-to-zero (NRZ) pulse circuit to the clock jitter effect, the DAC in the feedback circuit is a NRZ pulse [25]. In addition, during the full clock period, the feedback pulse

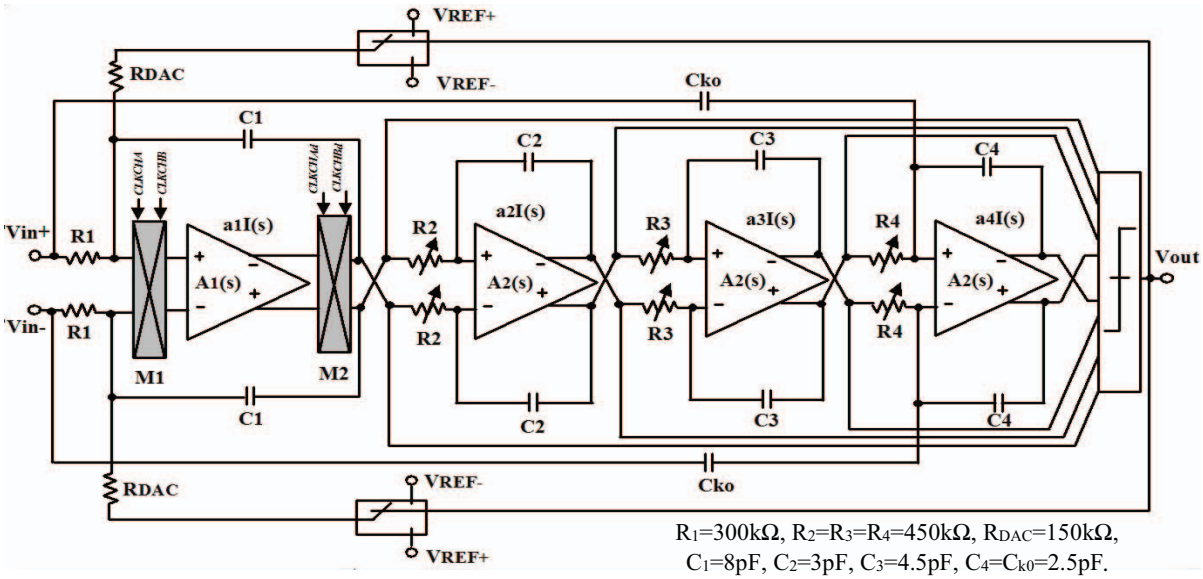

Fig. 3. Circuit diagram of the CT ΔΣ modulator.

remains constant. As a result, the NRZ pulse relaxes the first integrator slew rate requirement. Therefore, the amplifier power consumption is drastically decreased. The fourth-order CT ΔΣ modulator was designed with a standard 65-nm CMOS process with a supply voltage of 1.2-V. The circuit block diagram is shown in Fig. 3. Each integrator is realized by integrating a fully differential OTA with an active-RC filter. If the active-RC filter is placed in a closed-loop circuit, then it ensures several advantages like a good linearity and a parasitic insensitivity. Moreover, the active-RC filter virtual ground ensures relaxation of the amplifier input range constraint. As a result, the closed loop active-RC filter is suitable when operating in low-voltage level.

IV. Delay-time Chopper Stabilization Technique

The most critical stage of the CT ΔΣ modulator is its input integrator. The loop filter do not shape the non-idealities of the first integrator. Therefore, the performance of the modulator is directly affected. Some components generate noise sources at the modulator input, which they are the amplifier, the input resistor R_1 and the R_{DAC} resistors, as shown in Fig. 4. The equivalent input-referred noise of the CT ΔΣ modulator can be written as [26]

$$\overline{v_{in}^2} = 2.\left(\overline{v_{n,R_1}^2} + \overline{v_{n,R_{DAC}}^2}\frac{R_1^2}{R_{DAC}^2}\right) + \overline{i_{in,OTA}^2}R_1^2 + \overline{v_{n,OTA}^2}\left(1+\frac{R_1}{R_{DAC}}\right) \quad (1)$$

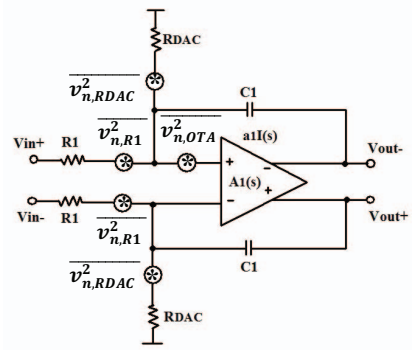

Fig. 4. Equivalent noise modeling of the RC integrator.

R_1 and R_{DAC} depict the modulator dominant noise sources in the objective to reduce its power consumption. If R_1 increases, then the active-RC filter linearity increases too [27]. For the modulator, R_1 is fixed as 300-kΩ and R_{DAC} is fixed as 150-kΩ. The input thermal noise is around 85-dB, which is lower than the full-scale of the input signal. Therefore, the value of the integrated capacitance of the first integrator C_1 is 8-pF. To reduce the input-equivalent noise of the first integrator, we propose to use the well-known technique as the Chopper Stabilization (CHS).

The traditional CHS technique is explained in [28][29]. The signal path mismatch and the demodulated current spikes generate a residual offset V_{os}. Therefore, an AC current spike is caused by the mismatch between the capacitances due to clock feed-through at the Chopper clocks transition moments. The first modulator M1 rectify this AC current. Therefore, a DC spike current appears at its input. As a result, the resulting DC spike current has an average value I_{offset} of

$$I_{offset} = 2\left(\Delta C_1 - \Delta C_2\right)V_{clk}f_{CH} \quad (2)$$

where ΔC_1 and ΔC_2 denote the CHS mismatch parasitic capacitance, V_{clk} denotes the clock signal magnitude and f_{CH} denotes the Chopping clock frequency, with f_{CH} = 6-kHz. The Chopper series impedance and the input signal source are went through by this noise current. Therefore, it depicts as an input voltage spike. The residual offset V_{os} resulting from the spike average DC value can be written as

$$V_{os} = 2R\left(\Delta C_1 - \Delta C_2\right)V_{clk}f_{CH} \quad (3)$$

Where R denotes the equivalent input impedance. Therefore, a residual offset V_{os} depicts the spike average DC value. Moreover, a spike voltage V_{os} is created in the input of the modulator M1. This spike voltage causes a low-frequency interference. To cancel-out this interference, the solution is to create a proper delay between the modulators M1 and M2. The proposed first integrator delay-time CHS technique is shown in Fig. 5. The first integrator is located between two modulating clock signals m1(t) and m2(t) with period T. Moreover, we introduce a delay Δt between the two clock

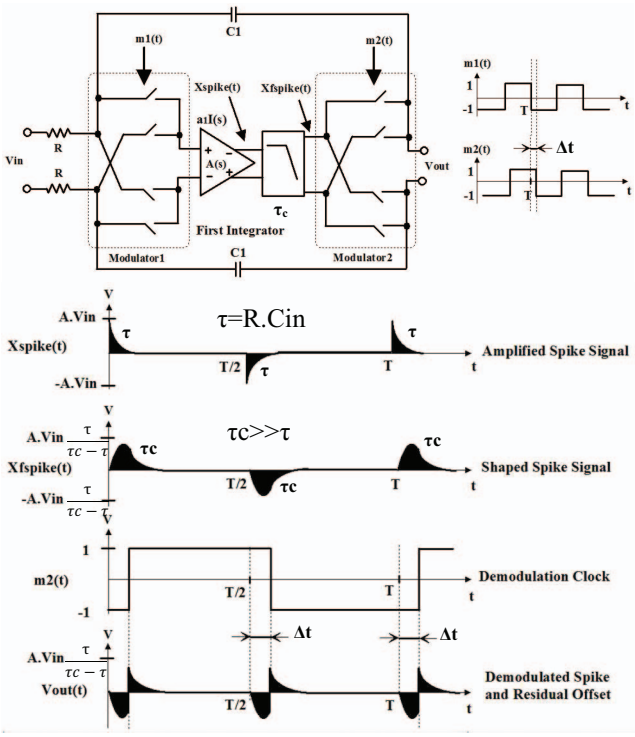

Fig. 5. Chopper stabilization clock feed-through circuit.

signals m1(t) and m2(t) at the same time. Due to the introduction of the delay Δt, this technique causes a chopping of the spike signal itself. As a result, the dc content of the output signal Vout(t) is minimized. The residual output dc offset is completely cancelled if an optimum delay value Δt_{opt} exists, which can be written as

$$\Delta t_{opt} = \ln(2) \times \tau \tag{4}$$

where $\tau = R \times C_{in}$ with R and C_{in} denotes respectively the input resistance and the amplifier's input capacitance.

The major weakness of this technique is the τ itself, which not only depends on the sensor's source resistance R, but also on the amplifier's input capacitance C_{in}. The input modulator's spike signal is amplified and then multiplied with m2(t) in the demodulator. The resulting output signal Vout(t) then contains, apart from higher order harmonics of the chopping frequency, a dc part or residual offset, which is due to chopping artifacts. To solve this problem, shaping of the spike can be introduced by the addition of a first order low-pass filter with time constant τ_c after the amplifier. We must have $T >> \tau_c >> \tau$ with T is the period of the square wave signal m1(t). The shape of the time response of the filtered spike is primarily determined by τ_c and independent of the impedance of the connected sensor. Since the output offset is still linearly dependent on τ, the optimization of Δt_{opt} has been done in such a way that offset reduction is most effective for a worst-case sensor resistance. For our specific implementation $\Delta t_{opt}/\tau_c = 0.8$ has been chosen. The low-pass filter in the signal path has a cut-off frequency of 40-kHz.

V. Measurement Results

A prototype CT ΔΣ modulator is fabricated in a 65-nm CMOS process with a 1.2-V supply voltage and a 0.4-mm^2 core area. The modulator die microphotograph is shown in

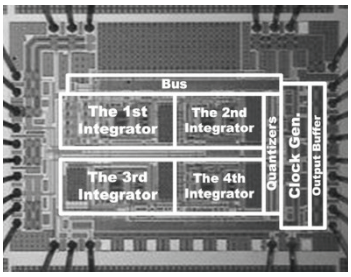

Fig. 6. Chip microphotograph of the fourth-order ΔΣ modulator in CMOS 65 nm technology.

Fig. 6. The method of simultaneous comparison is used to realize the measurement of the M&NEMS microphone as shown in Fig. 7. Some measurement devices are used to perform the test of the chip. A calibrated microphone is used as a reference microphone. It is placed near the tested microphone in the objective to compare their outputs. To isolate external unwanted phenomena, an anechoic chamber is used to perform all measurements. A loudspeaker is placed at a distance of one meter in front of the two microphones. The loudspeaker generates a sound with 1-kHz frequency, which is used as a reference point. In the objective to obtain an equal response of loudspeaker at all frequencies, a corrected EQ curve is used. The output of the M&NEMS microphone as well as the output of the B&K Type 2250 Analyzer are connected to the AP 2700 audio analyzer. An accurate clock with less than 1-ps jitter is provided by a clock generator SRS-CG635. In addition, we have realized a decimator filter on an FPGA to facilitate measurements. The filter has a serial audio interface, which is connected to the AP 2700 audio analyzer. The sound pressure of the loudspeaker is fixed at 94-dB with a frequency of 1-kHz. The B&K analyzer detects the sound pressure level. The 94-dB level corresponds to a 1-Pa acoustic sound pressure level. To obtain constant level, the frequency response is corrected by the EQ curve. Therefore, the reference microphone frequency is fixed at 1-kHz.

Measurement of peak SNR and peak SNDR versus the input signal is depicted in Fig. 8. From the curves, the peak SNR is 103-dB near a -1.4-dBFS input magnitude and the peak SNDR is 102-dB near a -3.4-dBFS input magnitude. In addition, the modulator has a DR of 108-dB at 25 °C. On the other hand, the modulator output spectrum with an input signal of -1.4-dBFS and a frequency of 1-kHz is shown in Fig. 9. It is clear that the CT ΔΣ modulator is stable and it has a good harmonic distortion (HD). The total power consumption measured is 370-μW divided as 300-μW for analog part and 70-μW for digital part. The measurement results of our CT ΔΣ modulator and the comparison with other audio CT ΔΣ modulators is reported in Table. I. The major advantage of our circuit is the modulator was measured with hybrid association with the sensor while all other modulators were measured without sensor. All other modulators have a peak SNR, peak SNDR and DR around or just above 100-dB [30-33]. On the other hand, for the same performances, our modulator reach a value greater than 100-dB. To compare performance of the modulator, it is widely to use the Schreier's figure-of-merit (FOMs) defined as [34]

$$FOMs = DR + 10\log\left(\frac{BW}{Power}\right) \quad (5)$$

Therefore, our modulator achieves a FOMs of 182-dB. As a result, our CT ΔΣ modulator proves a competitive performance compared to the state-of-the art.

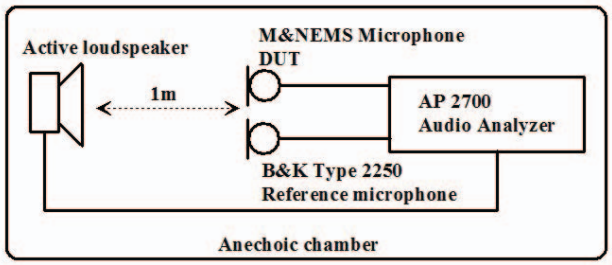

Fig. 7. Measurement setup of the hybrid circuit composed by the M&NEMS microphone and the ΔΣ modulator.

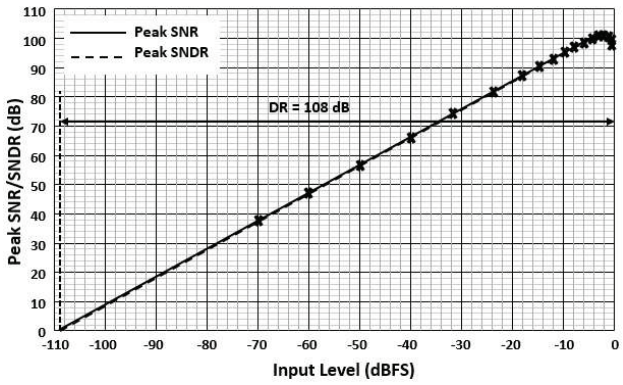

Fig. 8. SNR and SNDR measurements of the ΔΣ modulator.

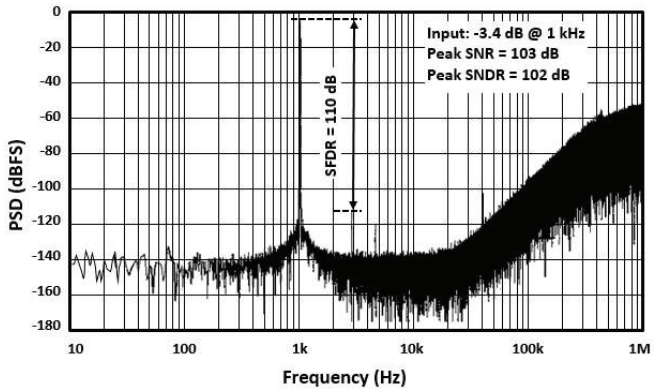

Fig. 9. ΔΣ modulator FFT measurement with a -3.4 dB 1 kHz input.

TABLE I
PERFORMANCES COMPARISON OF THE PROPOSED CT ΔΣ MODULATOR WITH THE STATE-OF-THE ART.

Spec	[30]	[31]	[32]	[33]	**This work**
Power, *mW*	0.8	1.12	0.28	0.01	0.37
Sup, *V*	1	1.8	1.8	1.2	1.2
BW, *Hz*	25k	20k	24k	5k	20k
Peak SNDR, *dB*	95.2	103	98.5	93.5	102
Peak SNR, *dB*	100	106	99.3	94.3	103
FOMs, *dB*	178	181	183	187	182
DR, *dB*	103	109	104	96.5	108
Area, mm^2	0.25	0.16	1	0.05	0.4
Tech, *nm*	65	160	180	40	65

VI. CONCLUSION

In this paper, a low-noise low-power and high sensitive M&NEMS microphone is presented. The resistive accelerometer and the electronic interface are respectively a silicon nanowires and a fourth-order single-bit CT ΔΣ modulator. Several low-noise and low-power techniques are developed at circuit and system levels in order to decrease both the power consumption and the noise and maintain a good performance. The CT ΔΣ modulator is implemented in a 65-nm CMOS technology. The supply voltage is 1.2-V while the power consumption is 370-µW. The core area is 0.4-mm^2. The circuit composed by the M&NEMS accelerometer and the modulator was fabricated and measured. From measurement results over a signal bandwidth of 20-kHz, the peak SNR is 103-dB, the peak SNDR is 102-dB and the DR is 108-dB.

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