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# Evaluation of a Hybrid Bouncer System for High Precision Klystron Modulators

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**Abstract**— In the framework of the development of pulsed klystron modulators for particle accelerators, this paper presents a complete study of a novel hybrid topology of a bouncer circuit used to compensate the voltage droop of the main capacitor bank. This topology allows to merge the advantages of the open loop passive  $L$ - $C$  resonant bouncer topology with an active linear bouncer one. The resulting performances are of great interest for highly repeatable modulators. The solution improves the pulse shape correction made by the passive bouncer alone, leads to a lower sensitivity to parameters deviation and causes a limited level of losses. This paper establishes the merits of such a topology through analytical and numerical studies.

*Klystrons; Pulsed power supplies; High-voltage techniques; Linear particle accelerator; Transfer functions; Circuit optimization.*

## I. INTRODUCTION

Recent advances in the development of linear particle accelerators impose new challenges regarding the design of pulsed power converters. On one hand, pulses quality (i.e. flat-top precision and ripple, stability and pulse repeatability) becomes more and more important because it directly influences the beam acceleration performances. On the other hand, the need for cost-effective and reliable systems often requires a capacitor discharge-based topology connected in series with a *bouncer circuit* in order to perform a pulse shape correction by compensating the capacitor bank voltage droop. In many cases, a bouncer circuit should not generate too much losses in order to keep an acceptable efficiency level for the whole system and to avoid the need of a bulky thermal management equipment. Literature provides us with many examples of bouncer circuits with their own advantages and drawbacks. One can imagine a very basic topology composed of a simple series connected active ballast operated in linear mode. In [1] such a solution has been implemented for magnets pulsed power supplies. Switch-based active bouncers have also been investigated [2]. In [3], the authors propose to merge the advantages of these two techniques by using a hybrid converter where the linear stage aims at compensating the high frequency ripple induced by the interleaved switching converters. Passive bouncer based topologies are also studied in [4...6]: the underlying principle consists in connecting a serial ballast made of a parallel L-C circuit with a low frequency switch. This family of solutions is especially interesting when short pulses are needed because of the active

bouncers' bandwidth limitations. A qualitative comparison of these four solutions is given in TABLE I.

This paper focuses on the study of a hybrid bouncer topology in order to capitalize the key strengths of the passive bouncer and the linear ballast, i.e. an effective droop compensation with the ability to correct short pulses, a good robustness and a reasonable efficiency. Additionally, the proposed solution aims at respecting the very challenging high voltage pulse repeatability (10ppm short-term repeatability) for the Compact Linear Collider requirements [7]. As demonstrated in [8] switching power converters introduce repeatability related issues primarily due to the switches jitter. The Low Level RF Control (LLRF) can compensate for non-repeatable high voltage pulses via feed-back loops. However, LLRF feed-back capabilities depends on the frequency content of the high voltage flat-top. Typically the LLRF control is able to regulate at frequencies of a few kilo Hertz, therefore a switching active bouncer can easily jeopardize the repeatability performance. This is the main reason why a hybrid solution is proposed, where the residual low frequency content on the high voltage flat-top can easily be compensated by the LLRF controls, and thus achieve challenging repeatability specifications.

First of all, a theoretical study is proposed through analytical calculation and numerical simulations in order to establish the merits of the proposed bouncer circuit and to provide with design rules.

## II. THE PRINCIPLE OF OPERATION

### A. Operation of a passive bouncer

A simplified scheme is given on Fig.1. In passive  $L$ - $C$  resonant topologies, the current source  $i_c$  does not exist. A detailed analysis can be found in [4] and similar topologies are studied in [5][6]. The capacitor bank is modeled through  $C_{in}$  and its parallel charger. The main switch  $K1$  aims at starting the pulse by discharging the capacitor bank in the load.

TABLE I. QUALITATIVE COMPARISON OF BOUNCER SOLUTIONS

	Correction	Ripple	Flexibility	Robustness	Eff.
<b>Lin.</b>	++	No	+	+	—
<b>Sw.</b>	+	Yes	++	—	+
<b>Hybrid</b>	+	No	++	—	+
<b>Passive</b>	—	No	—	++	++

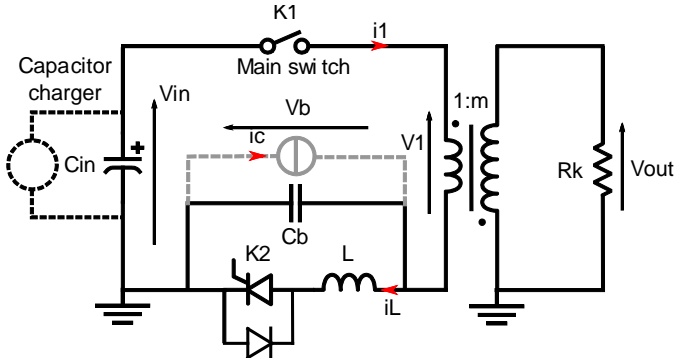


Fig. 1 Modulator with a passive bouncer.

The pulse transformer adapts the voltage level to be compliant with current power electronics component ratings; its typical turn ratio  $m$  can be about tens to hundreds, depending on the application.

The principle is to reach a wisely chosen set of initial condition for  $V_b$  and  $i_L$  at the time  $K1$  is turned-on to generate the pulse. This is achieved by accurately delaying the turn-on of  $K1$  relative to  $K2$ . Hence, the slope of the decreasing  $V_{in}$  is compensated by the slope of the increasing  $V_b$ ; the sum of these voltages is then nearly constant. Nevertheless, as  $V_b$  evolves in a sine curve, the pulse shape compensation is not perfect. With this technique, according to the literature it seems that peak-to-peak error below one percent was not achieved yet, which can be insufficient in specific applications.

### B. Principle of operation with an active linear regulator

The key idea is to add a current source  $i_c$  in order to bring a small compensation to the bouncer voltage  $V_b$ . The value of  $i_c$  is adjusted in real time in order to obtain a perfect ramp-up voltage for  $V_b$  which compensates exactly the  $V_{in}$  ramp-down. This can be achieved with a linear current controlled power supply. However, an analysis based on the passive bouncer waveforms shows that it should be a four-quadrant current source as  $V_b$  and  $i_c$  can be either negative or positive. Therefore, four three-segment switches would be needed, and as the bouncer capacitor is grounded, it would require the use of an external insulated power supply. As shown in Fig. 2, this four-quadrant concern can be turned into a two quadrant one thanks to few modifications in the passive bouncer topology.

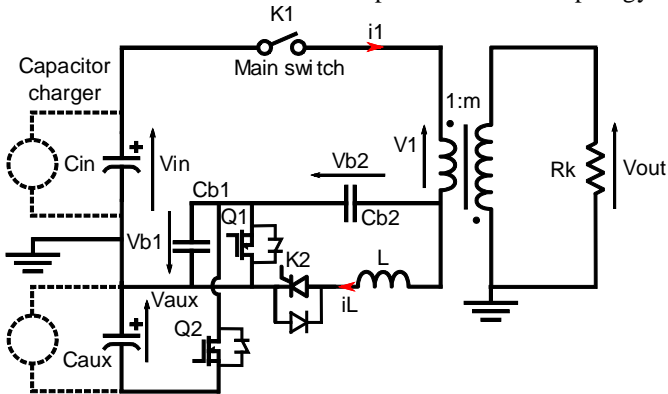


Fig. 2. Proposed topology: modulator with passive bouncer and linear circuit for pulses flat-top compensation.

The bouncer capacitance  $C_b$  is split into  $C_{b1}$  and  $C_{b2}$  and two current sources are made with MOSFETs in order to provide  $C_{b1}$  with a negative or positive current.

The sequence of operation of the bouncer circuit and theoretical waveforms when  $i_c=0$  are given in Fig. 3.  $V_{b1}$  is kept positive thanks to the antiparallel diode of  $Q1$  so a four-quadrant circuit is not needed anymore. The antiparallel diode of  $Q2$  has no effect as far as  $V_{aux} > V_{b1}$  which is typically less than ten percent of  $V_{in}$ . Hence, as  $Q2$  may deal with current in the order of magnitude of  $i_L$ , the auxiliary negative capacitor bank  $C_{aux}$  is designed to store an energy in the order of magnitude of only one percent of the  $C_{in}$ 's energy.

### III. CONTROL STRATEGY AND EXPECTED BEHAVIOUR

#### A. Theoretical analysis

From the circuit of Fig. 1, one can derive the expression of  $V_{out}$  as a function of  $i_c$ ,  $V_{in0}$ ,  $V_{b0}$  and  $i_{L0}$  where,  $V_{in0}$ ,  $V_{b0}$  and  $i_{L0}$  stand respectively for the voltage of  $C_{in}$ , of  $C_b$  and the current of  $L$  when the pulse starts. The two latter parameters are determined by  $t_d$ , the delay between the turn-on of  $K1$  relative to  $K2$ , and the initial bouncer voltage (before  $K2$  is turned on). A linear analysis which takes into account the pulse transformer's magnetic parameters leads to

$$V_{out}(s) = H_1(s)i_c(s) + H_2(s)V_{in0}(s) + H_3(s)V_{b0}(s) + H_4(s)i_{L0}(s), \quad (1)$$

where the  $H_f(s)$  are fifth order transfer functions. For this study it is assumed that the pulse transformer coupling is strong ( $\sigma \ll 1$ ) and that the bouncer's stored energy is much lower than in the main capacitor bank. The three latter terms, i.e. the components values and the initial conditions, are tailored to get a nearly flat pulse although the term  $H_1(s)i_c(s)$  brings the small pulse correction through a closed-loop control of  $i_c$ .

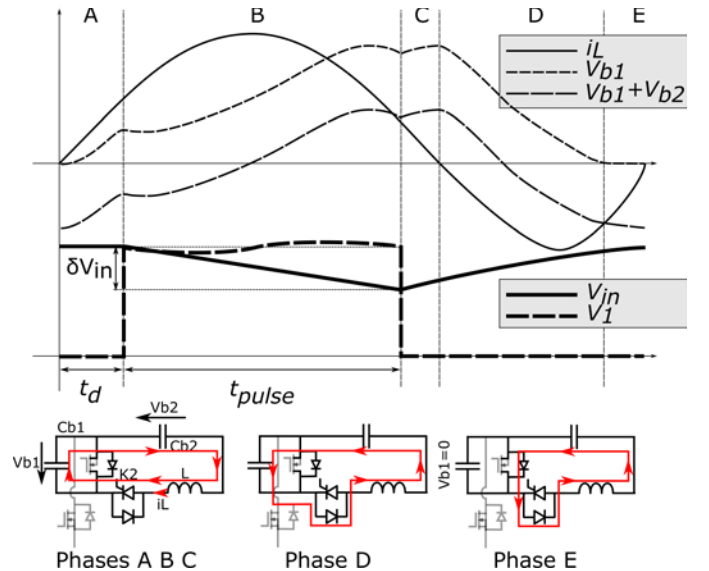


Fig. 3. Theoretical waveforms in the bouncer circuit and sequence of operation when the current-controlled switches are not used.

The bouncer's components values and the set of initial conditions  $\{V_{in0}, V_{b0}, i_{LD}\}$  have been chosen according to a non-linear minimization algorithm of the pulse voltage RMS error given by:

$$Err = (\int (V_{out}(t) - V_{outid}(t))^2 dt)^{1/2} / V_{outid}^{rms} \quad (2)$$

where  $V_{outid}(t)$  stands for the ideal pulse time evolution and  $V_{out}(t)$  stands for the actual pulse when  $i_c=0$ .

### B. Control strategy and design of the compensator

The study of  $H_I(s)$  leads to the Bode plot on Fig.4. It has three zeros at the null frequency, three negative real poles and two stable conjugate complex poles. The compensator must provide a high gain in the pulse bandwidth, which can be very large if a great accuracy is required. However, as shown on Fig.4, two instabilities must be avoided: the low frequency one because the phase curve cuts the  $+180^\circ$  line and the high frequency one because the phase curve cuts the  $-180^\circ$  line. These points can be addressed independently.

#### 1) The low frequency instability

The low frequency compensator  $C_{LF}(s)$  can be made with an integrator plus a low frequency phase lag compensator in order to put the low frequency phase asymptote at  $+180^\circ$  and to provide with a certain amount of phase margin ( $45^\circ$  have been chosen) at the low frequency 0dB point. It should also contain another low frequency zero  $-1/\tau_{LF1}$  in order not to modify the phase at higher frequencies (compensation of the integrator). It leads to:

$$C_{LF}(s) = (1 + \tau_{LF1}s)(1 + \tau_{LF2}s) / [s(1 + a\tau_{LF2}s)], \quad (3)$$

where  $a \approx 5$ .

#### 2) The high frequency instability

It can be addressed by putting a phase lead compensator at high frequency to repel at higher frequency the  $-180^\circ$  phase line cross thus allowing a wider closed-loop bandpass (4).

$$C_{HF}(s) = (1 + a'\tau_{HFS}) / (1 + \tau_{HFS}s), \quad (4)$$

where  $a' \approx 5$  and where  $\tau_{HF} \ll \tau_{LF}$ .

#### 3) Performances prediction

Numerical simulations based on the schematic Fig.2 and the normalized values given in TABLE II have been carried out.

TABLE II. VALUES USED IN THE SIMULATIONS.

Value			Value			Value		
$C_{in}$	10	F	$C_{b1}$	9.42	F	$t_{pulse}$	1	s
$L_{mu}$	148	H	$C_{b2}$	9.42	F	$V_{IN0}$	1.05	V
$\sigma$	0.0004	-	$L$	9.9	mH	$V_{b10}$	36	mV
$m$	1	-	$R_k$	1	$\Omega$	$V_{b10}$	4.3	mV
			$V_{pulse}$	1	V	$i_{LD}$	0.5	A

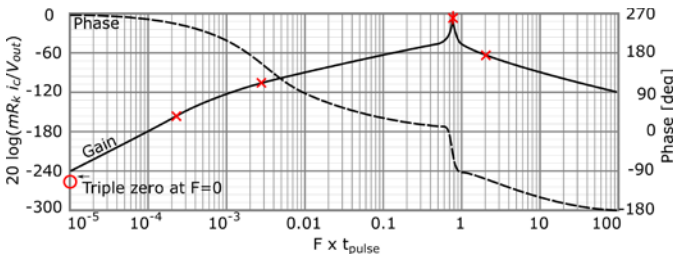


Fig.4. Bode plot of  $H_I(s)$

The values are chosen in order to perform a one-volt one-second pulse in a one-ohm load with a  $m=1$  turn-ratio pulse transformer. The conclusions apply in any actual system by scaling the values. The waveforms are plotted on Fig.5. The pulse settling time is excluded in this plot because it is mainly dependent on the pulse transformer's leakage inductance thus it cannot be improved with the bouncer circuit. As discussed, the linear converter compensation current ( $i_{comp}$ ) can be either negative or positive whereas  $V_{b1}$  is always positive. In this example, its value can reach 80% of the total pulse current but the linear converter voltage droop is limited to only a few percent of the pulse voltage. Calculations based on these simulated waveforms show that the pulse RMS error given by (2) is of 1300ppm. In this calculation, the lower bound of the integral of (2) is such that the pulse has reached 99% of the reference voltage for the first time in order to exclude the pulse settling time from the calculation. Losses estimation depends on the choice of  $V_{aux}$ , the auxiliary power supply voltage. Assuming that  $V_{aux}=0.05V_{in}$  we calculate that the energy lost in the linear circuit is 0.74% of the total pulse energy.

Nevertheless, by its principle, the linear converter losses value is highly sensitive to the needed compensation current  $i_{comp}$ ; thus to the components values. Actually, components values are uncertain and may vary in time and with temperature. When no linear stage is used, this results in an increased flat-top error. When a linear stage is used, the flat-top error should not change a lot but losses should increase since the compensation current becomes higher. For this reason, a sensitivity analysis is performed through a Monte Carlo simulation where  $C_{in}$  and the bouncer components values are randomly chosen in a  $\pm 10\%$  range from the values given in TABLE II. 500 randomly chosen sets of parameters have been simulated; the results are plotted in Fig. 6.

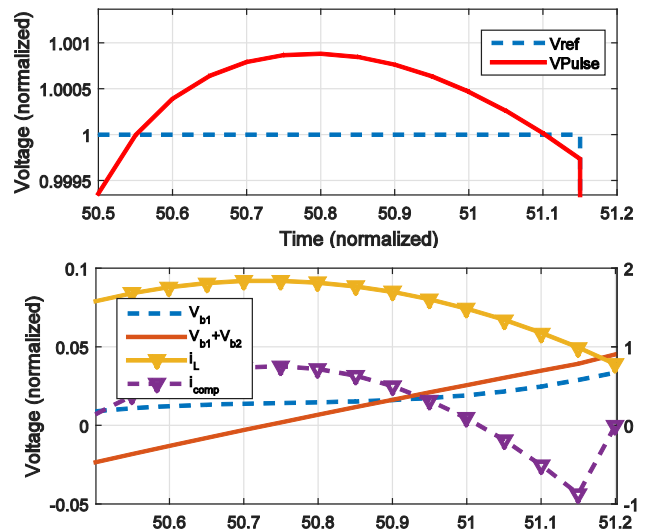


Fig.5. Simulation waveforms (normalized). Pulse voltage flat-top (top). Bouncer's voltages and current (bottom)

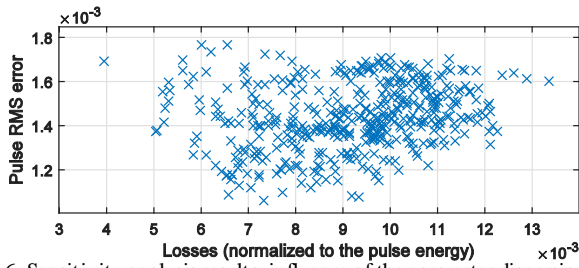


Fig.6. Sensitivity analysis results: influence of the parameter dispersion on losses and flat-top error

The losses axis stands for the energy lost in the linear ballast during one pulse, relative to the pulse energy. It is below 1.4%. This value should be compared to the case when only a serial linear circuit is used; a simple calculation based on the values given in TABLE II shows that it would lead to a value above 5% of the pulse energy. The relative RMS error remains below 1800ppm and may be improved by optimizing the control strategy. The same Monte Carlo simulation performed with the same setup but without the linear converter led to a flat-top RMS error of 9000ppm.

#### IV. CONCLUSION

The topology presented in this work allows to merge the advantages of two commonly used pulse shape compensation techniques: the passive  $L$ - $C$  bouncer and the linear ballast. The pulse voltage compensation is mainly accomplished with the resonance of the passive bouncer circuit and the additional linear circuit brings the small voltage compensation needed to turn the bouncer's voltage sine curve into an ideal ramp up one which exactly compensates the ramp down of the main capacitor bank voltage. The energy lost in the ballast is typically less than one percent of the pulse energy which do

not seriously impacts the whole efficiency of the modulator. In addition, this work showed that the closed loop operation of the linear circuit strongly reduces the sensitivity of the pulse flat-top error relatively to the components values at the cost of increased losses. This increases the versatility of use especially when the converters' bouncer circuits cannot be tailored individually.

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