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# Spectral Coexistence of LDACS and DME: Analysis via Hardware Software Co-Design in Presence of Real Channels and RF Impairments

Niharika Agrawal, S. J. Darak and Faouzi Bader

**Abstract**—To meet the exponentially increasing air traffic, *L*-band (960-1164 MHz) digital aeronautical communication system (LDACS) has been introduced. The LDACS aims to exploit the vacant spectrum between incumbent Distance Measuring Equipment (DME) signals and envisioned to follow an orthogonal frequency division multiplexing (OFDM) approach to support high-speed delay-sensitive multimedia services. This paper deals with the design and implementation of end-to-end LDACS the transceiver on the Zynq System on Chip platform, consisting of FPGA as programmable logic (PL) and ARM as processing system (PS). We consider OFDM based LDACS and improve it further using windowing and/or filtering. We propose a hardware-software co-design approach and analyze various transceiver configurations by dividing it into PL and PS. We demonstrate the flexibility offered by such a co-design approach to choose the configuration as well as word-length for a given area, delay and power constraints. The transceiver is also integrated with the programmable analog front-end to validate its functionality in the presence of various RF impairments and wireless channels and interference specific to the LDACS environment. Via in-depth performance analysis concerning parameters such as out-of-band attenuation, DME interference, bit-error-rate, word-length, and complexity, we demonstrate wide bandwidth filtered OFDM as an attractive solution for the next generation LDACS.

**Index Terms**—LDACS, Filtered OFDM, system-on-chip, analog front end, hardware-software co-design.

## I. INTRODUCTION

International Civil Aviation Organization (ICAO) envisioned the need for Future Communication Infrastructure (FCI) for aeronautical systems to support exponentially increasing air traffic and enable a wide range of services from voice data to multimedia [1–3]. The FCI is expected to be deployed in communications, navigation, and surveillance (CNS) applications as well. Research projects such as Next Generation Air Transportation System (NextGen) and Single European Sky air traffic management (ATM) Research (SESAR) [3] have been given the mandate to propose and demonstrate the FCI prototype. As shown in Fig. 1, FCI comprises several data links such as air-to-ground communication (A2GC), air-to-air communication, ground-to-ground communication, satellite-ground communication, and vice-versa. The A2GC link enables two-way communication between aircrafts and ground terminal, and it is the most critical data link in the

FCI. The ICAO standardization committee has proposed to switch the A2GC link from the narrow band (118-137 MHz) to wider *L*-band (960-1164 MHz), and the corresponding system is referred to as *L*-band digital aeronautical communications system (LDACS).

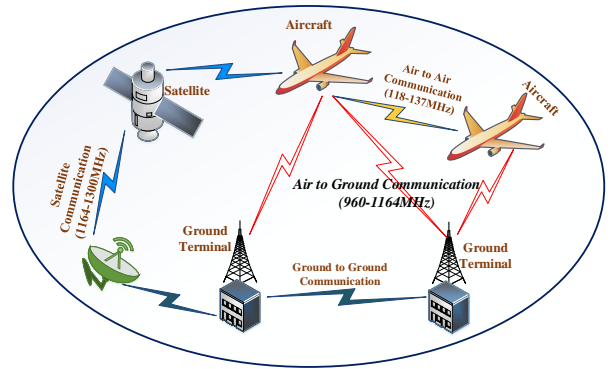


Fig. 1. Various communication links in the future communication infrastructure (FCI).

The *L*-band spectrum allocation, shown in Fig. 2, indicates that it has been occupied by various incumbent users such as distance measuring equipment (DME), Multi-functional Information Distribution System (MIDS), Joint Tactical Information Distribution System (JTIDS), Universal Access Transceiver (UAT), Secondary Surveillance Radar (SSR)/Airborne Collision Avoidance System (ACAS), etc. Based on various spectrum measurement studies, ICAO has identified multiple 1 MHz vacant bands between adjacent DME signals for LDACS. To exploit these bands for the A2GC link, ICAO proposed preliminary LDACS transceiver specifications based on orthogonal frequency division multiplexing (OFDM) transceivers. The OFDM has advantages such as low complexity, simple channel equalization, and multi-antenna support. However, the drawbacks such as large out-of-band emission (OOBE), limited flexibility, and stringent synchronization requirements limit the LDACS transmission bandwidth to at

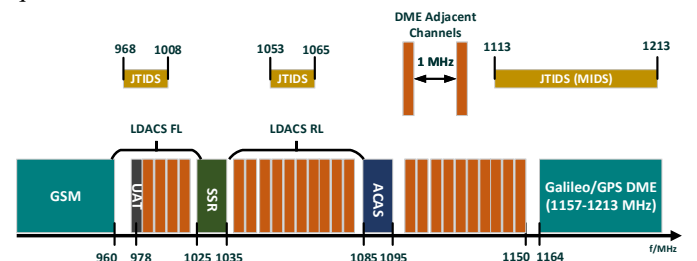


Fig. 2. Various incumbent users and spectrum occupancy in *L*-band.

Niharika Agrawal, and S. J. Darak are with the Department of ECE, IIIT-Delhi, India. E-mail: {niharika, sumit}@iiitd.ac.in.

Faouzi Bader is with the SCEE/IETR - CentraleSupélec, campus of Rennes, France and ISEP - Institut Supérieur d'Electronique de Paris, France. E-mail: faouzi.bader@isep.fr.

most 498 kHz (less than 50% spectrum utilization) due to significant interference to incumbent DME signals. Thus, ICAO expects further research on various windowing and filtering techniques to improve spectrum utilization and feasibility of OFDM based LDACS in complex channel environments encountered in the A2GC link during multiple stages of flight [4, 5]. From the architecture perspective, most of the LDACS transceivers are analyzed via simulations, and their performance analysis on fixed-point hardware in the presence of various RF impairments and wireless channels/interference has not been done yet.

The main objective of the proposed work is to design and implement end-to-end LDACS transceiver on heterogeneous Zynq System on Chip (ZSoC) platform, consisting of FPGA as PL and Advanced RISC Machines (ARM) as PS. We also provide detailed performance analysis for the parameters such as windowing, filtering, OOB, DME interference, bit-error-rate (BER), word-length, area, delay, and power. The contributions of the paper can be summarized as:

- 1) We design and implement fixed-point OFDM based LDACS and analyze the effect of windowing and/or filtering approaches. Based on the analysis, we suggest enhancements to existing LDACS specifications to improve spectrum efficiency.
- 2) Since each transceiver block can be realized on PS as well as PL; we provide the architecture for efficient sequential execution on PS and efficient parallel execution on the PL.
- 3) We propose a novel hardware-software co-design approach and implement various transceiver configurations by dividing it into PL and PS. We demonstrate the flexibility offered by such a co-design approach to choose the configuration, pipelining, and word-length for a given OOB, BER, area, delay, and power constraints.
- 4) In the end, various configurations are integrated with programmable analog front-end (AFE) to validate the transceiver functionality in the presence of various RF impairments and wireless channels/interference specific to the LDACS environment.

The first three contributions are a significant extension of our work in [6]. In this paper, we design and implement four more transceiver configurations than [6]. The performance analysis presented here is detailed as we consider the effect of word-length, pipelining, LDACS specific channels, DME interference as compared to only power spectral density in [6]. Furthermore, we integrate the proposed transceiver with programmable AFE and analyze the effects of RF impairments.

The remaining paper is organized as follows. Section II describes the work done previously in this area. Hardware-Software requirements for the transceiver models are discussed in section III. In section IV and V, the transceiver architecture followed by its variants implementation using hardware-software co-design on ZSoC along with pipelining and AD9361 integration are presented. Experimental results are analyzed in section VI. Section VII concludes the paper.

## II. LITERATURE REVIEW

Various works dealing with the performance analysis and feasibility of OFDM based LDACS transceivers for a wide range of CNS applications are discussed in [7–9]. In this section, we focus on the design, implementation, and validation of the LDACS transceiver as well as potential alternatives to improve its performance.

The implementation of various blocks in the conventional OFDM based LDACS on homogeneous platforms such as field-programmable gate arrays (FPGA) or application-specific integrated circuits (ASIC) have been discussed in [10–15]. The primary focus of these works was strictly on the synchronization and channel estimation techniques for the LDACS environment. In [10], a novel correlation-based synchronization approach for large carrier frequency offsets is proposed, and its implementation on the FPGA has shown to consume lower area and power without compromising on the BER performance [11]. In [12], partial reconfiguration capability of the FPGA is used to design a flexible LDACS transceiver. It offers a significant improvement in the area and power consumption, but provided gains cannot be extended for implementation on the ASIC. In [13], a novel sensing method for sensing the active LDACS transmissions via a multiplier-less correlation-based approach is proposed. It offers improved performance, especially at a low signal-to-noise ratio (SNR), and lowers power consumption than other architectures. On the receiver side, reconfigurable low complexity filter and filter bank architectures for channelization and spectrum sensing have been proposed in [14, 15]. Such architectures are based on a frequency response masking approach, and they enable LDACS ground stations to receive and/or sense single as well as multiple frequency bands simultaneously. The major drawback of these works is that they do not consider end-to-end transceiver design.

The homogeneous platforms have limitations of flexibility and scalability and may not be suitable for various real-time decision-making tasks. Hence, recently heterogeneous platforms consisting of processors and hardware such as FPGA or ASIC on a single chip are being explored. One such platform is ZSoC consisting of ARM and FPGA on a single chip, and it is being envisioned for various wireless communication applications [16–18] as well as autonomous driving, medical applications. For example, a Cognitive Radio Accelerated with Software and Hardware (CRASH) is introduced in [19] and authors analyzed three possible configurations of spectrum sensing and decision-making blocks: 1) Both blocks on the FPGA, 2) Both blocks on the processor and 3) Spectrum sensing on the FPGA and decision making on processor. Their experiments show that the third approach offers superior performance over the others. Similarly, cognitive radio exploiting the partial reconfiguration capability of the FPGA and decision-making capability of ARM is demonstrated in [20]. Precisely, the processor controls the functionality of the FPGA based on real-time network and spectrum status and allows dynamic switching between channelization and spectrum sensing blocks. Similarly, the hardware-software co-design approach for the IEEE 802.11a transceiver system is

discussed in [21, 22]. However, such study and analysis have not been done yet for LDACS transceivers.

Various alternatives have been discussed to improve the OOB performance of the OFDM based LDACS. In [23], filter bank multi-carrier (FBMC) based LDACS transceiver is presented, which offers better OOB performance and hence, higher vacant spectrum utilization than OFDM. However, the need of sub-carrier filtering at the transmitter and receiver significantly increases the complexity of the FBMC. Since the architecture of FBMC is significantly different from that of OFDM, the single transceiver cannot support both waveforms on a single chip unless they are stacked in parallel. Furthermore, the extension of FBMC for a multi-antenna transceiver system, a default configuration offering high data rates and superior performance in challenging environmental conditions, is difficult. Generalized Frequency Division Multiplexing (GFDM) [24] is another alternative to OFDM, but it has not been analyzed for LDACS yet. Furthermore, due to concern regarding the area and power consumption of the transceiver, ICAO prefers windowing and filtering approaches to improve OOB performance of the OFDM based LDACS [9]. In [25], we proposed a reconfigurable filtered OFDM (ReF-OFDM) using a reconfigurable linear phase digital filter. Proposed architecture offers better OOB performance than OFDM and GFDM as well as enables dynamical switch between various transmission bandwidths using a single prototype filter. Also, it has a lower complexity than FBMC and GFDM, making it an attractive solution for next-generation LDACS.

This paper deals in detail with the efficient hardware realization of end-to-end LDACS transceiver on the heterogeneous platform and such work has not been discussed yet in the literature. Furthermore, existing works lack in-depth analysis of the effect of windowing and filtering on the performance of LDACS in the presence of various RF impairments, realistic LDACS channels, and DME interference. The proposed work aims to overcome these drawbacks, thereby contributing to ICAO LDACS standardization activities.

### III. TRANSCIEVER ARCHITECTURE

In this section, we present the detailed architecture of the proposed transceiver and extensions via windowing and filtering. We also discuss the design of AFE along with various LDACS specific channels as well as interference. The detailed block diagram of the transceiver is shown in Fig. 3.

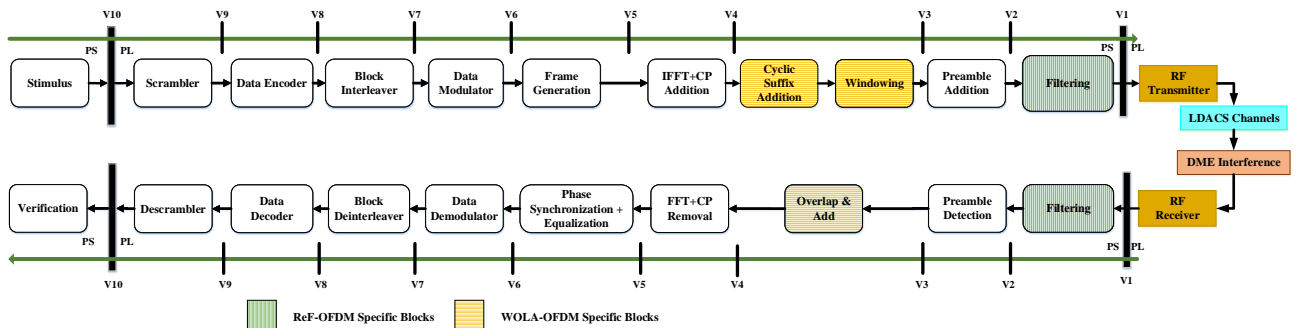


Fig. 3. Block diagram showing different configurations of the LDACS transceiver along with windowing and filtering blocks.

#### A. Stimulus and Verification Blocks

The stimulus block at the transmitter reads the input data bits to be transmitted. They are either stored on on-board ZSoC memory or they can be transmitted from the laptop over Ethernet (ENET). For illustration, we consider the total 864 data bits divided into 36 distinct frames of 24 bits each. Frame formation is done using simple counters and multiplexers. The verification block receives the frame and reads the corresponding data bits for subsequent performance analysis. Both blocks are implemented on the PS.

#### B. Digital Baseband Processing Blocks of Transceiver

Various baseband signal processing blocks of the transceiver are shown in Fig. 3. The blocks such as scrambler, inter-leaver, data encoder, data modulator, frame generation, IFFT followed by CP addition, and preamble addition are desired signal processing blocks for the OFDM transmitter. The receiver consists of similar blocks that perform the operations in the reverse direction. The OOB performance of the transceiver can be improved further using windowing or filtering or both. For windowing operation, two new blocks, 1) Cyclic suffix addition, and 2) Windowing, are added before preamble addition. Similarly, at the receiver, we need overlap and add block. For filtering operation, new filtering blocks are added at the transmitter as well as the receiver. The detailed explanation of various blocks in Fig. 3 is given later in III-B1.

Each transceiver block can be realized on the PS or PL. In Fig. 3, we consider 10 possible configurations,  $V1, V2, \dots, V10$ . Each configuration offers a unique boundary between PS and PL. We discuss these configurations in detail later in Section IV. Here, we focus on the functionality and architecture of each block for the serial implementation on the PS as well as parallel implementation on the PL.

**1) Orthogonal Frequency Division Multiplexing (OFDM):** The OFDM based transmitter consists of blocks such as scrambler, convolutional encoder, interleaver, binary phase-shift keying (BPSK) modulator, Inverse Fast Fourier Transform (IFFT) and cyclic prefix adder. The scrambler does the bitwise XOR operation on the incoming input data and a random scrambling sequence generated by the linear feedback shift register (LFSR). The same sequence is used to descramble the data at the receiver. This is followed by a convolutional encoder which uses the generator polynomial of  $g_0 = 133$  and  $g_1 = 171$ . These correspond to a rate 1/2

code with a maximum free distance of 7. Thus, the output of the convolution encoder is twice the length of the input. The interleaver performs two-step permutation on coded data and used to handle burst errors. The interleaved data is then converted to complex samples using the BPSK modulator to obtain 48 samples. Note that any other modulation scheme such as QPSK, 16 QAM, or 64 QAM can also be used. These samples are then mapped to 64 points IFFT, as shown in Fig. 4. As per the LDACS specifications, 64 subcarriers are used, out of which 50 are active subcarriers carrying data and pilot symbols. The number of subcarriers carrying pilots and data in each symbol is not fixed and depends on the symbol index. For example, the number of data subcarriers in the symbol with index 0 and 1 are 36 and 48, respectively, while the number of pilot subcarriers are 14 and 2, respectively. One LDACS frame comprises 54 symbols, as shown in Fig. 4 and the pilots at each symbol follow specific patterns except symbols with indices 0, 51, 52, and 53. Please refer to [26] for more details on the architecture which performs such a symbol to subcarrier mapping in SoC. **For the simplicity of representation, we discuss the architecture of various blocks of the transceiver assuming the transmission of OFDM symbol with index 1 (or 6, 11, ..., 46) of LDACS frame consisting of 48 data, two pilots, 1 DC, and 13 Null subcarriers. Note that depending on the symbol index, appropriate control signals are generated to meet the symbol mapping requirements of the LDACS frame, as shown in Fig. 4. The corresponding details are omitted to maintain the brevity of paper and avoid repetitive description.** Also, we consider the forward link of LDACS since forward and reverse links differ only in the symbol-to-sub-carrier mapping which is not a challenging task.

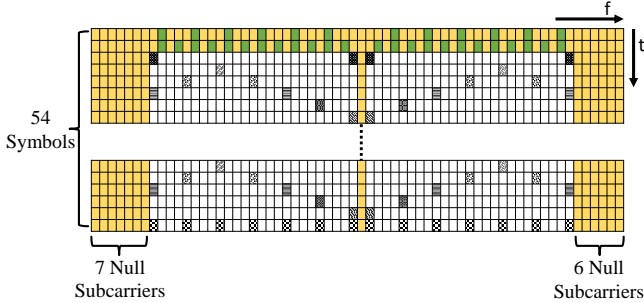


Fig. 4. LDACS frame with 54 symbols and corresponding symbol-to-subcarrier mapping.

To avoid inter-symbol interference, a cyclic prefix (CP) of length 11 is added to the OFDM symbol. In the end, preambles are added, which aim the receiver for synchronization. The preamble consists of both short training sequence (STS) and long training sequence (LTS). The STS is used for timing acquisition, coarse frequency acquisition, and diversity selection, while LTS is used for channel estimation and fine frequency acquisition [7, 8]. For the length of 160 samples, LTS is repeated twice, while STS is repeated ten times. In the end, the signal is transmitted over the wireless channel via AFE and antenna.

The difference in processing modes of PL (Sample mode) and PS (frame mode) leads to a difference in the implementation of each block of the transceiver in the two modes. Due

to limited space constraints, we discuss the architecture of a few blocks here while remaining blocks are discussed in detail in Supplementary [26]. The PS implementation of the CP addition involves only vector concatenation due to frame-based processing. As shown in Fig. 5(a), the last 11 samples of the IFFT output are appended in the beginning as CP. On the other hand, PL implementation of the same involves additional counter and registers to store the samples to be added as CP. As shown in Fig. 5(b), we need two registers of length  $2CP$  (22) and  $N$  (64) along with  $\text{Mod-}N$  counter. For easier understanding, we consider the illustrative example of a frame consisting of 4 samples with 1 CP sample. In this case, we need the first register of size 2 and the second register of size 4. In the first clock cycle, input sample,  $a_0$ , is loaded into the first register, and hence the content of two registers are  $\{a_0, 0\}$  and  $\{0, 0, 0, 0\}$ . At the fifth clock cycle, content of two registers will be  $\{a_4, a_3\}$  and  $\{a_2, a_1, a_0, 0\}$ . In the next clock cycle, frame reset (reset\_in) happens since we have received all samples of a frame, and hence the content of two registers will be  $\{0, a_3\}$  and  $\{a_2, a_1, a_0, 0\}$ . From the next cycle onward, output valid is always 1 and we get the first output which is  $a_3$  from the first register and content of register becomes  $\{b_0, 0\}$  and  $\{a_3, a_2, a_1, a_0\}$ . Here,  $b_0$  is the first sample of a new frame. Subsequently, the next four outputs are taken from the second registers. In this way, we get the output as  $a_3, a_0, a_1, a_2, a_3$ . Similarly, in next four clock cycles, the output will be  $b_3, b_0, b_1, b_2, b_3$ . As discussed before, valid and reset signals are used to synchronize the transfer of data between any two adjacent blocks and needs to be handled carefully in each block. For instance, as shown in Fig. 5(b), a valid signal involves 22 and 64 tapped delays, similar to the ones used in the data signal.

2) **WOLA-OFDM**: In WOLA-OFDM, the conventional rectangular window is replaced by a windowing pulse with

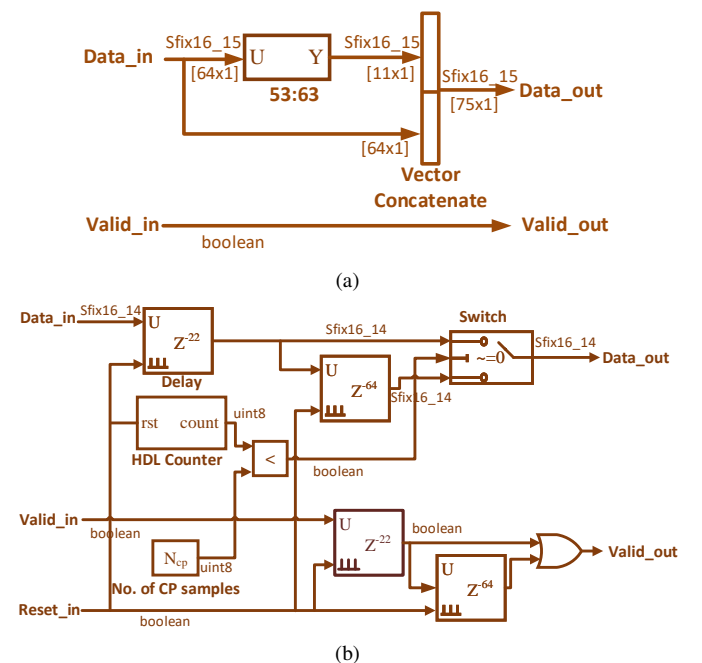


Fig. 5. (a) PS and (b) PL implementations of OFDM cyclic prefix addition.



soft edges to improve the out-of-band emission of CP-OFDM [27]. This soft edge windowing is applied in the time domain via point-to-point multiplication between the output of the CP block and window function. The additional sequence of operations at the transmitter are as follows:

- 1) **Cyclic Extension:** The CP addition is slightly different in WOLA-OFDM than CP-OFDM. As shown in Fig. 6, the CP is formed by appending the last  $CP + W$  samples of a given symbol (output of IFFT) to its beginning, and the cyclic suffix (CS) is formed by appending the first  $W$  samples of a given symbol in its end. Therefore, the length of the WOLA-OFDM time domain symbol is extended from  $N$  to  $N + CP + 2W$ , as shown in Fig. 6.
- 2) **Windowing:** After the cyclic extension, a Root Raised Cosine (RRC) window of length  $L = N + CP + 2W$  is applied in the time domain. For LDACS, we have  $N = 64$ ,  $CP = 11$  and  $W = 8$ , and corresponding window length is  $L = 91$  with the taper region of length  $W$ .

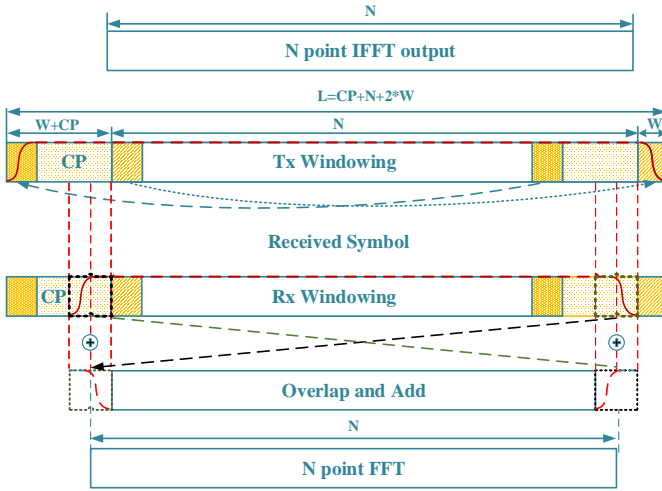


Fig. 6. Cyclic prefix and cyclic suffix processing along with windowing for WOLA-OFDM.

Such windowing at the transmitter demands additional signal processing at the receiver to suppress the asynchronous inter-user interference. As shown in Fig. 6, the additional steps at the receiver are as follows:

- 1) **The starting and ending samples of length  $W + \lfloor \frac{CP}{2} \rfloor = 13$  and  $W = 8$  respectively are discarded, and the RRC windowing is applied at the retrieved data. The window length at the receiver is not same as the transmitter and the receiver window length is taken as  $N + \lfloor \frac{CP}{2} \rfloor = 70$ .**
- 2) Two adjacent received WOLA-OFDM symbols are overlapped with each other and then added to the next symbol to retrieve the 64 main samples. The overlap and add process is applied to minimize the effects of windowing on the useful data, as shown in Fig. 6.

The PS and PL implementation of windowing is shown in Fig. 7 (a) and Fig. 7 (b), respectively. The PS implementation at the transmitter is straightforward due to a frame-based approach in which a time domain multiplication of the input data with the windowing coefficients is performed, as shown in Fig. 7 (a).

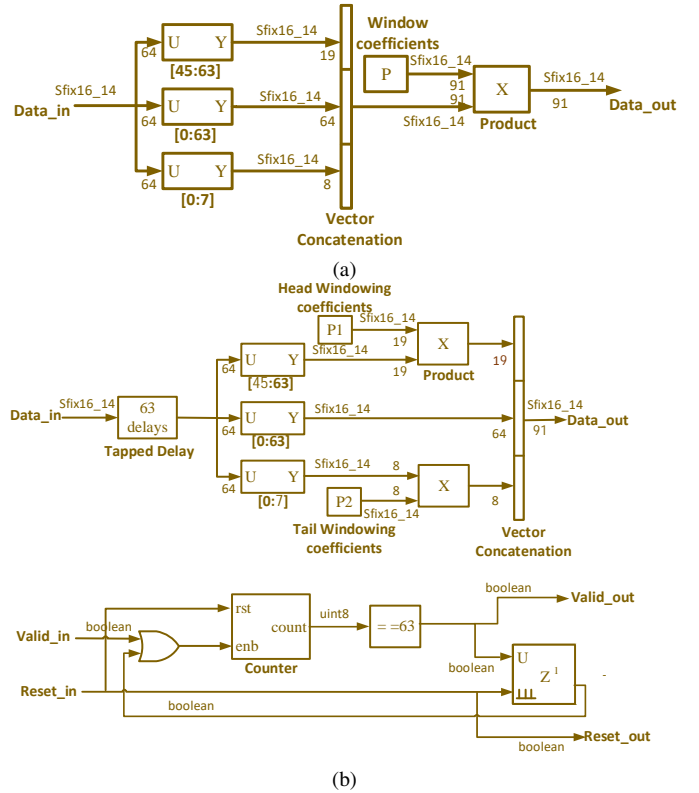


Fig. 7. (a) PS and (b) PL implementation of time-domain windowing.

In PL implementation, the data is coming in the form of samples, therefore to add the cyclic prefix, suffix, and windowing samples, all 64 samples (1 frame) are collected with the help of 63 tapped delays. For PL implementation of windowing, we exploit the parallel operation by dividing the windowing into head and tail sections. Consider  $P1$ , and  $P2$  denote the windowing coefficients for head and tail sections, respectively. The  $P1$  is of length  $W + CP$  in which the first  $W$  samples corresponds to the first  $W$  RRC windowing coefficients ( $P$ ) while remaining samples are fixed to 1. The  $P2$  is of length  $W$ , and it corresponds to the last  $W$  RRC windowing coefficients, ( $P$ ). In the end, the cyclic prefix, cyclic suffix, and the data are concatenated, and total 91 samples are selected for transmission over the air.

The input valid signal increments the counter value, and the counter counts till 63 i.e., a total of 64 samples. Once we have received the whole frame of 64 samples (without adding cyclic prefix and suffix), the output valid signal will become one. The output valid signal is generated for one clock cycle for the output frame of size 91 (similar to the size of the transmitted data (91 samples)).

At the receiver, windowing is implemented in the same manner as the transmitter. Additionally, the **overlap and add processing is performed on the  $N + \lfloor \frac{CP}{2} \rfloor = 70$  windowed samples** by directly extracting the desired samples from the received frame and then concatenate it to the beginning and ending of the symbol. The PS and PL implementation is the same for overlap and add processing, as presented in Fig. 8 (a) and (b).

3) **Filtered OFDM:** The FOFDM uses a linear phase finite impulse response filter instead of time-domain windowing for

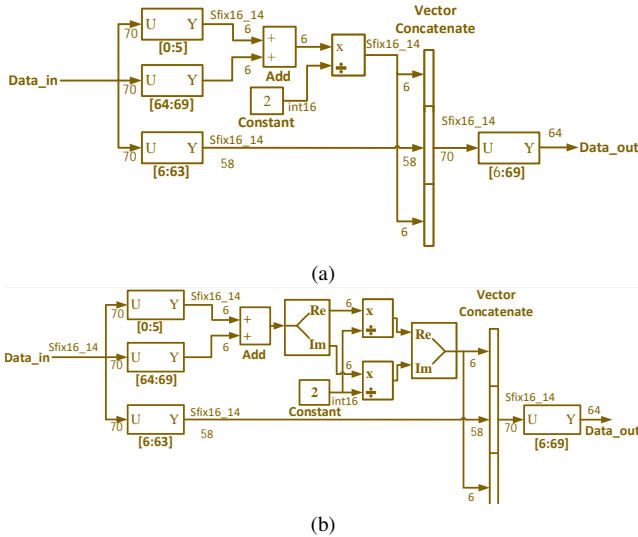


Fig. 8. (a) PS and (b) PL implementation of overlap and add processing.

further improvement in out-of-band emission. In [25], we have shown that FOFDM enables higher transmission bandwidth compared to bandwidth limitation to 498 kHz in the OFDM based LDACS system. It also enables the transmission in non-contiguous bands and the sharing of adjacent frequency bands among asynchronous users. However, the filter needs to be carefully designed and implemented as it may lead to higher inter-symbol and inter-carrier interference. In the proposed FOFDM transceiver, we consider LDACS with 480 kHz of bandwidth with a sampling frequency of 1.1 MHz and hence, we designed a linear phase low-pass filter of order 150 with a normalized cut-off frequency of 0.86 and the transition bandwidth of 0.02 generated using park McClellan approach [28, 29]. The PS and PL implementation of the FIR filter is shown in fig. 9 (a) and 9 (b) respectively.

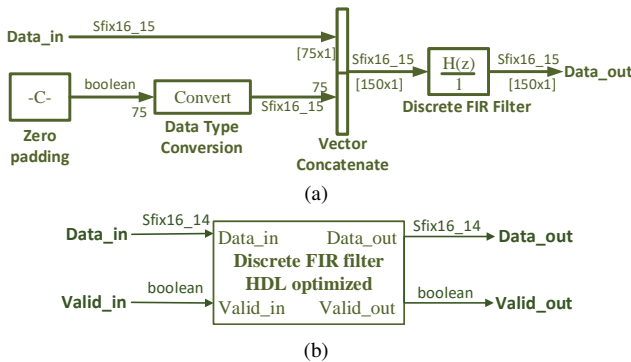


Fig. 9. (a) PS and (b) PL implementation of Filter.

The filter specifications and implementation are identical at the transmitter and receiver. For the implementation of the filter, we have directly used the HDL optimized model provided by Xilinx. In case of PS implementation, we need additional zero-padding to handle delay balancing and selector to choose the desired filtered data. For PL implementation of the filter, we have studied the effect of word-length on the performance of the transceiver. Please refer to Section V for more details.

### C. Analog Front End: RF Transmitter and Receiver

The output of the transmitter is passed to the AFE for over-the-air transmission in  $L$ -band. The AFE is designed using the RF models provided by Analog Devices for use in MATLAB/Simulink. The transmitter consists of Digital up-conversion (DUC) filters, analog filters and RF front-end as shown in Fig. 10. The digital up-conversion filter is a series of digital FIR filters that convert the baseband signal to an intermediate frequency (IF) signal. The sample rate of the DUC filter should be the same as the input signal. The digital filter also introduces the noise floor. The analog filters are used to shape this noise floor and provide a continuous-time signal processed by the RF front-end. The RF front-end up-converts the IF signal to RF carrier frequency using the local oscillator, followed by amplification using a power amplifier.

At the receiver side, the RF front-end down-converts the signal centered on the same LO frequency to IF using a quadrature demodulator, as shown in the Fig. 11. The RF front-end has mainly three components: low noise amplifier (LNA), quadrature demodulator (Mixer), and trans-impedance amplifier (TIA), and the chain is indicated as LMT. The gains of each component are tunable and controlled by the AGC. The analog filters provide a continuous-time signal to the ADC. The ADC models a high-sampling rate third-order delta-sigma modulator. The low-pass digital down conversion filters convert the highly sampled signal at the output of the ADC to the baseband. The output of the AFE is passed to the OFDM receiver in Zynq. The integration of the AFE with the transceiver in Fig. 3 and its parameters as per the LDACS specification are discussed in section V-A.

### D. LDACS Specific Wireless Channels and DME Interference

As shown in Fig. 12, three channels that are specific to the LDACS environment are considered, and they are Airport (APT), Terminal Maneuvering Area (TMA), En-routing (ENR). The channels are modeled as wide sense stationary with uncorrelated scattering and characterized using three properties: fading, delay paths, and Doppler frequency [30]. The channel parameters are given in Table I [30–33]. Note that the Doppler frequency is obtained as  $F_D = F_c \frac{v}{c}$  where  $F_c$  is the carrier frequency and is at most 1215 MHz,  $v$  is the velocity of the aircraft in  $m/s$  (1 Knots True Airspeed (KTAS)=  $0.5144 m/s$ ) and  $c = 3 * 10^8 m/s$ .

Along with these specific LDACS real-time channels, DME interference is also taken into account. DME is measuring equipment used for navigation purposes and has major interference on LDACS as LDACS is deployed between two DME

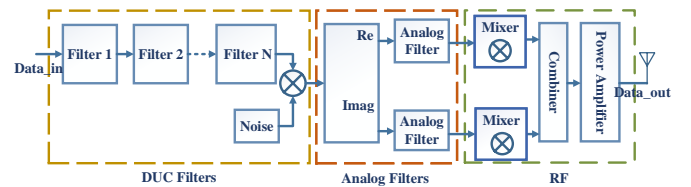


Fig. 10. Analog Front End: RF Transmitter.

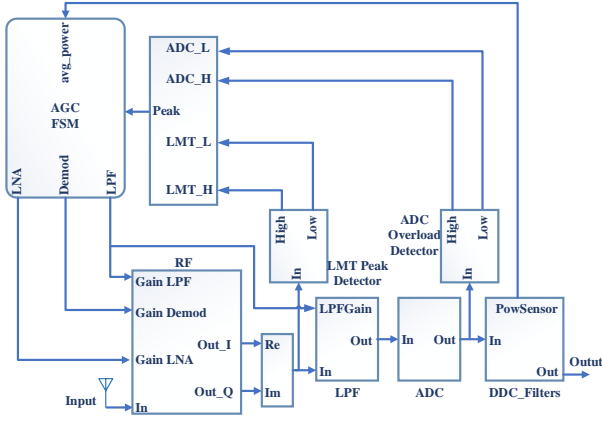


Fig. 11. Analog Front End: RF Receiver.

TABLE I  
CHANNEL PARAMETERS

Scenario	Max Delay ( $\mu s$ )	Acceleration ( $m/s^2$ )	Harmonics	Velocity (KTAS)	Doppler Frequency (Hz)
APT	3	5	8	200	$(1215e6) \frac{200 * 5144}{3e8} = 413$
TMA	20	50	8	300	$(1215e6) \frac{300 * 5144}{3e8} = 624$
ENR	15	50	25	600	$(1215e6) \frac{600 * 5144}{3e8} = 1250$

channels. The DME signal is composed of Gaussian pulse pairs given as:

$$S = e^{-\frac{\alpha t^2}{2}} + e^{-\frac{\alpha(t-\Delta t)^2}{2}} \quad (1)$$

where,  $\Delta t = 12\mu s$  denotes the spacing between the pulses and  $\alpha$  is the pulse width of  $4.5 \times 10^{-11} s^{-2}$ . All the experimental results presented in this paper considers the DME interference. **The DME interference signal is scaled by a factor of 0.2 so that the power level of the DME signal closely matches the LDACS signal.**

### E. Receiver

At the receiver, the preamble detection block detects the beginning of the data frames using auto-correlation and extract it for subsequent processing. For cyclic prefix removal, the starting 11 samples are discarded out of the 75 incoming samples. The remaining 64 samples are given as input to the 64 point FFT block. Out of 64 symbols at the output of the FFT block, 48 data symbols are extracted by a selector. The output data symbols are demodulated using the BPSK demodulator. The deinterleaver then deinterleaves the bits

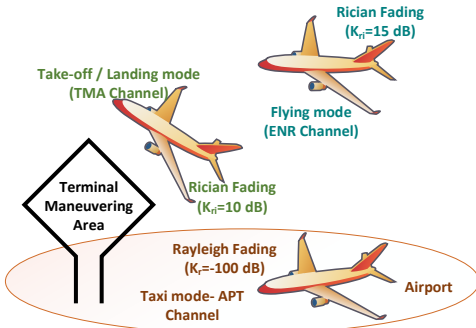


Fig. 12. Various LDACS channels and their parameters for different positions of the aircraft.

using the predefined sequence followed by decoding using a Viterbi decoder using the same generator polynomial as a convolutional encoder in the transmitter. The descrambler uses the corresponding descrambling sequence to retrieve the 24 bits of a frame. A similar process is repeated for each frame. The next section presents the HW-SW co-design approach used for transceiver design and implementation.

## IV. HARDWARE-SOFTWARE CO-DESIGN APPROACH

The HW-SW co-design approach gives the flexibility to choose which part of the transceiver is best suited to be implemented on PL and PS of the ZSoC. In this section, we present design details of various transceiver configurations (V1-V10), shown in Fig. 3 realized using the HW-SW co-design approach. The data transfer between PS and PL plays an important role in this approach, and corresponding details are summarized in Table II. We begin with the configuration

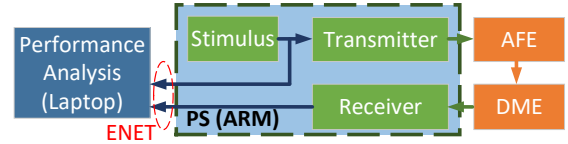


Fig. 13. Configuration V1 of the transceiver.

V1 in which the complete transceiver is implemented on the PS, as shown in Fig. 13, and hence, there is no data transfer between PS to PL as shown in Table II. The stimulus model generates 32-bit unsigned integers out of which 24 are data bits (single frame), 2 are valid and reset signals, and remaining are zero-padded bits. Each data bit is modulated and processed to obtain an OFDM symbol with 75 samples (64 subcarriers + 11 samples as CP). Each sample can be represented in the form of an 8/16/32-bit fixed-point data type. **Each OFDM symbol in a frame comprises 75 samples (64 + 11 CP) and corresponding symbol period is  $75\mu s$  assuming 1 sample takes  $1\mu s$ . We refer this as time per frame symbol (tpfs).** With 36 data frames, 2 pilot frames, and additional delays due to frame synchronizations, one simulation runs for  $43 * tpfs$  duration. The performance analysis model compares the transmitted and received bits for subsequent BER and throughput analysis. The realization of this architecture on ZSoC is done using MATLAB HDL coder and verifier, along with Embedded Coder toolboxes. Please refer to [6, 26] for detailed steps involved in the HW-SW co-design.

TABLE II  
DATA TRANSFER BETWEEN PS AND PL (TRANSMITTER SIDE)

Model Variants	Data Type	Size of 1 element	No. of elements
V1	-	-	-
V2 (FOFDM)	Signed Fixed Point	8/16/32 bits	150
V3	Signed Fixed Point	8/16/32 bits	75
V4 (WOLA-OFDM)	Signed Fixed Point	8/16/32 bits	91
V5	Signed Fixed Point	8/16/32 bits	48
V6	Signed Fixed Point	8/16/32 bits	48
V7	Boolean	1 bit	48
V8	Boolean	1 bit	24
V9	Boolean	1 bit	24
V10	Boolean	1 bit	24

In configuration V2, the filtering operation is moved to PL, and hence, it is applicable only for FOFDM. As shown in Fig. 14, the transmitter and receivers are divided into two sections, one for PS and other for PL. For V2, the output of



transmitter\_1 is the frame consisting of 150 complex filtered OFDM samples, each of which can be represented in 8/16/32-bit fixed-point format. One such frame, along with valid and reset signals are interfaced with AXI-compatible buffer realized in PL. The buffering is necessary for subsequent sample-based processing in PL. Similarly, unbuffering is needed while passing the data from PL to PS after the filtering operation of the receiver in PL (Receiver\_1). Note that the sampling time of the blocks in PS is  $75\mu s$  while the sampling time of the blocks in PL is  $1\mu s$ .

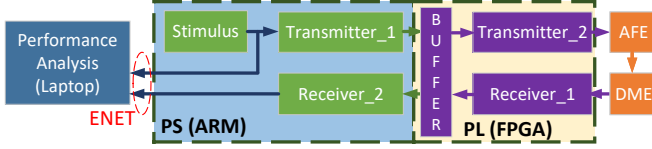


Fig. 14. Configurations V2-V9 of the transceiver.

Configurations V3-V9 are similar to V2, where few more blocks are moved from PS to PL. For instance, in V3, preamble addition and detection blocks are realizing in PL along with filtering (in FOFDM). The configuration V4 realizes the windowing, overlap and add block along with the preamble addition and detection in PL, and the rest of the blocks are implemented on PS. This configuration is only applicable in WOLA-OFDM. In configuration V5-V6, IFFT and CP addition operations are also moved to PL, and hence, frame size is reduced from 75 to 48, as shown in Table II. Similarly, in configuration V7, data modulation and demodulator blocks are moved to PL, which means Boolean data being transferred between PL and PS. For configurations V8-10, the number of data elements are reduced from 48 to 24 since channel encoder and decoders with a coding rate of  $\frac{1}{2}$  are moved to PL. In final configuration V10, an entire transceiver is realized on PL except for stimulus block. It can be observed that each configuration needs to be designed carefully to synchronize the data transfer between PS and PL. Furthermore, the architecture of the block changes when it is moved between PS and PL due to frame and sample-based processing. For PL implementation of each block, we have added pipelining inside the block as well as between the blocks. This demands additional synchronization efforts between PS and PL due to the change in latency.

## V. EXPERIMENTAL SETUP AND RESULT ANALYSIS

In this section, we present the details of the experimental setup and analyze different results to compare the performance and complexity of the proposed transceivers.

### A. Testbed Setup and Configuration

In this paper, we have used the Xilinx ZSoC ZC706 evaluation board shown in Fig. 15 for implementation of the proposed transceivers and its specifications are briefly given in the Table. III [34]. It consists of dual-core cortex A9 Advanced RISC Machines (ARM) as the software component (PS) and Xilinx 28nm Kintex 7-series as the hardware component (PL) [35]. It is a processor centered device in which PS always boots first and is fully autonomous to PL. Both

TABLE III  
SPECIFICATIONS OF ZYNQ BOARD

Device	ZC706
PL	Kintex-7
Registers	4,37,200
LUTs	2,18,600
DSP slices	900
BRAM blocks	545
Processor	ARM Cortex 9

PS and PL communicate with each other using the Advanced eXtensible Interface (AXI) protocol. There are 9 AXI ports between PS and PL, and in this project, we use four ports for communication between PS and PL. Among various AXI protocols, we use AXI-stream for communication between PS and PL and AXI-Lite for communication between various signal processing blocks realized in the PL.

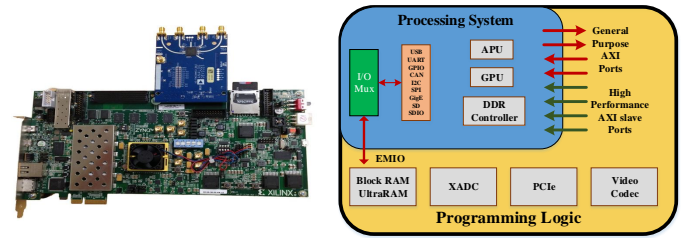


Fig. 15. Xilinx ZC706 evaluation board along with its important architectural features [35].

For the design and implementation of the transceivers, we have used MATLAB 2017b and Vivado 2016.4. These are augmented with various MATLAB toolboxes such as Embedded coder and HDL coder/verifier to target the implementation on the PS and PL, respectively. To design and configure the AFE, we have used RF Toolbox along with communication and signal processing toolboxes, hardware support packages provided by Mathworks.

The AFE is programmed to meet the desired sampling and carrier frequency requirements of the LDACS. The custom digital and analog filters are designed and configured with the help of the RF Toolbox of the Matlab/Simulink. For the LDACS transceiver, the passband and stopband normalized frequencies are 0.33 and 0.41, respectively. The stopband attenuation is 80 dB, and the desired baseband sampling rate is 1.1 MHz. The filter at the receiver is identical to the transmitter. The local oscillator frequency is set to 985 MHz as the LDACS is deployed in the range of 960-1164 MHz, and for such up-conversion, various rate changer blocks are added in the design. The output of the AFE receiver is scaled by an appropriate factor (0.00019 to be exact) so that the power level of the signal at AFE receiver output closely matches the signal at AFE transmitter input. The AFE transceiver also introduces the phase noise due to transmission at RF frequency, and hence, it demands phase error estimation and correction at the receiver. For the proposed transceiver, we have used pilot signals in LDACS for phase estimation, and accordingly, correction is applied to all received samples. **Next, we present the experimental results demonstrating the PSD and BER performance of the proposed transceivers using the discussed ZSoC based testbed.**

### B. Power Spectral Density (PSD) Comparison

We begin with the PSD comparison for OFDM, WOLA-OFDM, and FOFDM based LDACS transceivers and analyzed their out-of-band (OOB) emission. Since higher OOB emission leads to higher interference to the legacy DME users, the transceivers should have lower OOB emission, and it should not exceed the desired interference constraints of the DME. Here, we assume that single LDACS transmitter is active in 1 MHz of the spectral gap between adjacent DME channels.

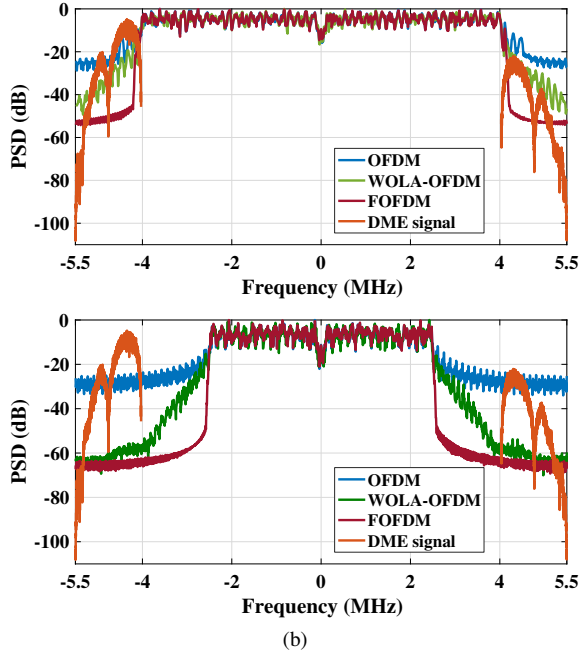


Fig. 16. The PSD comparison of various waveforms for two different transmission bandwidths, (a) 732kHz, and (b) 498kHz.

The PSD comparisons of OFDM, FOFDM, and WOLA-OFDM for 2 transmission bandwidths 1) 732 kHz and 2) 498 kHz are presented in Fig. 16 (a) and (b) respectively. The legacy DME transmission is shown using orange color. Note that 498 kHz is the maximum possible bandwidth of existing OFDM based LDACS beyond which it fails to meet the interference constraints of DME. Though FOFDM can achieve 800 kHz bandwidth, we have chosen 732 kHz because it can be achieved using the frame structure same as that of 498 kHz, making it compatible with legacy LDACS [25]. For all the transceivers, word-length (WL) is fixed and equal to 32 bits. It can be observed that the FOFDM has approximately 40 dB lower OOB emission and hence, much lower interference to the legacy DME signals. This allows FOFDM to increase the transmission bandwidth from the standard 498 kHz (maximum possible in OFDM) to 732 kHz leading to significant improvement of approximately 50% in the spectral utilization over existing OFDM based LDACS.

Next, we compare the performance of all transceivers by varying the WL. First, we change the WL of windowing and filtering blocks of the transceiver to 8/16 while keeping the WL of the rest of the transceiver to 32. As expected, there will be no change in the performance of OFDM as it does not involve windowing and filtering. The PSD of FOFDM and WOLA-OFDM for different WLs are shown in Fig 17 (a) and (b). It can be observed that the PSD for WLs of 16 and 32 are

almost identical, while there is significant degradation when WL is 8. Thus, it is possible to reduce the WL to 16 without compromising on the PSD performance.

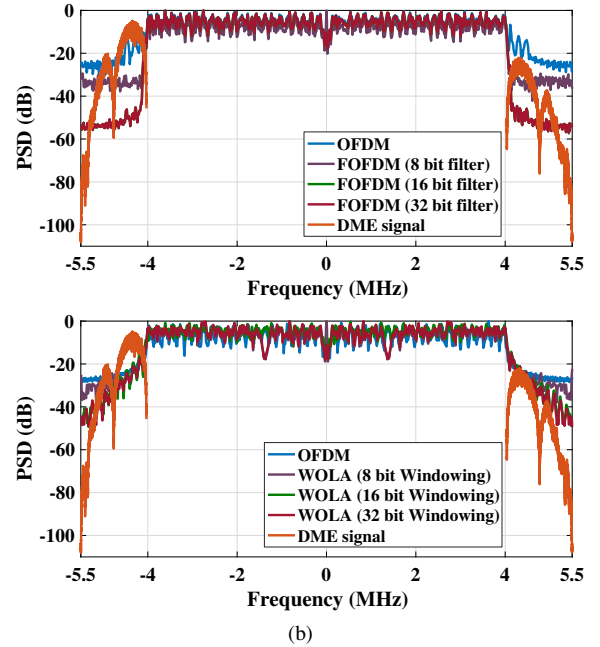


Fig. 17. The PSD comparison of different fixed length implementation of (a) Filter and (b) Windowing.

Next, we also analyzed the PSD performance when WL of the complete transceiver is reduced to 8 and 16 from 32. For illustration, we have shown the PSD of the OFDM in Fig. 18. Due to limited space constraints and to avoid repetitive results, we omitted the FOFDM and WOLA-OFDM transceivers. For all the transceivers, we observed that the PSD is almost identical for WL of 16 and 32, but there is significant degradation when WL is reduced to 8.

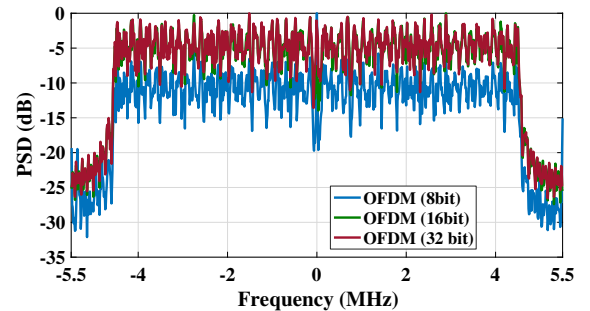


Fig. 18. The PSD comparison of various waveforms for different fixed lengths.

To summarize, we observed that the FOFDM offers superior PSD and hence, lower interference to legacy DME when compared to other transceivers. This allows FOFDM to have wider transmission bandwidth, which is desired for the future air to ground communication. However, better PSD at the cost of poor BER performance is not acceptable for wireless transceivers. Hence, we study the BER performance of various transceivers in the next sub-section.

### C. Bit Error Rate Comparison

For BER analysis, we consider end-to-end transceiver with LDACS channels (ENR, APT and TMA), DME interference,

and RF impairments due to the AFE. We consider two transmission bandwidths: 1) 732 kHz and 2) 498 kHz. All BER results are obtained from hardware with at least 1000 frames of data.

As shown in Fig. 19, FOFDM offers better BER performance than OFDM and WOLA-OFDM for a wide range of SNRs. This is mainly due to the ability of FOFDM to reduce the effect of DME interference due to inherent filtering operation at the transmitter and receiver. Note that though BER performance of WOLA-OFDM and OFDM is acceptable for 732 kHz, they cannot be deployed due to severe interference to DME.

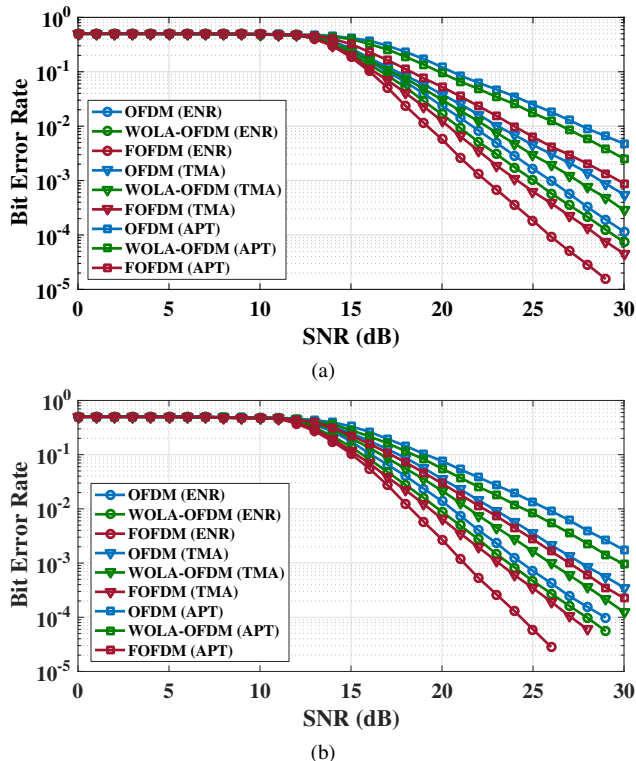


Fig. 19. The BER comparison of various waveforms for two different transmission bandwidths, (a) 732kHz, and (b) 498kHz and three different channels.

Similar to PSD analysis, we compare the BER performance for three different WLs, 32, 16, and 8. As shown in Fig. 20, BER performance degrades with the decrease in WL for all the transceivers. However, FOFDM offers significantly better performance than others. In fact, the BER of FOFDM with WL of 16 is significantly better than that of WOLA-OFDM with WL of 32. Similarly, the BER of FOFDM with WL of 8 is significantly better than that of OFDM and WOLA-OFDM with WL of 32 and 16, respectively.

Next, we study the effect of WL of windowing and filtering blocks on the BER. Since the PSD and BER performance of transceivers with the WL of 16 and 32 are comparable, we have used the transceiver with WL of 16 for the results shown in Fig 21. It can be observed that the FOFDM with filtering operation using WL of 16 and 32 offers similar performance while its performance degrades when the WL is reduced to 8. The same trend is also observed for WOLA-OFDM. Thus, the selection of WL is an important criterion for transceiver, and

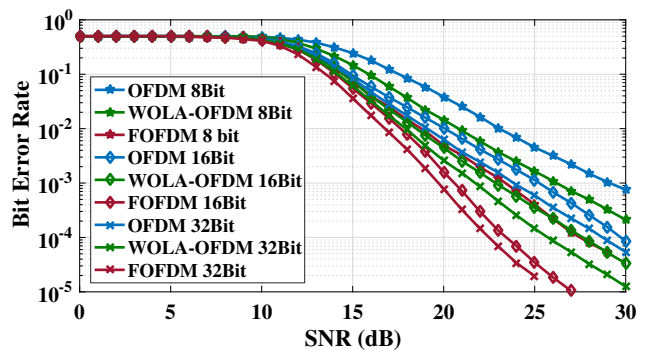


Fig. 20. The BER comparison of various waveforms for different fixed lengths

higher WL may not guarantee a higher gain in performance. In terms of BER and PSD, FOFDM not only offers better performance but also leads to higher transmission bandwidth. However, this gain in performance should not come at a high cost in terms of complexity. To analyze this, we present the area and power complexity of these transceivers in the next sub-section.

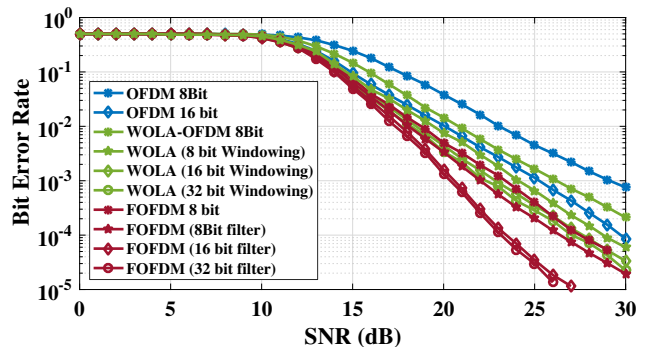


Fig. 21. The BER comparison of various waveforms for different fixed lengths of filter and windowing operation

#### D. Resource Utilization and Power Consumption

In this subsection, we compare the resource utilization and power consumption of the proposed OFDM, WOLA-OFDM, and FOFDM architectures for ten different configurations. Since the bandwidth of the transceiver is tunable, the results are shown in Table IV corresponds to 732 kHz bandwidth, which has higher complexity than 498 kHz bandwidth. To begin with, we consider the WL of 16 in Table IV. All results are obtained after realizing the transceiver on ZC706 from Xilinx.

As shown in Table IV, the comparison is made in terms of the number of flip-flops, DSP48 (embedded multipliers), look-up-table (LUT) for memory, LUT for logical and arithmetic operations, multiplexers and dynamic power consumption of the PL. The static power consumption of PS (1.566 W) and PL (0.247W) is, as expected, identical for all configurations and hence, not shown in the table.

Since V1 configuration is realized completely in PS, PL resource utilization results are omitted. In V2, FOFDM resource utilization is due to the filtering block realized in PL. As expected, multiply-accumulate operations in the filter are

TABLE IV  
RESOURCE UTILIZATION AND POWER CONSUMPTION OF TRANSCIVER ON ZSOC

Parameter	Waveform	V2	V3	V4	V5	V6	V7	V8	V9	V10
No. of Flip-Flops	OFDM	N/A	14200 (3.25%)	N/A	31617 (7.21%)	31945 (7.29%)	32628 (7.45%)	33982 (7.75%)	37738 (8.61%)	38193 (8.72%)
	WOLA-OFDM	N/A	14200 (3.25%)	23018 (5.26%)	33015 (7.54%)	34785 (7.93%)	38254 (8.75%)	41945 (9.58%)	43015 (9.83%)	44971 (10.02%)
	FOFDM	10100 (2.31%)	29954 (6.84%)	N/A	37285 (8.51%)	39120 (8.92%)	40015 (9.13%)	41184 (9.40%)	44015 (10.04%)	46253 (10.56%)
No. of DSP48	OFDM	N/A	534 (59.33%)	N/A	570 (63.33%)	570 (63.33%)	570 (63.33%)	570 (63.33%)	570 (63.33%)	570 (63.33%)
	WOLA-OFDM	N/A	534 (59.33%)	554 (61.56%)	570 (63.33%)	570 (63.33%)	570 (63.33%)	570 (63.33%)	570 (63.33%)	570 (63.33%)
	FOFDM	296 (32.89%)	785 (87.22%)	N/A	812 (90.22%)	812 (90.22%)	812 (90.22%)	812 (90.22%)	812 (90.22%)	812 (90.22%)
No. of LUT as Memory	OFDM	N/A	396 (0.56%)	N/A	865 (1.23%)	881 (1.25%)	918 (1.30%)	922 (1.31%)	941 (1.34%)	994 (1.35%)
	WOLA-OFDM	N/A	396 (0.56%)	685 (0.972%)	940 (1.34%)	945 (1.35%)	972 (1.38%)	982 (1.39%)	1050 (1.48%)	1102 (1.56%)
	FOFDM	64 (0.09%)	411 (0.583%)	N/A	894 (1.27%)	913 (1.29%)	936 (1.32%)	943 (1.34%)	964 (1.37%)	995 (1.41%)
No. of LUT as Logic	OFDM	N/A	22083 (10.10%)	N/A	31687 (14.50%)	31985 (14.63%)	32555 (14.89%)	33509 (15.328%)	35509 (16.24)	36657 (16.77%)
	WOLA-OFDM	N/A	22083 (10.10%)	30513 (13.96%)	33218 (15.195%)	34824 (15.96%)	36156 (16.54%)	37599 (17.20%)	41621 (19.04%)	44376 (20.30%)
	FOFDM	5350 (2.45%)	25361 (11.61%)	N/A	32811 (15.01%)	34495 (15.78%)	35391 (16.19%)	37052 (16.95%)	40660 (18.60%)	42539 (19.46%)
No. of MUXes	OFDM	N/A	35	N/A	683	745	1144	1217	1882	1930
	WOLA-OFDM	N/A	35	872	1254	1501	1784	1835	2575	2725
	FOFDM	25	57	N/A	835	1152	1401	1523	1985	2102
Dynamic Power in Watt	OFDM	N/A	0.045	N/A	0.285	0.295	0.297	0.299	0.301	0.304
	WOLA-OFDM	N/A	0.073	0.161	0.294	0.296	0.299	0.301	0.302	0.306
	FOFDM	0.112	0.205	N/A	0.434	0.493	0.494	0.496	0.500	0.509

mapped to DSP48 to get the best possible performance. In V3, preamble addition and detection block is moved to PL, and due to in-built auto-correlation operations, it is one of the most complicated block as evident from the increase in the resource utilization compared to V2. Similarly, a significant increase in resource utilization and power consumption is observed in V5, where FFT/IFFT is moved from PS to PL.

To summarize, FOFDM incurs 27% higher DSP48 than others due to MAC-based filtering, which can be shifted to LUT if needed. For example, windowing operation in WOLA-OFDM is realized using a combination of DSP48 and LUTs. The utilization of the rest of the resources is almost identical in all three waveforms. The IFFT/FFT block consumes the highest power, followed by filtering in the FOFDM. Due to limited space constraints, we have skipped some results. For completeness of the discussion, we briefly mention the observations: 1) The power consumption of the FOFDM increases slightly if we reduce the number of DSP48 at the cost of LUT as logic, 2) Resource utilization and power consumption increases with the rise in the WL, 3) The process of pipelining the transceiver architecture involves addition of registers at the appropriate locations so as to reduce the critical path delay. The reduction in critical path delay allows the transceiver to be clocked at higher frequency. Thus, pipelining offers trade-off between resource (number of FFs) utilization and clock period. For instance, the critical path delay with and without pipelining for OFDM, WOLA-OFDM and FOFDM transceivers are {9.75 ns, 10.25 ns, 12.5 ns} and {259 ns,

265.83 ns, 271.23 ns}, respectively. Furthermore, pipelining incurs additional latency due to newly added registers [36].

In Fig. 21, we discussed the effect of WL of filter coefficients in the filtering block of FOFDM on BER. In the case of resource utilization, we observed the increase in the utilization with WL, as shown in Fig 22. For WOLA-OFDM, different WL of windowing coefficients is not feasible for air to ground communications due to poor PSD and BER performance.

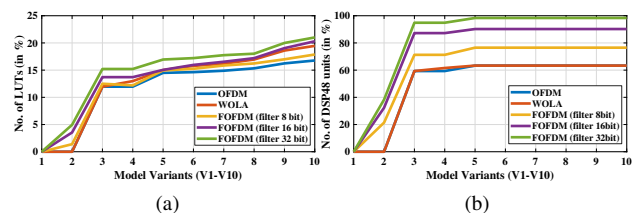


Fig. 22. Analysis of resource utilization on ZC706 for different model variants and fixed lengths, (a) Number of LUTs and (b) Number of DSP48 units.

The above-discussed results show that the FOFDM offers better sidelobe attenuation and better BER performance in trade-off to resource utilization. Filter designed by considering 8 bit fixed WL performs worse than 16/32 bit filter in terms of PSD and BER but better in terms of resource utilization. The FOFDM has a higher usage of resources compared to OFDM and WOLA-OFDM but still uses less than 50% of the Zynq ZC702 resources except for DSP48. This makes the FOFDM based LDACS as an appealing substitute to the future air to ground communication.



## VI. CONCLUSION

In this paper, we proposed the design and implementation of end-to-end LDACS transceiver on Xilinx ZC706 FPGA via a hardware-software co-design approach. We considered OFDM based LDACS and improved the performance using windowing and/or filtering. The proposed approach offers flexibility to choose the configuration along with the word-length for a given area, power, and delay constraints. The transceiver architectures are then integrated with analog front-end to endorse its performance in the presence of various RF impairments, DME interference, and LDACS specific wireless channels. Detailed experimental results are presented to analyze the area, power, PSD, and BER performance for OFDM, WOLA-OFDM, and FOFDM, having three word-lengths of 8/16/32 bit. The results show that the transceivers with the WL of 16 and 32 bit offer similar performance while the performance degrades for 8 bit WL. The Filtered OFDM based LDACS performs much better in terms of out of band emission (approximately 40 dB) and has significantly better BER performance, which allows adapting a wider transmission bandwidth up to 732 kHz with a slight penalty in terms of resource utilization and power consumption. This paper provides profound performance analysis and results to present the flexibility of end-to-end LDACS transceiver and proposed wide bandwidth FOFDM based LDACS offers an attractive solution for the next generation air to ground communication.

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