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Design and Analysis of a Gilbert Analog Multiplier for Input Dynamic Range Optimization

R. Vauche[1], Z. Benjelloun[1], R. Assila Belhadj Mefteh[1], W. Rahajandraibe[1], R. Bouchakour[1,2], H. Barthelemy[1]

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***Abstract*—In this paper, the design of a Gilbert analog multiplier is presented from design equations for input dynamic range optimization to measurement results, these last being obtained in the context of a square function dedicated to analog signal processing. The full circuit has been implemented using an AMS 0.35µm technology with a voltage supply (*VDD*) of 3.3V. Assuming a differential input voltage of +/-400mV with a common voltage of *VDD*/2, it is able to compute the square value of its differential input voltage with a mean precision of 2.92% in 5µs. Finally, the analog multiplier itself has a core area of 620µm² and offers power-gating capability, which enables a power consumption of 2.28µW when a duty cycle of 0.25% is considered.**

Keywords—analog multiplier, analog processing chain, energy detector, dynamic optimization, Gilbert cell, power-gating

I. Introduction

Among the different cardiovascular diseases which cause as many deaths as cancer in Europe, cardiac arrhythmia is one of the most common one. Fortunately, several types of cardiac arrhythmia can be detected using only heart rate variability [1]. To achieve it, the instantaneous heart rate can be estimated in real-time from pulsed physiological signals synchronized with heartbeats such as electrocardiogram [2], phono-cardiogram [3], arterial pressure [4] or photoplethysmogram [5]. It is also necessary to be able to detect each pulse associated to a heartbeat in one of these signals, which has led to the development of lots of detection methods [6].

Most of instantaneous heart rate detection methods are based on a digital signal processing [7][8][9] in addition to an analog conditioning chain for the pre-processing of the sensed signal. They also require at least an Analog-to-Digital Converter (ADC) and a computing unit such as a microcontroller, the both having a certain cost in terms of power, size, and price. However, the time during which cardiac arrhythmia is detectable can be very brief. Its detection also requires a full-time monitoring which can be more comfortably achieved from the patient point of view with a compact battery-powered device.

Unfortunately, advanced digital processing and full-time monitoring can be done by compact battery-powered devices at the cost of regular battery recharges. To reduce power consumption, size, and cost, it has been proposed in [2] a processing based on an analog energy detector to detect heartbeat-synchronized pulses in electrocardiograms, which has been inspired by low-power and low-cost non-coherent receivers used in Ultra-WideBand Impulse Radio (IR-UWB) [10]. The main processing step of this non-coherent detection requires to compute the square value of the sensed signal. This can be done in the analog domain with an analog multiplier which potentially has a smaller cost in terms of power consumption (especially when it can be periodically turned-off), size, and price compared to a digital processing.

Many analog multiplier architectures have been proposed in literature and especially the well-known Gilbert cells. However, they are usually able to work as a multiplier on a limited input voltage range. Indeed, a true multiplication can be obtained with bipolar Gilbert cells when input voltages are small in front of the twice of the thermal voltage, or with MOS Gilbert cells when one of the both input voltages is small and the other one is large. Although this is enough for mixing stage in wireless emitters and receivers, this becomes an issue when the square value of sensed physiological signals has to be computed since they can have a high dynamic range according to the measurement conditions.

For these reasons, the design of the MOS Gilbert cell is analyzed in section II in order to optimize the voltage input range for which a true multiplication can be obtained. In section III, post-layout simulation results of the designed multiplier are provided and analyzed in terms of computing precision of the multiplication. Next, section IV deals with the implementation of an analog square function built around the designed multiplier and shows measurements results which are compared to an ideal squarer.

II. Design of the Analog Multiplier

The designed analog multiplier is based on a Gilbert cell which has the advantages to use a limited number of transistors in addition to have high input impedances. Its transistor level schematic is shown on Fig. 1.a. This structure also consists of three differential pairs (M1-M2, M3-M4, and M5-M6), two active loads (MA and MB), and a current source M0 controlled here by a *PDB* signal, *PDB* being a logic signal which enables the multiplier to be switched-on or switched-off. Finally, for reasons of symmetry, it should be noted that the transistors M1 and M2 must have the same dimensions, as well as the transistors MA and MB and the transistors M3, M4, M5, and M6.

However, it should be noted that although *VD1* and *VD2* are differential inputs voltage, *VOP* is here a single output voltage thanks to the connection between the gate and the drain of the MA transistor. Thus, this analog multiplier and also, the processing chain where it could be used, does not require an additional differential to single voltage converter. Nevertheless, a differential output can be obtained by removing this connection but then requires an appropriate biasing of MA and MB gates.

In the following subsections, the designed analog multiplier is analyzed in order to demonstrate with the help of design equations that it can operate as a true multiplier over a large range of *VD1* and *VD2*.

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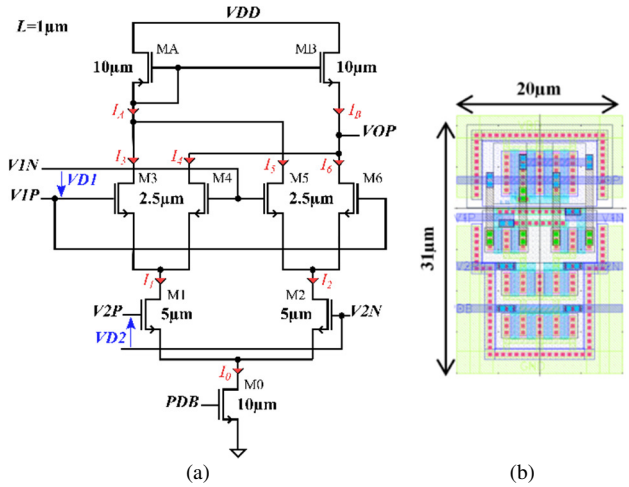

Fig. 1. Transistor level implemetation (a) of the designed analog multiplier and its layout implementation (b).

A. Biasing and Kirchhoff's Laws

To allow a four-quadrant multiplication on the widest dynamic range, the circuit must be biased as follows:

$$VOP = \frac{VDD}{2} \text{ when } V1P = V1N = V2P = V2N = \frac{VDD}{2}. \quad (1)$$

In this case, if capacitive effects are neglected, the output voltage *VOP* can be written for low working frequencies according to Fig. 1.a as follows:

$$VOP = \frac{VDD}{2} + R_{OUT} \cdot I_D \quad (2)$$

where R_{OUT} is the output resistance of the analog multiplier and I_D is the differential current in the active loads defined as follows:

$$I_D = I_A - I_B \quad (3)$$

with:

$$I_0 = I_A + I_B. \quad (4)$$

To demonstrate that the proposed circuit works as an analog multiplier, it is necessary to write I_D as a function of *VD1* and *VD2*. To do this, I_A and I_B can be written as follows:

$$I_A = I_3 + I_5 \quad (5)$$

$$I_B = I_4 + I_6, \quad (6)$$

which allows I_D to be computed as follows:

$$I_D = I_{D1} - I_{D2} \quad (7)$$

with:

$$I_{D1} = I_3 - I_4 \quad (8)$$

$$I_{D2} = I_6 - I_5 \quad (9)$$

where I_{D1} (resp. I_{D2}) is the differential current of the differential pair M3-M4 (resp. M5-M6), and I_X is the drain-source current of the MX transistor. Thus, it is now necessary to compute I_{D1} and I_{D2} using the well-known long channel MOS model introduced by Shockley [11] since every MOS length *L* has been set to 1µm according to Fig. 1.a.

B. Study of the Differential Pairs M3-M4 and M5-M6

In this subsection, the differential pair M3-M4 is firstly considered. Then, using the Kirchhoff's current law, I_1 can be written as follows:

$$I_1 = I_3 + I_4 \quad (10)$$

However, considering (1), M3 (resp. M4) must be in the saturation region of the Shockley's model since the drain-source voltage of M3 (resp. M4) is higher than its gate-source voltage minus the threshold voltage of NMOS transistors. This leads to:

$$I_3 = \frac{\beta_{3\text{-}6}}{2}\left(V_{GS3} - V_{TH}\right)^2 \quad (11)$$

$$I_4 = \frac{\beta_{3\text{-}6}}{2}\left(V_{GS4} - V_{TH}\right)^2 \quad (12)$$

with:

$$\beta_{3\text{-}6} = \mu \frac{\varepsilon_{ox}}{t_{ox}} \frac{W_{3\text{-}6}}{L} = \alpha \frac{W_{3\text{-}6}}{L} \quad (13)$$

where μ is the electron mobility, ε_{ox} is the oxide permittivity, t_{ox} is the oxide thickness, $W_{3\text{-}6}$ is the width of transistors used in M3-M4 and M5-M6, V_{GSX} is the gate-source voltage of MX, and V_{TH} is the threshold voltage of NMOS transistors. For the considered 0.35µm technology, α is about 200µA/V^2 and V_{TH} is about 0.55V.

By solving the equation system constituted by (8) and (10), it is possible to write with the help of (11) and (12):

$$I_1 + I_{D1} = \beta_{3\text{-}6}\left(V_{GS3} - V_{TH}\right)^2 \quad (14)$$

$$I_1 - I_{D1} = \beta_{3\text{-}6}\left(V_{GS4} - V_{TH}\right)^2 \quad (15)$$

which enables to write V_{GS3} and V_{GS4} as follows:

$$V_{GS3} = \sqrt{\left(I_1 + I_{D1}\right)/\beta_{3\text{-}6}} + V_{TH} \quad (16)$$

$$V_{GS4} = \sqrt{\left(I_1 - I_{D1}\right)/\beta_{3\text{-}6}} + V_{TH}. \quad (17)$$

However, since *V1P* and *V1N* can be expressed as follows:

$$V1P = VDD/2 + VD1/2 = V_{GS3} + V_{DS1} + V_{DS0} \quad (18)$$

$$V1N = VDD/2 - VD1/2 = V_{GS4} + V_{DS1} + V_{DS0} \quad (19)$$

with V_{DSX} is the drain-source voltage of MX transistor, the differential input voltage *VD1* can be written as follows:

$$VD1 = V_{GS3} - V_{GS4} = \left(\sqrt{I_1 + I_{D1}} - \sqrt{I_1 - I_{D1}}\right)/\sqrt{\beta_{3\text{-}6}}. \quad (20)$$

By supposing:

$$\left|I_{D1}\right| \ll I_1 \quad (21)$$

which is true thanks to (19) while:

$$\left|VD1\right| \ll VDD - 2\left(V_{DS1} + V_{DS0} + V_{TH}\right) \quad (22)$$

since (21) leads to:

$$0 \ll 2\left(V_{GS4} - V_{TH}\right)^2 \quad (23)$$

and also to:

$$V_{TH} \ll V_{GS4}, \quad (24)$$

(20) becomes:

$$VD1 = I_{D1} / \sqrt{\beta_{3-6} I_1} \tag{25}$$

which allows the differential current I_{D1} of the differential pair M3-M4 to be written as follows:

$$I_{D1} = VD1 \sqrt{\beta_{3-6} I_1} \,. \tag{26}$$

By following the same reasoning from (10) to (25) for the differential current I_{D2} of the differential pair M5-M6, I_{D2} can be written as follows:

$$I_{D2} = VD1 \sqrt{\beta_{3-6} I_2} \tag{27}$$

which is true while:

$$|VD1| \ll VDD - 2\left(V_{DS2} + V_{DS0} + V_{TH}\right). \tag{28}$$

Thus, (7) becomes:

$$I_D = VD1 \sqrt{\beta_{3-6}} \left(\sqrt{I_1} - \sqrt{I_2}\right) \tag{29}$$

while (22) and (28) are true and it is also necessary to study the differential pair M1-M2 to link I_D to $VD2$.

C. Study of the Differential Pair M1-M2

In literature, M1 and M2 transistors are usually considered in saturation region which leads to:

$$I_D = \sqrt{\frac{\beta_{3-6}\beta_{1-2}}{2}} \cdot VD1 \cdot VD2 \tag{30}$$

since:

$$I_1 = \frac{\beta_{1-2}}{2}\left(V_{GS1} - V_{TH}\right)^2 \tag{31}$$

$$I_2 = \frac{\beta_{1-2}}{2}\left(V_{GS2} - V_{TH}\right)^2 \tag{32}$$

with:

$$\beta_{1-2} = \mu \frac{\varepsilon_{ox}}{t_{ox}} \frac{W_{1-2}}{L} = \alpha \frac{W_{1-2}}{L} \tag{33}$$

where W_{1-2} is the width of M1 and M2 transistors.

However, in practical, it is not possible to bias M1 and M2 in saturation region due the stacking of 4 MOS lines between the ground and the voltage supply when the Gilbert multiplier is biased according to (1). Indeed, this biasing requires that:

$$V_{DSX} > V_{DSXsat} = V_{GSX} - V_{TH} \tag{34}$$

where X has to be replaced by 1 or 2 according to the considered transistor is M1 or M2. When applied to M1 and M2, (34) leads to the following impossible conditions:

$$VD2 \ll -VD1 \tag{35}$$

$$VD2 \gg VD1\,, \tag{36}$$

since (22) and (28) combined to (34) can be written as follows:

$$2V_{DS1sat} \ll VDD - VD1 - 2\left(V_{DS0} + V_{TH}\right) \tag{37}$$

$$2V_{DS2sat} \ll VDD - VD1 - 2\left(V_{DS0} + V_{TH}\right) \tag{38}$$

where V_{GSX} and also V_{DSXsat} can be computed with the help of:

$$V2P = VDD/2 + VD2/2 = V_{GS1} + V_{DS0} \tag{39}$$

$$V2N = VDD/2 - VD2/2 = V_{GS2} + V_{DS0}\,. \tag{40}$$

M1 and M2 can also never been in the saturation region in the same time.

For this reason, it is now considered in this paper that M1 and M2 operate in linear region which leads according to the Shockley model to:

$$I_1 = \beta_{1-2}\left(V_{GS1} - V_{TH} - V_{DS1}/2\right)V_{DS1} \tag{41}$$

$$I_2 = \beta_{1-2}\left(V_{GS2} - V_{TH} - V_{DS2}/2\right)V_{DS2}\,. \tag{42}$$

Thus, by supposing that:

$$V_{GS1} - V_{TH} \gg V_{DS1}/2 \tag{43}$$

$$V_{GS2} - V_{TH} \gg V_{DS2}/2 \tag{44}$$

(41) and (42) can be written as follows:

$$I_1 = \beta_{1-2}\left(V_{GS1} - V_{TH}\right)V_{DS1} \tag{45}$$

$$I_2 = \beta_{1-2}\left(V_{GS2} - V_{TH}\right)V_{DS2}\,. \tag{46}$$

According to the Fig. 1.a, I_1 and I_2 can be equally written as a function of the bias current I_0 and of the differential current I_{D0} of the differential pair M1-M2:

$$I_1 = \left(I_0 + I_{D0}\right)/2 \tag{47}$$

$$I_2 = \left(I_0 - I_{D0}\right)/2 \tag{48}$$

since:

$$I_0 = I_1 + I_2 \tag{49}$$

$$I_{D0} = I_1 - I_2\,, \tag{50}$$

which allows (29) to be rewritten as follows:

$$I_D = \sqrt{\beta_{3-6}/2} \cdot VD1 \cdot \left(\sqrt{I_0 + I_{D0}} - \sqrt{I_0 - I_{D0}}\right) \tag{51}$$

and simplified to:

$$I_D = \sqrt{\beta_{3-6}/(2I_0)} \cdot VD1 \cdot I_{D0} \tag{52}$$

when:

$$|I_{D0}| \ll I_0 \tag{53}$$

which is true by replacing I_1, and I_2 in (49) and (50) with their expression given (45) and (46) when:

$$|VD2| \ll VDD - 2\left(V_{DS0} + V_{TH}\right). \tag{54}$$

Considering the assumptions made on V_{DS1} and V_{DS2} indicated in (43) and (44), it is also possible to assume that V_{DS1} and V_{DS2} have small variations compared to their average values and therefore that:

$$V_{DS1} \simeq V_{DS2} \simeq \left(V_{DS1} + V_{DS2}\right)/2 \tag{55}$$

By injecting now (45) and (46) in (50) taking into account (39) and (40), this gives:

$$I_{D0} = \beta_{1-2} \cdot VD2 \cdot \left(V_{DS1} + V_{DS2}\right)/2 \tag{56}$$

since:

$$VD2 = V_{GS1} - V_{GS2}\,. \tag{57}$$

Using (52) and (56), the differential current I_D of the analog multiplier can also be written as follows:

$$I_D = \beta_{1\text{-}2} \cdot \sqrt{\frac{\beta_{3\text{-}6}}{2I_0}} \cdot \frac{V_{DS1}+V_{DS2}}{2} \cdot VD1 \cdot VD2 \qquad (58)$$

which demonstrates that the proposed Gilbert cell works as a voltage multiplier while (28) and (54) are true when M3 to M6 operate in saturation region and M1 and M2 in linear region. It can be noted that the drain-source voltage of M0, M1, and M2 should be as low as possible to optimize the input voltage range of the multiplier.

Finally, it is possible to write (58) using only the technology parameters, the biasing current I_0 and V_{DS0}. For this, by now injecting (45) and (46) in (49) and taking into account (39), (40), and (55), I_0 can be written as follows:

$$I_0 = \beta_{1\text{-}2} \frac{V_{DS1}+V_{DS2}}{2} \left(VDD - 2 \cdot \left[V_{DS0}+V_{TH}\right]\right) \qquad (59)$$

which leads using (58) and (59) to:

$$I_D = \sqrt{\frac{\beta_{3\text{-}6} I_0}{2}} \cdot \frac{1}{VDD - 2 \cdot \left[V_{DS0}+V_{TH}\right]} \cdot VD1 \cdot VD2 \cdot \qquad (60)$$

Thus, the output voltage of the proposed analog multiplier can be written as follows:

$$VOP = VOP_{OFFSET} + K \cdot VD1 \cdot VD2 \qquad (61)$$

where K is the gain of the analog multiplier which is equal to:

$$K = \sqrt{\frac{\beta_{3\text{-}6} I_0}{2}} \cdot \frac{R_{OUT}}{VDD - 2 \cdot \left[V_{DS0}+V_{TH}\right]} \qquad (62)$$

and VOP_{OFFSET} is the output offset voltage which is equal to:

$$VOP_{OFFSET} = \frac{VDD}{2} \cdot \qquad (63)$$

III. Post-Layout Simulations of the Designed Analog Multiplier

The proposed analog multiplier has been implemented using an AMS 0.35µm CMOS technology with a supply voltage of 3.3V. Its layout is shown in Fig. 1.b and has a core area of 620µm^2. The size and the post-layout simulated operating point of each MOS transistor is shown in Tab. I when *V1P*, *V1N*, *V2P*, and *V2N* are set to *VDD*/2 (1.65V) and when *PDB* is equal to *VDD* (3.3V). These values lead to an output voltage *VOP* of 1.75V instead of *VDD*/2 (1.65V) as initially desired in (1). However, this is not an issue since it is just an offset which can be taken into account by increasing the threshold used in the analog processing chain [10]. Finally, operating regions of each transistor are in accordance with the theoretical analysis.

To analyze multiplier performances in terms of computing precision, the distribution of its gain K defined in (61) has been studied using post-layout simulations for given ranges of *VD1* and *VD2*. Indeed, K being extracted as a gain relative to the true multiplication, the less the distribution of K over an input range is wide, the more the multiplier is accurate. Thus, the figure of merit used here is the relative standard deviation (also known as coefficient of variation) of K in percent noted $c_{V\text{-}K}$ which is defined, with the help of the average value of K noted μ_K and the standard deviation of K noted σ_K, as follows:

$$c_{V-K} = \frac{\sigma_K}{\mu_K} \times 100 \cdot \qquad (64)$$

TABLE I. Size and Biasing of MOS Transistors used in the Deisgned Multiplier

MOS	W (µm)	L (µm)	$\lvert I_{DS}\rvert$ (µA)	$\lvert V_{GS}\rvert$ (V)	$\lvert V_{DS}\rvert$ (V)	Region
M0	10	1	275	3.3	0.1	Linear
M1-M2	5	1	138	1.55	0.25	Linear
M3-M6	2.5	1	68.8	1.3	1.4	Saturation
MA-MB	10	1	138	1.55	1.55	Saturation

The output voltage *VOP* obtained for the range of *VD1* and *VD2* defined over the interval [-400mV; 400mV] is shown in Fig. 2 when *VD1* is independent of *VD2*. From this curves network, the distribution of K for different ranges of *VD1* and *VD2*, which are [-100mV; 100mV], [-200mV; 200mV] and [-400mV; 400mV], has been extracted and results are shown in Tab. II. It also appears that μ_K is relatively stable over the ranges since it is between 4.51 and 4.60. Moreover, σ_K and $c_{V\text{-}K}$, decreases as the ranges of *VD1* and *VD2* are reduced. This was expected since the more the ranges of *VD1* and *VD2* are small, the more the conditions seen during the theoretical study on *VD1* and *VD2* are true. Furthermore, for the range [-400mV; 400mV] corresponding to the worst case, $c_{V\text{-}K}$ which represents the mean computing precision of the multiplier is 5.72%. Finally, the theoretical conditions on the voltage ranges of *VD1* and *VD2* allowing multiplier operation of the proposed circuit are verified since *VD1* (resp. *VD2*) is small in front 1.5V (resp. 2V) according to (28) (resp. (54)).

Since the proposed analog multiplier has to be used in an energy detector, the distribution of the gain K has been equally studied when it works as a squaring stage, or in other words, when *VD1* is equal to *VD2*. The output voltage *VOP* obtained for the *VD1* range (and also *VD2* range) [-500mV; 500mV] is shown in Fig. 3. To verify that the circuits operates as a true square function, the curve of an ideal squarer having a gain of 4.5 has been plotted on the same figure. It appears that the curves are very close to each other as confirmed by the analysis of the distribution of K indicated in Tab. III. Indeed, it appears that for the interval [-400mV; 400mV], μ_K value is 4.50 and $c_{V\text{-}K}$ (mean computing precision of the squarer) is only 1.14% which is better than the 5.72% obtained in multiplier mode.

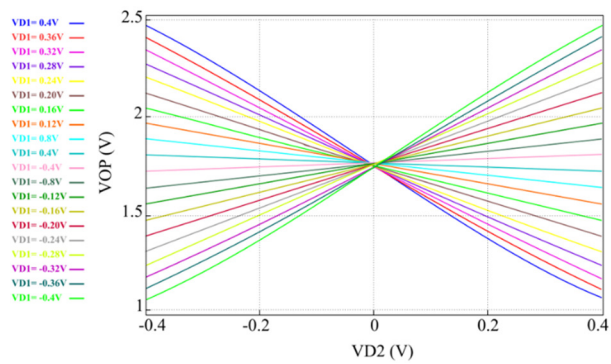

Fig. 2. DC transfer characteristics of the proposed analog multiplier for a high impedance output load when *VD1* and *VD2* are independent.

TABLE II. Simulated Distribution of K for a High Impedance Output Load.when *VD1* and *VD2* are Independent

VD1 and VD2 range	μ_K	σ_K	$c_{V\text{-}K}$ (%)
[-100mV;+100mV]	4.51	0.12	2.59
[-200mV;+200mV]	4.54	0.18	3.86
[-400mV;+400mV]	4.60	0.26	5.72

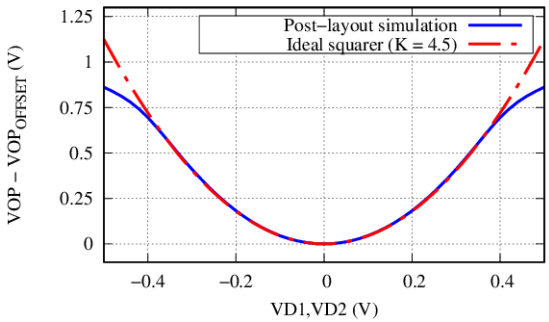

Fig. 3. DC transfer characteristic of the proposed analog multiplier for a high impedance output load when *VD1* is equal to *VD2*.

TABLE III. SIMLATED DISTRIBUTION OF *K* FOR A HIGH IMPEDANCE OUTPUT LOAD WHEN *VD1* IS EQUAL TO *VD2*.

VD1 and VD2 range	μ_K	σ_K	$c_{V\text{-}K}$ (%)
[-100mV;+100mV]	4.49	6.48e-3	0.14
[-200mV;+200mV]	4.50	18.9e-3	0.42
[-400mV;+400mV]	4.50	51.2e-3	1.14

Finally, the multiplier output has a speed of variation of 0.56V/µs on a capacitive load of 10pF for a simultaneous step of *VD1* and *VD2* from 0V to 0.4V. According to Tab. I, the current consumed by the multiplier is 275µA (i.e. a power consumption of 0.91mW) when it is turned-on (*PDB* = *VDD*), but it is only 5pA (i.e. a power consumption of 16.5pW) when it is turned off (*PDB* = 0V). Thanks to its output slew rate and its very low power consumption when it is turned-off, it is therefore possible to use a power management scheme which consists in turning-off the circuits as soon as they have accomplished their task [12][13]. Thus, assuming that it is possible to compute the multiplication using the proposed circuit and to store the result in a capacitor in less than 10µs, the multiplier would be turned-on with a duty cycle of only 250/100 000 (0.25%) since 250Hz is a sufficient sampling frequency to detect pulses centred on 10Hz which are synchronized with heart beats in electrocardiograms [2]. In this case, the average power consumption of the proposed analog multiplier would be only 2.28µW.

IV. MEASUREMENT RESULTS OF THE SQUARE FUNCTION BASED ON THE DESIGNED MULTIPLIER

The designed multiplier has a single output but two differential inputs. To use it as an analog square function which has a single input, op-amp based subtractors with *R*=100kΩ have been implemented on chip before the multiplier as shown on Fig. 4. They also allow the single input having an offset of *VDD*/2 (1.65V) to be transformed to a symmetrical input around *VDD*/2. Furthermore, *V1P* and *V2P* as well as *V1N* and *V2N* have been connected together to have *VD1* equal to *VD2* and thus, to use the multiplier as a square function. Finally, op-amp based followers have been implemented to isolate the square function from input source and output load. It can be noted that all used op-amps are standard IPs of the 0.35µm AMS design kit, which have led to a core area of 0.9mm² for the full squarer. The obtained square function is also not optimal in terms of space and power consumption since its goal is just to highlight the multiplier performances in terms of input voltage range and precision.

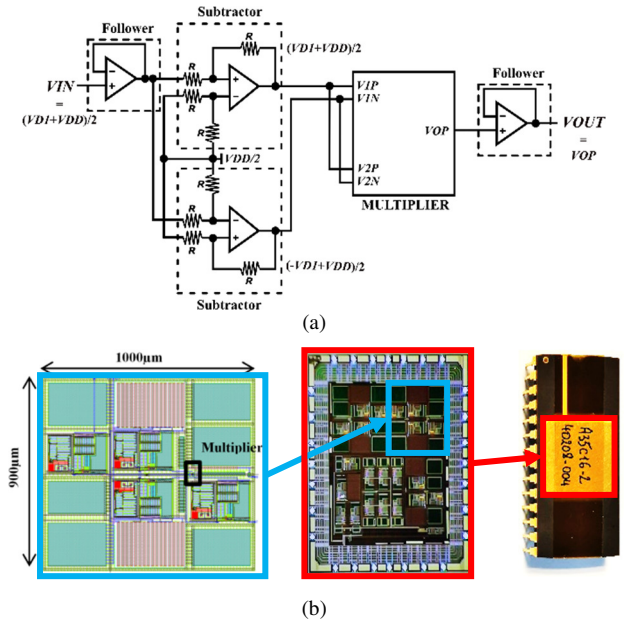

Fig. 4. Implemented square function based on the designed multiplier: schematic (a) ; layout implementation, chip photography and package photography (b).

The DC transfer characteristic of the implemented square function has been measured and compared to the ideal response of a square function having a gain of 3.5 in Fig. 5. It appears that the curves are close to each other for *VD1* range [-400mV;400mV]. However, compared to the post-layout simulations of the stand-alone multiplier, the gain has decreased from 4.5 to 3.5 due to process variations and the additional load introduced by the op-amp based functions. About the distribution of K, it appears that the measured relative standard deviation $c_{V\text{-}K}$ of the gain *K* has increased from 1.14% to 2.93% for the *VD1* range [-400mV;400mV] according to Tab. IV. Moreover, unlike post-layout simulations of the stand-alone multiplier, $c_{V\text{-}K}$ increases for as the *VD1* range decreases. These both phenomena are due to the observed output noise when *VD1* is near to 0V since the square of a near zero value is lower than this near zero value. Finally, transient response of the squarer for a 1kHz triangular voltage input is shown in Fig. 6 and follows well the DC characteristic. In addition, the impulse response of the squarer is given in Fig. 7 and shows an overshoot of 66% and a response time defined at 5% around the final output step equals to 5µs. Unfortunately, the power consumption of the multiplier alone has not been verified since other circuits are connected on the same *VDD* pin.

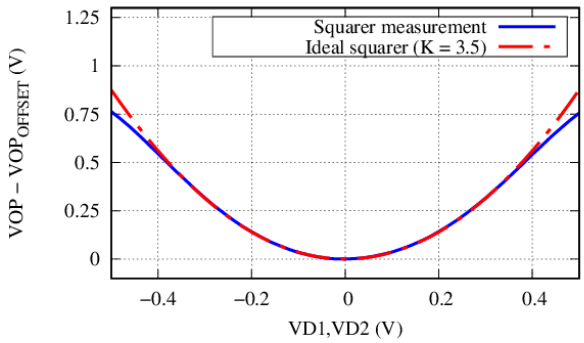

Fig. 5. DC transfer characteristic of the designed analog square function based on the proposed multiplier for a high impedance output load.

TABLE IV. MEASURED DISTRIBUTION OF *K* FOR A HIGH IMPEDANCE OUTPUT LOAD WHEN *VD1* IS EQUAL TO *VD2*

VD1 and VD2 range	μ_K	σ_K	$c_{V\text{-}K}$ (%)
[-100mV;+100mV]	3.59	210e-3	5.86
[-200mV;+200mV]	3.56	136-3	3.83
[-400mV;+400mV]	3.52	103-3	2.93

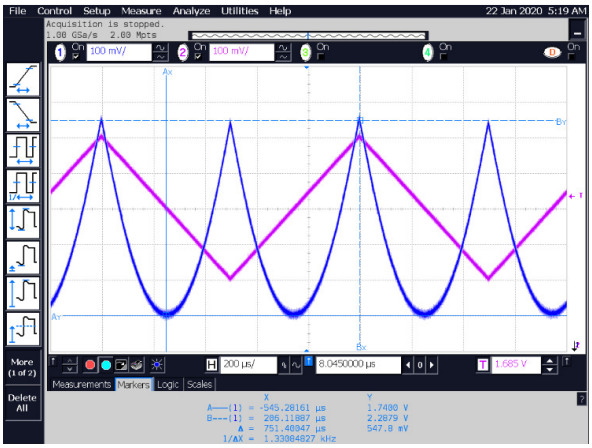

Fig. 6. Transient response of the analog square function for a 1kHz triangular voltage input (0.4Vpp around *VDD*/2=1.65V) on a high impedance output load.

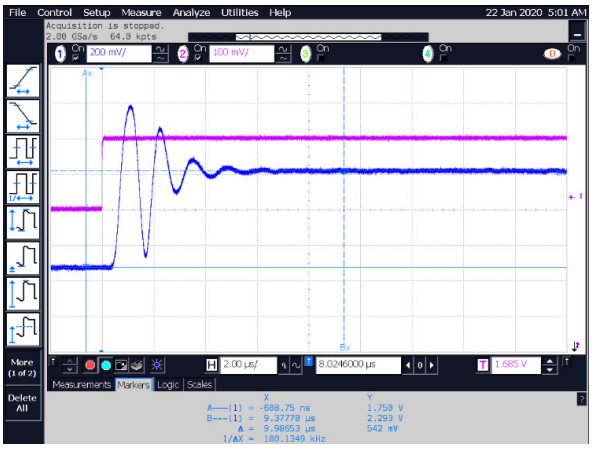

Fig. 7. Impulse response of the analog square function for a 1kHz square voltage input (V_{LOW} = *VDD*/2 = 1.65V, V_{HIGH} = *VDD*/2 + 0.2 = 1.85V) on a high impedance output load.

V. CONLUSION

In this paper, a Gilbert analog multiplier has been presented from design equations for input dynamic range optimization to measurement results, these last being obtained in the context of a square function dedicated to analog signal processing. The full circuit has been implemented using an AMS 0.35µm technology with a voltage supply (*VDD*) of 3.3V. Assuming a differential input voltage of +/-400mV with a common voltage of *VDD*/2, it is able to compute the square value of its differential input voltage with a mean precision of 2.92% in 5µs. Finally, the analog multiplier itself has a core area of 620µm^2 and offers power-gating capability, which enables a power consumption of 2.28µW when a duty cycle of 0.25% is considered. As it has been done using post-layout simulations in [2], the test chip must now be inserted in a full processing chain in order to verify its ability to detect pulses synchronized with heartbeats in electrocardiogram according to the Signal-to-Noise Ratio (SNR) of the sensed signal. However, the accuracy of the proposed multiplier could be improved. Firstly, the proposed Gilbert cell works in open loop which simplifies the design and the standby of the cell, but makes it sensitive to Process, Voltage, and Temperature (PVT) variations. To reduce this sensitivity, a feedback could also be added on the gate of the MOS current source but removes the possibility to easily turn-off it using a logic signal. Secondly, the current source is achieved using a MOS transistor in linear region which makes the bias current (drain-source current of this MOS transistor) dependent to its drain-source voltage. This is due to the difficulty to bias this MOS transistor in saturation region with the targeted operating point and the same drain-source current (and also the same gain). Indeed, this necessitates to increase the MOS transistor width in order to enable a decrease of the gate-source voltage and also, removes again the possibility to easily turn-off the cell using a logic signal. Finally, in this work, bulks and sources of NMOS differential pairs are not biased to the same voltage, which can induce variations of the threshold voltage due to the body effect. To avoid it, a triple well option must be considered for NMOS transistors. Unfortunately, this process option is not available in every design kit and so, PMOS differential pairs should be considered for future designs since bulk of each PMOS can usually be separately biased.

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