New Noise Cancellation Topology in Common-gate LNAs

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New Noise Cancellation Topology In Common-gate LNAs

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Abstract

In this paper a new approach for designing noise canceling common gate (CG) low noise amplifiers (LNAs) is proposed. This method investigates using inductively degenerated common source (IDCS) stage in parallel with CG stage instead of common source(CS) stage. Considering special specification of IDCS LNA, proposed topology can achieve lower noise figure (NF) and better input impedance matching. Analytical calculation for this topology is performed and the equations to satisfy input impedance matching along with noise cancellation condition are presented. The NF of proposed LNA is also calculated while satisfying these conditions by using the calculation of each noise source's transfer function. To validate theoretical analysis, two different LNAs in X band are designed and optimized. The simulations are performed using Advanced Design System (ADS) electromagnetic momentum with GaAS pHEMT 0.1μm process model. The results shows the proposed method can achieve better input impedance matching and lower NF while the output impedance matching and gain have relatively the same behavior.

Keywords: Low noise Amplifier (LNA), Inductively degenerated common source (IDCS), Common Gate Amplifier, Noise figure (NF), Noise Cancellation.

1. Introduction

Rapid development of wireless communication systems has caused an increased demand for wide band low noise blocks with good input impedance matching.
To achieve the lowest possible noise figure (NF) and return loss with high gain over the desired bandwidth several topologies in low noise amplifiers (LNAs) design have been investigated. A frequent approach is common gate (CG) amplifier which provides wide band input matching due to its input impedance of 1 over g_m. The basic topology of CG is shown in Fig. 1 (a). In this topology NF can be calculated as in Eq. 1.

$$NF = 1 + \frac{\gamma}{g_m R_s} + \frac{R_s}{R_l}(1 + g_m R_s)^2 \quad (1)$$

R_s and R_l are the source and load resistance respectively and γ is the coefficient for the thermal noise of transistor. In matching condition this topology can achieve to a NF of $1 + \gamma + \frac{4R_s}{R_l}$. Therefore, even the input return loss remains in acceptable range over the frequency bandwidth, the NF is relatively high [1]. In this topology, different modifications has been previously proposed to decrease the NF of LNA in input matching conditions. These methods had the cost of extra parasitic elements that limit the frequency range of the LNA [2]-[3]. Fig. 1 (b) represents utilization of feedback element to improve the NF of this topology. According to this method by increasing the effective g_m, the NF decreases due to the reduction of channel noise effect [3]. The positive feedback have been also previously used in [4] in order to decrease the NF of LNA in input impedance matching. Using both positive and negative feedback is also investigated in [5] which can improve the NF in input matching condition. Noise cancellation technique is the other approach used to improve the performance of CG stage[6]-[8]. In this method a common source (CS) stage is used in parallel with CG stage to cancel its noise in expense of a limitation on the bandwidth of the LNA due to its capacitive input impedance. Moreover, the CS topology, itself has relatively high NF. Another low noise LNA with similar behavior to CS topology that can cancel out the noise of CG is inductively degenerated common source (IDCS). This topology is very common in high frequency LNAs with a very low noise behavior because of its capability of simultaneously impedance and noise matching (SNIM) for achieving minimum possible NF along with maximum gain [9]-[18]. In this topology, an inductor is added at the source terminal of the CS stage to achieve noise and impedance matching condition simultaneously by setting $\Gamma_{opt} = \Gamma_{in}^*$ [9]-[10], [16], [18].

In this paper, design procedure of new noise cancellation technique by using an IDCS stage instead of CS stage, is discussed. In spite of conventional method which uses CS stage to cancel out the noise of CG, IDCS parallel with CG stage is used. First analytical calculations that represents the feasibility of this topology is demonstrated and second the theoretical analysis of how the noise of common gate can be canceled out by IDCS stage is presented. Third the magnitude of circuit elements for noise canceling condition is presented. MATLAB simulation is also used to show the reduction of noise in proposed method in comparison to conventional method. To validate the theo-

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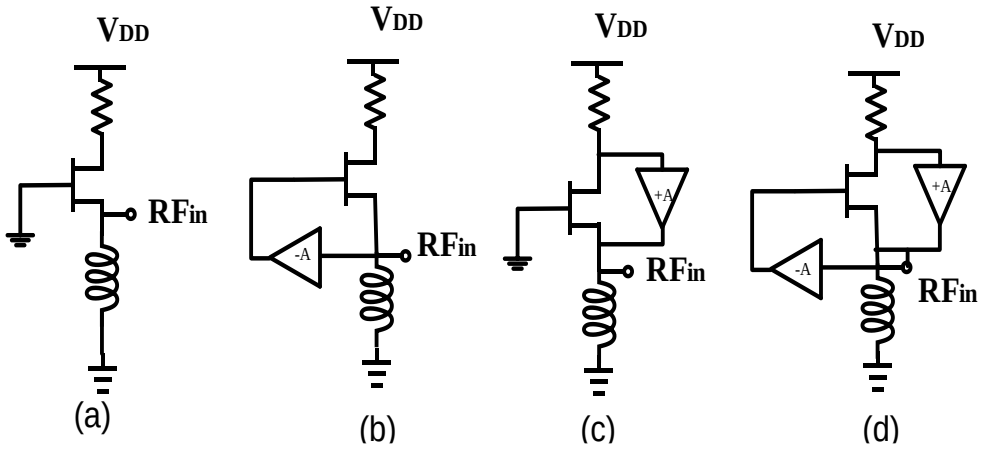

Figure 1: Different common gate LNAs

retical analysis, two different LNAs with conventional method and proposed one are designed and compared using ADS (Advanced Design System) with technology file of GaAs pHEMT 0.1 μm.

This paper is arranged in two main parts. In the first section, analytical calculation of overall NF and noise cancellation condition is presented. In this section, the noise behavior of two noise cancellation methods are compared using MATLAB simulation. In the second section two different circuit have been designed and compared using Electromagnetic simulation with utilization of GaAs pHEMT 0.1 μm process model. The designed circuit's simulation results confirm the performance improvement of proposed topology.

2. Noise Analysis

To calculate the noise factor of the LNA, transfer function of each noise sources have been calculated. The topology of proposed LNA which uses an IDCS stage instead of CS is presented in fig. 2. The noise model of transistor is also shown in fig. 3. Due to their inconsiderable effect and negligible magnitude, the noise of R_d and R_s (parasitic resistors of the drain and source) are neglected. Also the effect of the output resistance of the transistor (r_o), gate-drain capacitance (C_{gd}) and drain-source capacitance (C_{ds}) are neglected in this analysis for simplicity.

The noise sources of the transistors are the noise current in the drain (i_{nd}) and gate resistor's noise source (v_{nrg}). To calculate the NF the transfer function of the output voltage with respect to each of these noise sources are calculated.

$$\begin{aligned} \overline{i_{nd}^2} &= 4kTg_m\gamma\Delta f \\ \overline{v_{nrg}^2} &= 4kTR_g\Delta f. \end{aligned} \quad (2)$$

Considering the input admittance of common-gate and common-source stage to be Y_1 and Y_2 respectively, the condition of input impedance matching can be calculated.

$$\begin{aligned} Y_1 &= \frac{C_{gs1}s}{C_{gs1}R_{g1}s+1} + g_m \\ Y_2 &= \frac{C_{gs2}s}{C_{gs2}L_s s^2 + (g_{m2}L_s + C_{gs2}R_{g2})s + 1} \end{aligned} \quad (3)$$

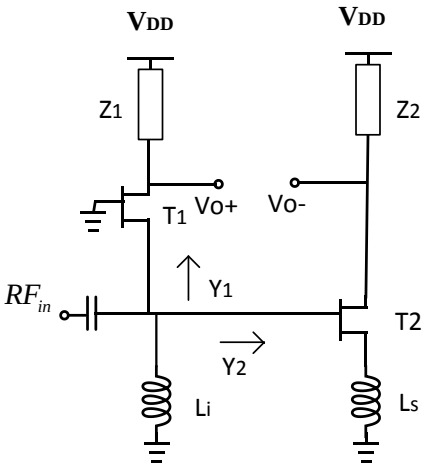

Figure 2: Schematic of new noise cancellation technique

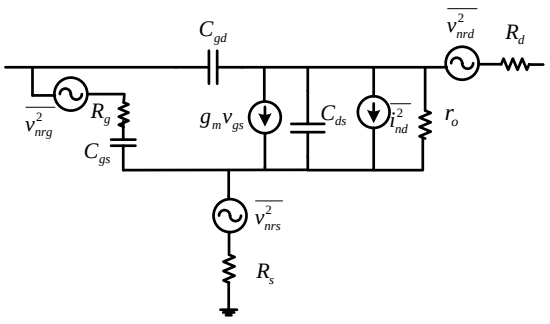

Figure 3: Noise model of transistor

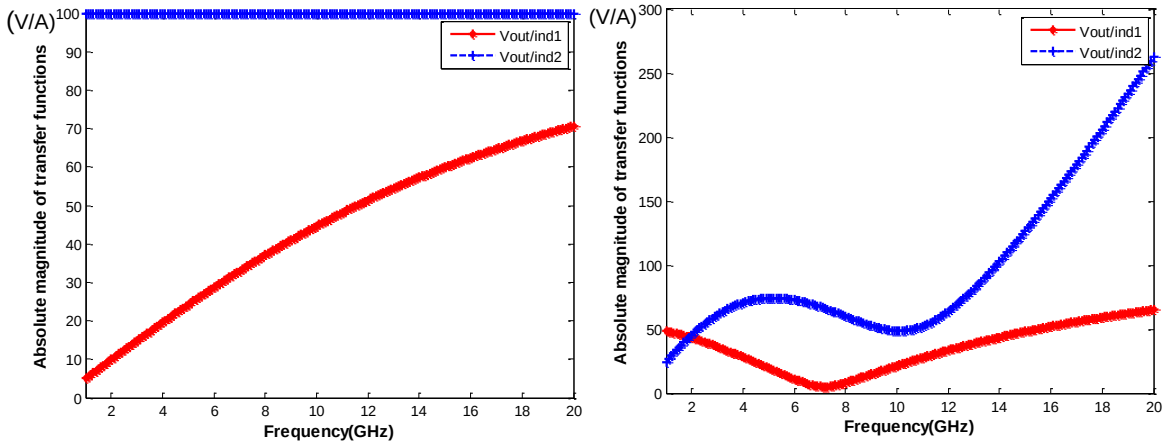

Figure 4: Absolute magnitude of transfer functions: (a) Conventional method (b) Proposed method

In the design frequency band the effect of R_g in input admittance is inconsiderable due to its negligible magnitude because $\omega \ll \frac{1}{R_g C_{gs1}}$ and $\omega \ll \frac{1}{R_g C_{gs2}}$. To have real value for input admittance of IDCS stage, the source inductor is selected in a way that $C_{gs2} L_s \omega^2 = 1$. Therefore, the Y_1 and Y_2 becomes $C_{gs1} + g_m$ and $\frac{C_{gs2}}{g_{m2} L_s}$ respectively and for obtaining matching condition, source admittance (Y_s^*) should be equal to $Y_1 + Y_2$.

$$\frac{1}{R_s} - \frac{1}{L_i s} = C_{gs1} s + g_m + \frac{C_{gs2}}{g_{m2} L_s} \tag{4}$$

Considering (4) for input matching these conditions should be met

$$\begin{aligned} L_i &= \frac{1}{C_{gs1}\omega^2} \\ g_{m2} L_s &= g_{m2} L_s g_{m1} R_s + C_{gs2} R_s \end{aligned} \tag{5}$$

Considering these constraints, and $Z_1 = R_1$, the transfer function of CG and IDCS stage's noise sources are calculated in (6)-(9). The transfer function of source voltage is also shown in (10).

$$A = \frac{V_{out}}{i_{nd1}} = \frac{(R_1 C_{gs2} R_s + L_s R_1 g_{m2}) s - Z_2 g_{m2} R_s)}{2 L_s g_{m2} s} \tag{6}$$

$$B = \frac{V_{out}}{i_{nd2}} = C_{gs2} R_s \frac{R_1 g_{m1} L_s s + Z_2}{(L_s s g_{m2}(1 + R_s g_{m1}) + C_{gs2} R_s)} \tag{7}$$

$$C = \frac{V_{out}}{V_{nrg1}} = \frac{L_s R_1 g_{m1} s + R_2}{L_s s} \tag{8}$$

$$D = \frac{V_{out}}{V_{nrg2}} = \frac{(R_1 g_{m1} L_s s + R_2)\left({g_{m2}}^2 L_s (1 + R_s g_{m1})\right)}{(L_s g_{m2}(1 + R_s g_{m1}) + C_{gs2} R_s)} \tag{9}$$

$$E = \frac{V_{out}}{v_{ns}} = g_{m2} R_s \frac{(R_1 g_{m1} L_s s + Z_2 g_{m2})}{(L_s g_{m2}(1 + R_s g_{m1}) + C_{gs2} R_s)} \tag{10}$$

The overall NF can be calculated using following equation:

$$NF = 1 + \gamma g_{m1} \frac{|A|^2}{|E|^2} + \gamma g_{m1} \frac{|B|^2}{|E|^2} + R_{g1} \frac{|C|^2}{|E|^2} + R_{g2} \frac{|D|^2}{|E|^2} \tag{11}$$

To have the noise cancellation condition, it is known that the transfer function of CG stage's noise source should be equal to zero. This condition is met using (12).

$$\left| A = \frac{V_{out}}{i_{nd1}} = \frac{(R_1 C_{gs2} R_s + L_s R_1 g_{m2}) s - Z_2 g_{m2} R_s)}{(L_s g_{m2}(1 + R_s g_{m1}) + C_{gs2} R_s) s} \right|^2 = 0 \tag{12}$$

This equation shows that the load of IDCS stage should be inductive and its inductor value can be calculated using (13).

$$\begin{aligned} R_1 C_{gs2} R_s + L_s R_1 g_{m2} - L_2 g_{m2} R_s = 0 \\ L_2 = \frac{R_1 C_{gs2}}{g_{m2}} + \frac{L_s R_1}{R_s} \end{aligned} \tag{13}$$

Under these circumstances, the condition for having simultaneous impedance matching and minimum NF can be obtained and this topology can be used as a CG noise canceling method which can decrease the NF in comparison to conventional approach. To have a better look on this topology, we used MATLAB code to show the absolute magnitude of $\frac{v_{nout}}{i_{nd1}}$ and $\frac{v_{nout}}{i_{nd2}}$ in each stage in both conventional and proposed topology versus frequency. The transfer function is calculated with the transistor model and by use of its element's magnitudes the frequency behavior is depicted in Fig. 4.

As it shows due to the effect of considering C_{gs} in calculations, the transfer function of v_{out}/i_{nd1} in conventional method is not exactly equal to zero. These two LNAs are designed to have noise cancellation condition at $f = 10GHz$ and input impedance matching. Due to derived equations, the value of source inductance of IDCS stage is calculated. The results show that the magnitude of transfer function of noise sources can be reduced in proposed method in designed frequency band which can lead to reduction in NF.

3. Circuit Design

To validate the theoretical and simulation results, two different noise canceling CG LNA with conventional approach

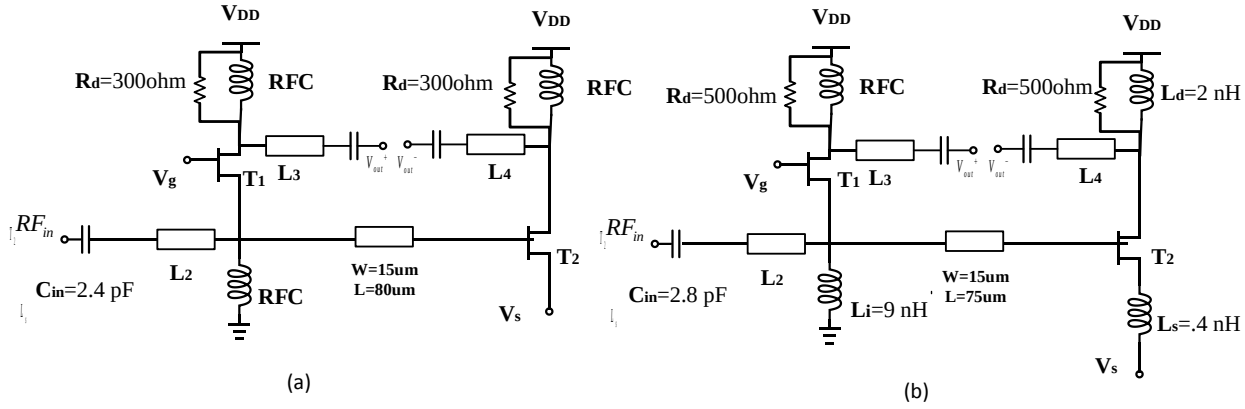

Figure 5: Schematic of designed LNAs: (a) Conventional method (b) Proposed method

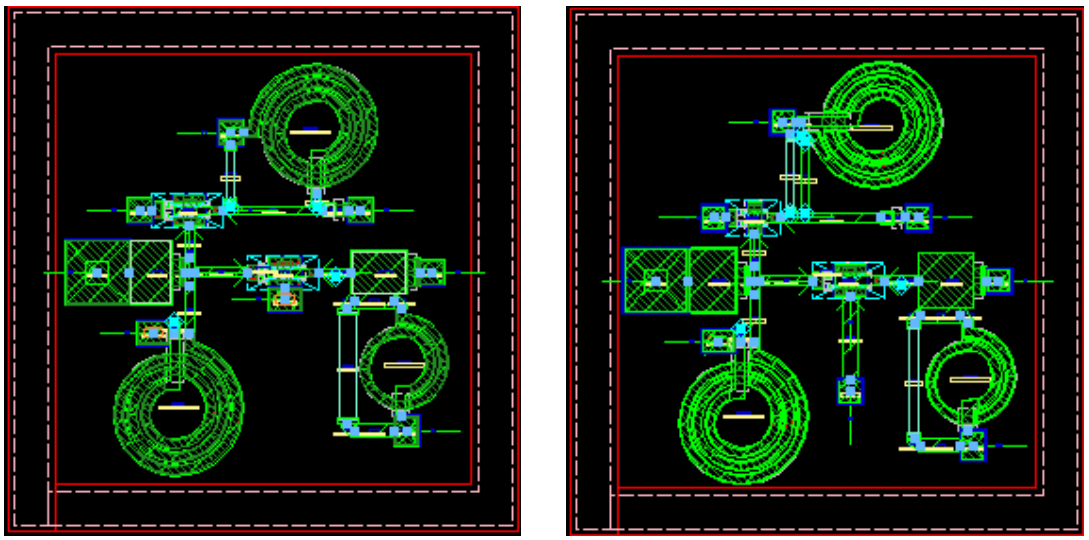

Figure 6: Layout micro-graph of designed LNAs: (a) Conventional method (b) Proposed method

Table 1: Performance comparison of LNAs with similar design approach and bandwidth

Ref	Technology	Bandwidth (GHz)	DCPower (mW)	Gain (dB)	Design Method	S_{22} (dB)	S_{11} (dB)	NF (dB)
[19]	.18um CMOS	2.4-9	–	24	Broadband Noise canceling	-10	-7.5	3.16
[20]	.18um CMOS	1.2-11.9	20	9.7	Broadband Noise canceling	-11	-10	4.5
[21]	.18um CMOS	1.25-11.34	5.8	11	Gm-boosted Noise cancellation	-11	–	2.4
[22]	.18um CMOS	3.1-10.6	12.5	13.4	Broadband Noise canceling	-10	-10	3.7-4.5
[23]	.13um CMOS	3.1-10.6	9.13	15.33	Broadband Noise canceling	-10	-10	2.65-3.45
This work	100nm GaAs	10-12	56.6	6.5	Conventional Noise cancellation	-10	-8	2.25
This Work	**100 nm GaAs**	**9.8-11**	**43.5**	**7**	**Proposed Noise cancellation**	**-10**	**-12**	**1.75**

and proposed approach have been designed using ADS. To compare these two topologies and to see if the proposed approach can make an improvement in ideal condition, these LNAs needs to be compared completely with the exact same condition. This can only happen in simulation environment. By comparing these two topologies in ADS, it can surly be assumed that the transistors and passive elements have the exact same parameters and the comparison can be done. These two LNAs have been optimized and designed using GaAs pHEMT .1 μm process model. In this process the thickness of the substrate is 50 μm. The process offers two metal layers with 1- and 2- μm thickness, air bridges, and ground back-vias and the unity gain frequency f_T and the maximum oscillation frequency f_{max} of the process are 130 and 180

GHz. Other passive components of this process include the metal-insulator-metal (MIM) capacitors with a capacitance density of 400 pF/mm^2, and thin film and mesa resistors with sheet resistances of 50 and 140 $^{\Omega}/_{\square}$ respectively.

The LNAs are designed in X-band. The first LNA is optimized considering the conventional noise cancellation technique by using CS stage and the second LNA is designed by using an IDCS stage. The transistors in this process have relatively higher g_m than 20 mS. This makes it harder for the conventional approach to have good input matching but it has rather low NF. On the other hand the proposed approach due to real value in input impedance in IDCS stage can have better input matching.

The schematic of both LNAs are depicted in Fig. 5. The output matching of each stage is designed to meet its own load requirement. In the proposed method by adding a degree of freedom with source inductor the noise cancellation condition can happens with lower g_{m2} in comparison to conventional method. This can lead to less power consumption. In the designed LNAs, the proposed method can achieve less power consumption. The size of common gate transistors are chosen to be $2 * 50\mu m$ and size of transistors in common source stages are chosen to be $2 * 50\mu m$ and $2 * 30\mu m$ in both conventional and proposed method respectively. The preliminary value of design parameters are calculated using MATLAB simulation. In order to achieve best matching in both input and output of both LNAs, ADS optimization is also done to choose the appropriate magnitudes for circuit elements. In this case, simulation results show the performance improvement of proposed approach in comparison to conventional design method. To consider the high frequency effects of elements, electromagnetic momentum simulation is done for both LNAs. The layout micro-graph of both LNAs are represented in Fig. 6. It should be mentioned that the effect of bond wires are considerable in inductively degenerated common source topology, while it cannot be exactly predicted and measured, these effects are modeled using parasitic resistor and inductors with appropriate range for their magnitudes. These have been added in the final EM simulated circuit and their effect are considered in final simulations and presented results. The NF and gain performance of both LNAs are represented in Fig. 7. It can be seen that the NF decreases in the proposed approach and the gain have a slight increment. The S-parameters of both LNAs are depicted in Fig. 8. The S_{11} of the proposed method is better than -12 dB while the input matching condition in conventional method is better than -8 dB. The output matching in both topologies have a narrow band behavior and at the center frequency the S_{22} of both LNAs are better than -10 dB. The comparison of proposed approach to other works with similar bandwidth and design methods is presented in table 1. It can be seen that the proposed noise cancellation method shows the least NF in comparison to other LNAs. Its gain is less than other LNAs because of being single stage LNA while others are multi-stage LNAs. The input and output matching of all LNAs are in acceptable range. The DC power consumption of proposed LNA is higher than other LNAs due to different process model.

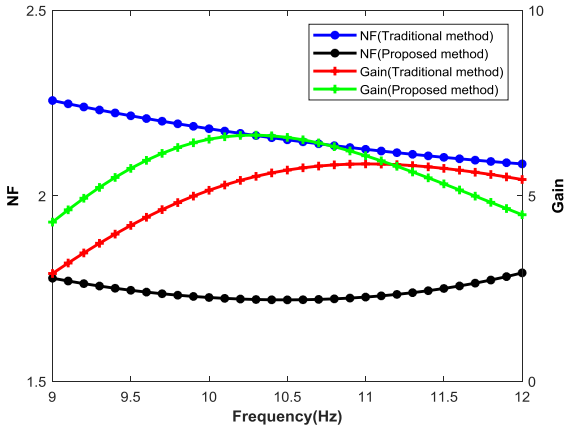

Figure 7: NF and Gain of both LNAs

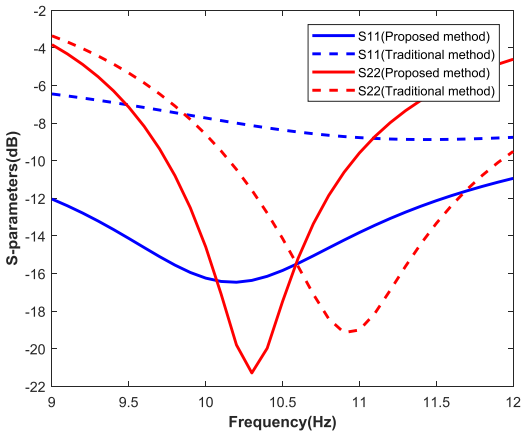

Figure 8: S-parameters of both LNAs

4. Conclusion

In this paper, a new methodology for designing noise cancellation CG LNAs is proposed. The analytical calculations for design parameters of this topology are also presented. Using MATLAB simulation the analytical and numerical analysis have shown that according to this topology the absolute magnitude of transfer function of noise sources decrease in comparison to conventional noise canceling technique which leads to better NF performance. To validate the theoretical analysis, two different noise canceling LNAs are designed. The first LNA designed using a CS stage in parallel with CG stage and the second one is designed using IDCS instead of CS stage. The EM simulation results have shown that in proposed method with slight degradation in power consumption, the NF is decreased and better input impedance matching is obtained while the gain has slightly improved.

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