



HAL
open science

A New Multilevel Inverter Topology Based on Cascade H-Bridge and Extended Boost Quasi Z-Source for Photovoltaic System Applications

Behrad Shirmardp, Reza Choupanp, Ali Zakerianp, Daryoosh Nazarpourp

► To cite this version:

Behrad Shirmardp, Reza Choupanp, Ali Zakerianp, Daryoosh Nazarpourp. A New Multilevel Inverter Topology Based on Cascade H-Bridge and Extended Boost Quasi Z-Source for Photovoltaic System Applications. 7th conference on renewable, clean and efficient energies, May 2015, Tehran, Iran. <hal-02545355>

HAL Id: hal-02545355

<https://hal.science/hal-02545355v1>

Submitted on 17 Apr 2020

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

A New Multilevel Inverter Topology Based on Cascade H-Bridge and Extended Boost Quasi Z-Source for Photovoltaic System Applications

Behrad Shirmard¹, Reza Choupan², Ali Zakerian³, Daryoosh Nazarpour⁴
Faculty of Electrical Engineering, Urmia University, Urmia, Iran
b.shirmard@gmail.com

Abstract

Nowadays, photovoltaic power systems are widely accepted due to the worldwide energy shortage. This paper proposes a new multilevel inverter topology based on Cascaded H-bridge (CHB) and Extended Boost Quasi Z-source (EBQZS), which can change output voltage in a wide range, usable in photovoltaic systems (PV). In other words, output voltage amplitude is not limited to DC voltage source. Proposed topology consists, solitary DC source and EBQZS, therefore, it is more reliable against short circuit and also it has small size compared to the typical CHB-MLI in which several DC voltage sources is applied. This topology uses a shoot-through control switching to adjust output voltage. The proposed topology is simulated by the MATLAB/Simulink and the results conform the performance of the topology.

Keywords: Cascaded H-Bridge (CHB), Multilevel Inverter (MLI), Z-Source inverter (ZSI), Extended Boost Quasi Z-Source (EBQZS), Photovoltaic (PV), shoot-through state.

1- Behrad Shirmard, M.Sc. Student.

2, 3, 4- Reza Choupan, M.Sc. Student, Ali Zakerian, M.Sc. Student, Daryoosh Nazarpour, Associate Professor.

1- INTRODUCTION

In recent years, due to energy crisis, renewable energy sources, such as wind, photovoltaic (PV) and fuel cell are becoming more popular in industrial and residential applications. Today, PV cells are used in many applications due to the advantages like less maintenance, free from pollution and zero fuel cost [1]. In PV generation, power converter interface is the major part in the overall system [2]. Fig. 1, shows the structure of photovoltaic systems. In PV power generation the output voltage varies depending on the temperature and solar irradiation changes. Because of the wide voltage range variations of the PV power generation, the traditional inverter either oversized to cope with the variations or a DC-DC boost circuit should be used. However, both ways are cost, reliability and efficiency killers of the system [2].

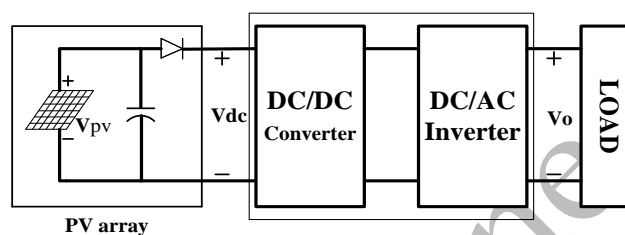


Fig. 1. The structure of photovoltaic systems.

The main point in this study is proposing a structure to link the PV output DC voltage to the load. Voltage Source Inverter (VSI) is one of the power electronic equipment that is used in this field. However, restrictions of traditional VSI, such as, phase legs short-circuit risk and limited obtainable output voltage can be overcome by the Z-source inverter [3].

Over the recent years, many researchers have worked on developing different kinds of topological variations, while others have worked on developing Z-Source Inverter (ZSI) into different applications, where component sizing, modeling, analysis, controller design, and modulation method are addressed [4–8]. To improve on the traditional ZSIs, new quasi-Z source inverters, have been developed which feature several improvements and no disadvantages when compared to the traditional ZSIs. The advantages of these topologies include reduced passive component ratings, reduced component count, and improved input profiles [7, 8]. Another family of quasi-ZSI, extended boost quasi-ZSI [9] is introduced to fill the vacancies in development of ZSI. The most important profits of this topology are increasing gain and its expandability as that for each added new stage the boost factor can be increased by a constant factor and lower voltage stress across the capacitors compared to those of traditional ZSI.

On the other hand cascaded H-bridge (CHB) multilevel inverter is one of the popular converter topologies used in high-power medium-voltage (MV) drives [10–12]. This structure needs fewer number of power electronic components than other classic topologies. Cascaded H-bridge inverter is useful because of the following advantages:

- I. A modularized circuit layout and packaging is possible because each H-bridge cell has the same structure.
- II. It does not need extra clamping diodes (compared with diode clamped structure) or voltage balancing capacitors (compared with flying capacitors structure).

III. It requires the reduced number of components to achieve the same number of output voltage levels among the conventional multilevel inverters [13].

Despite these advantages, independent DC-link voltage needs to be provided by each H-bridge separately, output voltage amplitude of cascaded H-bridges multilevel inverter is limit to DC voltage source and output voltage amplitude cannot boosted flexibility.

Therefore, this paper proposes a new topology based on CHB and EBQZS that can increase the output voltage of the PV in a wide range which is not limited to the output DC voltage of the PV array. This paper covers following sections:

Section 2 introduces EBQZS inverter and describes the analysis of its circuit, Section 3 introduces the proposed topology, section 4 presents the simulation results, and the conclusion placed at the final section.

2- EXTENDED BOOST QUASI Z-SOURCE INVERTER TOPOLOGY

Extended Boost Quasi Z-Source (EBQZS) converter as z-source converter can utilize shoot-through (short circuit) states to boost the input DC voltage of inverter switches by gating on both upper and lower switches of a phase leg. Occurring of short circuit can destroy traditional inverters but in the family of Z-source inverters with control of shoot-through state it becomes more reliable. In [9] there are four topologies for EBQZS inverters. These topologies can be categorized mainly as diode assisted boost and capacitor assisted boost and can be further divided into continuous current and discontinuous current topologies. All these topologies can be modulated using the modulation methods proposed for the original ZSI. The main advantages of these topologies are their expandability and possibility of increasing voltage in comparison with original ZSI.

In this paper, capacitor-assisted topology is used, because it would produce high boost with smaller shoot-through and cause lower voltage stress on devices [9]. Discontinuous-current and continuous-current capacitor-assisted EBQZS with single H-bridge inverter structure is shown in Fig. 2.

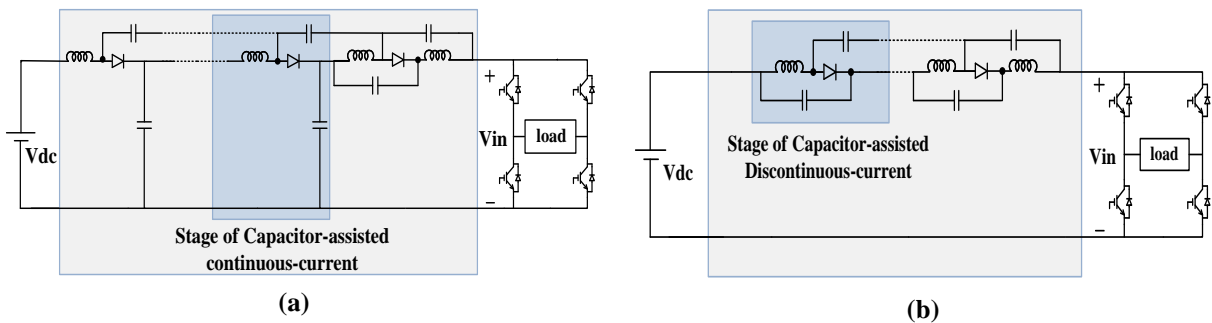


Fig. 2. Capacitor-assisted extended-boost quasi Z-source.
(a) Discontinuous-current (b) Continuous-current

The following equations are obtainable according to Fig. 3(a) that is one stage of Capacitor-assisted boost.

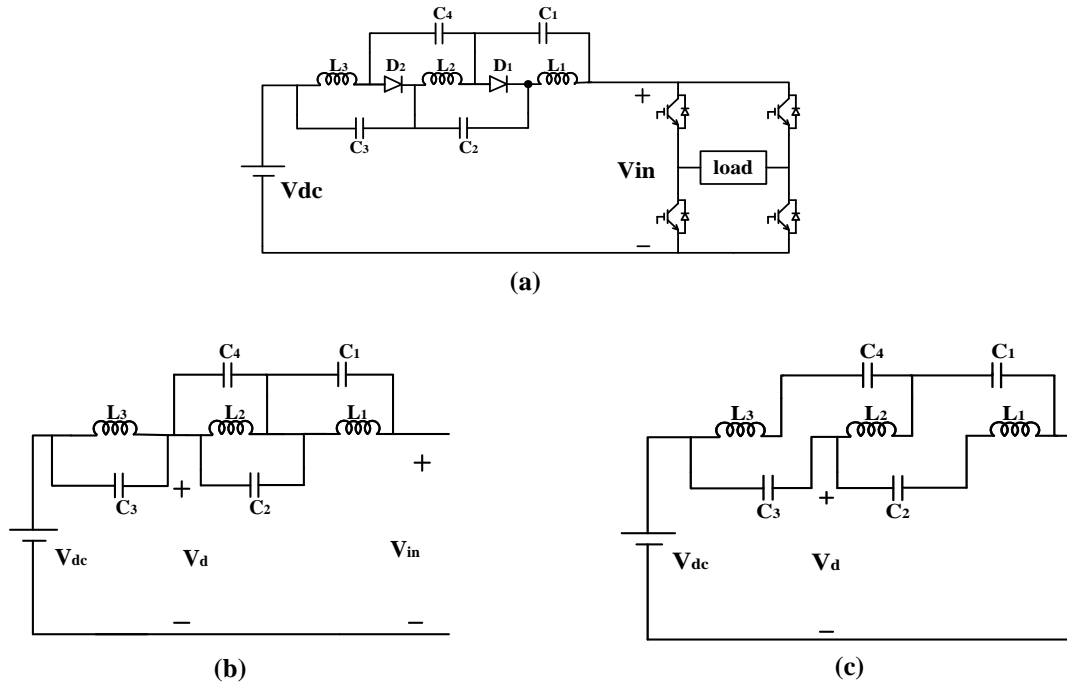


Fig. 3. (a) Structure of the capacitor-assisted extended-boost discontinuous current quasi Z-source first extension (b) Non-shoot-through state. (c) Shoot-through state.

First, consider equivalent circuit of non-shoot-through state shown in Fig. 3(b), which is represented with an open circuit. Then, the following steady-state equations can be observed by applying KVL.

$$V_{C_1} = V_{L_1} \quad (1)$$

$$V_{C_2} = V_{L_2} \quad (2)$$

$$V_{C_3} = V_{L_3} \quad (3)$$

$$V_{dc} + V_{C_3} = V_d \quad (4)$$

Consider equivalent circuit of shoot-through state shown in Fig. 3(c):

$$V_d + V_{C_2} + V_{L_1} = 0 \quad (5)$$

$$V_d + V_{C_1} + V_{L_2} = 0 \quad (6)$$

$$V_{dc} + V_{C_3} = V_d \quad (7)$$

It is assumed that average voltage of inductor is zero and by defining the shoot-through duty ratio as D_S and non-shoot through duty ratio as D_A where $D_A + D_S = 1$, so the following equations can be derived:

$$D_S = \frac{T_{sh}}{T} \quad (8)$$

$$D_A = \frac{T_{ns}}{T} \quad (9)$$

$$V_d = \frac{1 - 2D_S}{1 - 3D_S} V_{dc} \quad (10)$$

$$V_{in} = \frac{1}{1-3D_s} V_{dc} \quad (11)$$

Where, T_{sh} is the total shoot-through state period and T_{ns} is the total non-shoot-through state period during all period of switching, T . According to the above equations, boost factor for one stage capacitor-assisted extended-boost is as follows:

$$B = \frac{1}{1-3D_s} \quad (12)$$

The following equation is obtained for both structures of capacitor-assisted extended-boost in which the boost factor will increase while the number of stages increases.

$$B = \frac{1}{(1-(n+2)D_s)} \quad (13)$$

Where, n is the number of capacitor assisted stages. Similar argument, boost factor relation for both topologies discontinuous-current and continuous-current for diode-assisted can be written as:

$$B = \frac{1}{(1-2D_s)(1-D_s)^n} \quad (14)$$

Fig. 4, shows the comparison between boost factor of the Z-source and EBQZS. According to this figure, voltage enhancement ability in EBQZS is more than Z-Source for same rate of the shoot-through state, and also the capacitor assisted boost structure operates better than diode assisted boost.

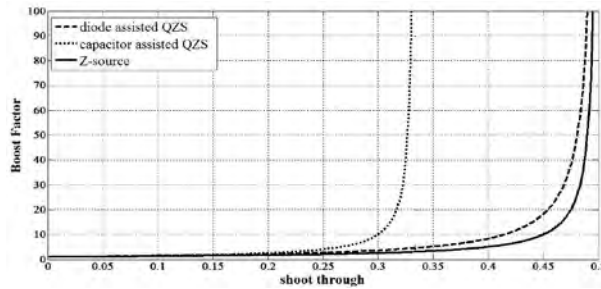


Fig. 4. Boost Factor capability of different topologies.

3- PROPOSED TOPOLOGY

Fig. 5, shows a circuit configuration of the proposed new multilevel inverter topology based on CHB and EBQZS for single-phase applications. In this paper, a cascaded H-bridge multilevel inverter is suggested which applies one single input DC voltage source, one Z impedance network, some isolated single-phase transformers and H-bridge cells.

In Fig. 5, H-bridge modules are connected in parallel to the unit DC input source (EBQZS). In this structure, the output voltages of H-bridge modules apply as input voltage for transformers and the secondary windings of the transformers are connected in series. The amplitude of the output voltage is determined by the input voltage and turn ratio of the transformer. Each primary terminal of the transformer is connected to an H-bridge module to produce V_{in} , zero, and $-V_{in}$. The number of output voltage levels in the suggested topology is $2n+1$ where n is the number of H-bridge cells.

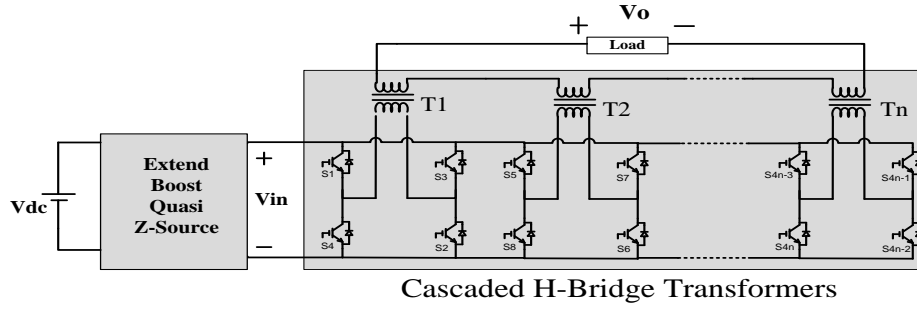


Fig. 5. Proposed new inverter topology based on CHB and EBQZS.

Several modulation techniques have been presented for multilevel inverters such as sinusoidal PWM [14], space vector PWM (SV-PWM) [15-16], selective harmonic elimination (SHE-PWM) [17-18], fundamental frequency switching [19] and so on. The widely used multicarrier PWM methods are known as Phase Shifted (PS), Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposite Disposition (APOD), Hybrid (HD) and Phase Shift (PS) [20]. For this topology, Phase opposition disposition (POD) multicarrier PWM method is utilized.

Since the small modulation index increases the THD [21], both the modulation index and shoot-through state are used in this paper to control the output voltage. Turning zero states into the shoot-through states and keeping the active switching states unchanged is the main point of the control. In other words, the shoot-through states only occur during the zero states. During the shoot-through state, the output voltage of EBQZS is zero ($V_{in} = 0$). In this case, besides upper keys of H-bridge, the other switches, that is lower keys, are turned on and vice versa. While, in non-shoot-through state only upper keys and lower keys are turned on according to Table 1.

TABLE 1. Switching states and output voltage for proposed topology

Voltage level	Output voltage	State	ON switches
1	nV_{in}	Non-shoot through (Active state)	$S_1, S_2, S_5, S_6, S_9, S_{10}, \dots, S_{(4n-3)}, S_{(4n-2)}$
2	$(n-1)V_{in}$	Non-shoot through (Active state)	$S_1, S_2, S_5, S_6, S_9, S_{10}, \dots, S_{(4n-3)}, S_{(4n-1)}$
		⋮	
$n-1$	$2V_{in}$	Non-shoot through (Active state)	$S_1, S_2, S_5, S_6, S_9, S_{11}, \dots, S_{(4n-3)}, S_{(4n-1)}$
n	V_{in}	Non-shoot through (Active state)	$S_1, S_2, S_5, S_7, S_9, S_{11}, \dots, S_{(4n-3)}, S_{(4n-1)}$
$n+1$	0	Non-shoot through (Zero state)	$S_1, S_3, S_5, S_7, S_9, S_{11}, \dots, S_{(4n-3)}, S_{(4n-1)}$
$n+1$	0	shoot through	All switches
$n+1$	0	Non-shoot through (Zero state)	$S_2, S_4, S_6, S_8, S_{10}, S_{12}, S_{14}, S_{16}$
$n+1$	0	shoot through	All switches
$n+2$	$-V_{in}$	Non-shoot through (Active state)	$S_3, S_4, S_6, S_8, S_{10}, S_{12}, \dots, S_{(4n-2)}, S_{(4n)}$
$n+3$	$-2V_{in}$	Non-shoot through (Active state)	$S_3, S_4, S_7, S_8, S_{10}, S_{12}, \dots, S_{(4n-2)}, S_{(4n)}$
		⋮	
$2n$	$-(n-1)V_{in}$	Non-shoot through (Active state)	$S_3, S_4, S_7, S_8, S_{11}, S_{12}, \dots, S_{(4n-2)}, S_{(4n)}$
$2n+1$	$-nV_{in}$	Non-shoot through (Active state)	$S_3, S_4, S_7, S_8, S_{11}, S_{12}, \dots, S_{(4n-1)}, S_{(4n)}$

The shoot-through control method for output voltage is explained in the next section.

4- SIMULATION RESULTS

Fig. 6, shows the proposed topology structure to produce the 13-level output voltage. The CBPWM switching method and POD technique is used in this structure. Simulation results have obtained by the MATLAB/Simulink software and the structure parameters is presented in Table 2.

TABLE 2. Electrical specifications of the proposed topology

Frequency	50 Hz
V _{dc}	50 V
Load Resistor	150 Ω
Load Inductor	100 mH
Extend Capacitor	100 μF
Extend Inductor	5 mH
Switching Frequency	2000 Hz

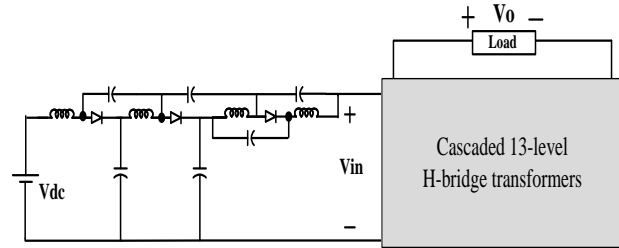


Fig. 6. Thirteen level proposed topology.

As it mentioned, for this topology, Phase opposition disposition (POD) multi-carrier PWM method is utilized. POD technique employs $(m - 1)$ numbers of carriers for m -level phase waveforms where the carriers above the zero reference are in phase but shifted by 180° from those carriers below the zero reference. The carriers are defined with the same frequency (f_c) and amplitude (A_c). The amplitude of the modulator is denoted as (A_m) and the frequency (f_m). In multilevel inverters, the amplitude modulation index (m_a), and the frequency ratio (m_f), are given by (15) and (16), respectively:

$$m_a = \frac{A_m}{(m-1)A_c} \quad (15)$$

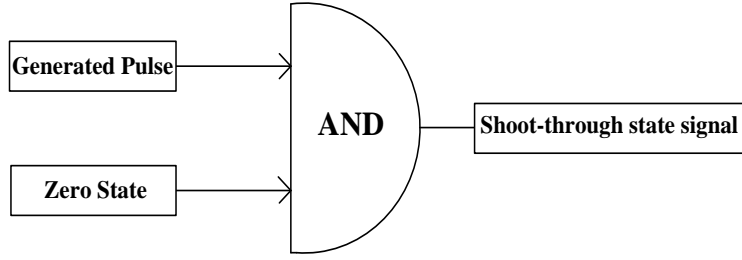
$$m_f = \frac{f_c}{f_m} \quad (16)$$

This topology uses shoot-through state signal for controlling the output voltage. According to Fig.7, AND logical gate have two inputs: one of them is Generated Pulse, produced by pulse generator with T_{GP} period, and the other one is Zero State, produced by logical gates according to Table 2. Output signal is high when both the input signals are high.

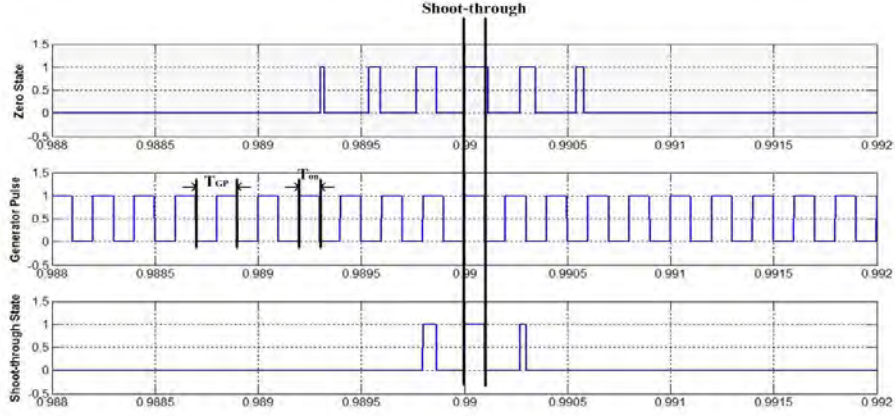
Duty cycle of generated pulse, D is obtained as:

$$D = \frac{T_{on}}{T_{GP}} = \frac{T_{sh}}{T_{zs}} \quad (16)$$

Where, T_{on} is high state time of generated pulse at T_{GP} . T_{zs} and T_{sh} are total zero state time and total shoot-through time during switching period, T .



(a)



(b)

Fig. 7. Shoot-through state generation.

(a) Shoot-through state signal generator circuit.

(b) Zero state, generator pulse and shoot-through state signals.

Boost factor is obtained as:

$$B = \frac{1}{1 - 4 \frac{T_{sh}}{T}} \quad (18)$$

According to relation (17) Boost Factor can be derived as:

$$B = \frac{1}{1 - 4 \frac{DT_{zs}}{T}} \quad (19)$$

It is considerable that boost factor B will be increased by increasing D . Consequently, both the EBQZS network output voltage, V_{in} in Fig. 6, and load voltage will be increased too.

Figs. 7(a) to (c) show the output voltage and harmonic spectrum, output current and harmonic spectrum and output voltage of EBQZS (V_{in}) for duty cycle of zero percent which have been considered for generated pulse. Similarly Figs. 8 and 9 show the same parameters for duty cycle 50 and 100 percent, respectively.

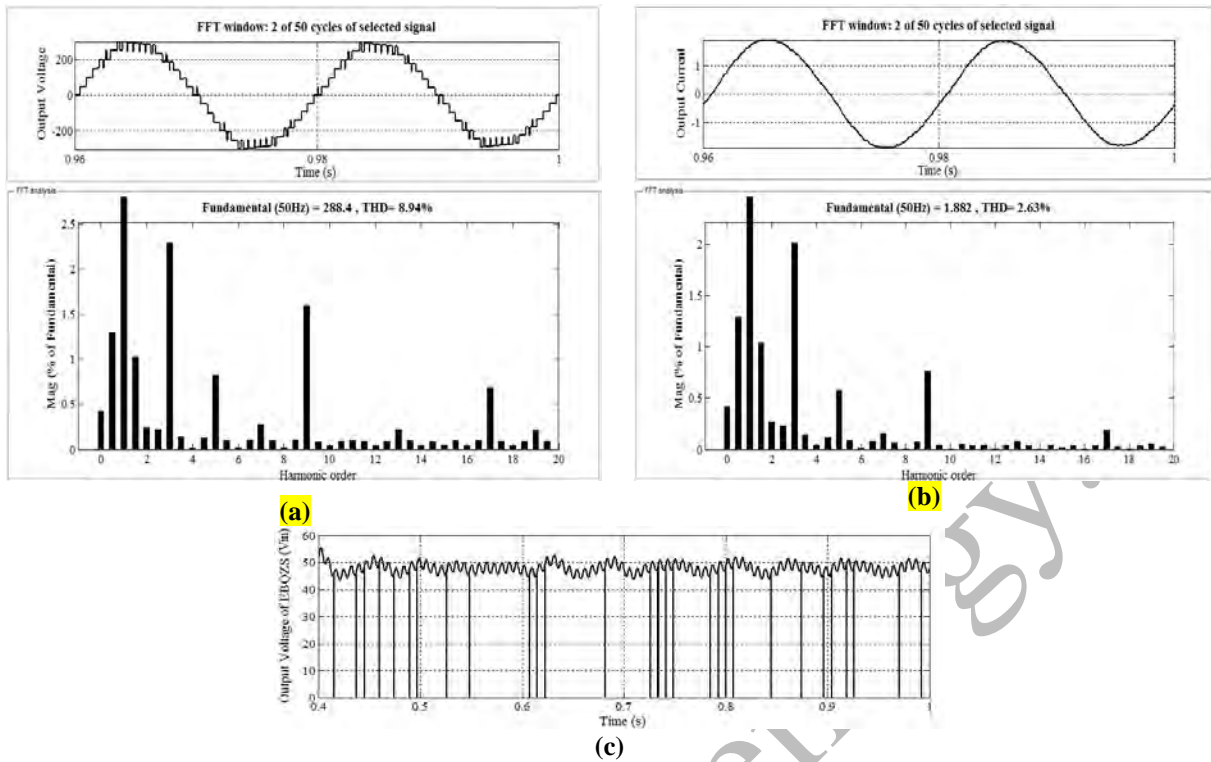


Fig. 7. Output voltage, Output current and V_{in} for $D = 0\%$

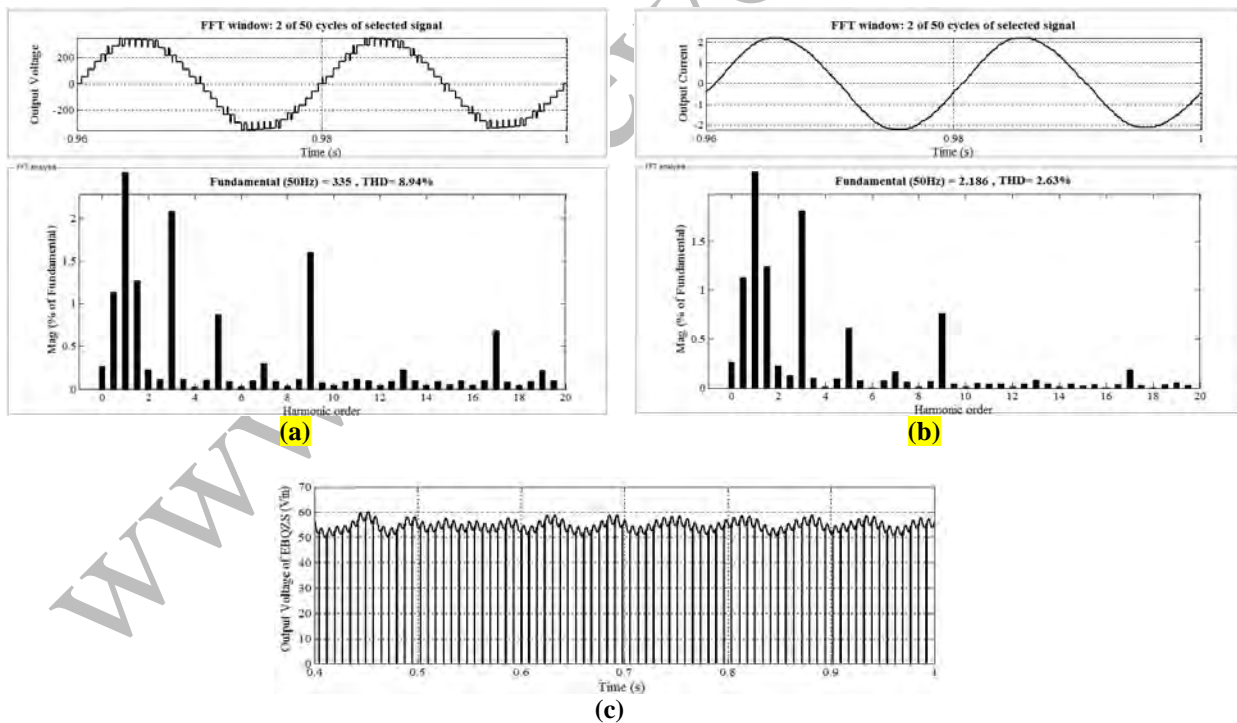


Fig. 8. Output voltage, Output current and V_{in} for $D = 50\%$

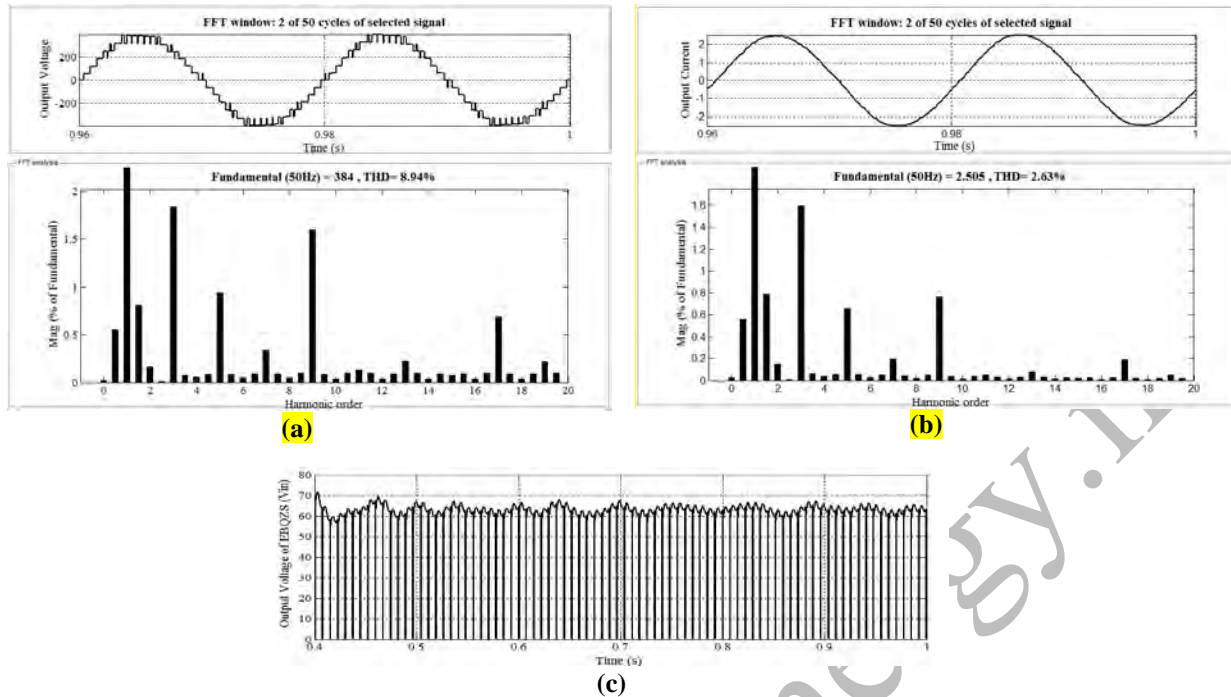


Fig. 9. Output voltage, Output current and V_{in} for $D = 100\%$

By comparing the Fig. 7(a) and Fig. 9(a), it can be inferred that the output voltage have been increased. According to Figs. 7, 8 and 9, it is inferable that output voltage will be altered by variation of shoot-through and will be increased by adding EBQZS stages. And also THD will be decreased by increase in the number of CHBs.

5- CONCLUSION

In this paper a new multilevel inverter topology based on CHB and EBQZS has been proposed in order to use in photovoltaic systems. This topology can control the output voltage with shoot-through state and it has ability to increase the output dc voltage of PV in a wide range for the multilevel inverters input voltage. Proposed topology was simulated by MATLAB/Simulink and the validity of performance was proved.

REFERENCES

- [1] Y. Huang, M. Shen, F. Z. Peng, J. Wang, 'Z-Source Inverter for Residential Photovoltaic Systems' IEEE Transactions on Power Electronics, vol. 21, no. 6, November 2006.
- [2] Fayyad, Y.; Ben-Brahim, L. "Deadbeat control of Z source inverter with voltage ride-through capability", GCC Conference and Exhibition (GCC), 2013 7th IEEE, On page(s): 204 – 209.
- [3] F. Z. Peng, 'Z-source inverter,' IEEE Trans. Ind. Appl., vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.
- [4] C. J. Gajanayake, D. M. Vilathgamuwa, and P. C. Loh, 'Development of a comprehensive model and a multiloop controller for Z-source inverter DG systems,' IEEE Trans. Ind. Electron., vol. 54, no. 4, pp. 2352–2359, Aug. 2007.
- [5] F. Gao, P. C. Loh, F. Blaabjerg, and C. J. Gajanayake, 'Operational analysis and comparative evaluation of embedded Z-Source inverters,' in Proc. IEEE Power Electron. Spec. Conf. (PESC), 2008, pp. 2757–2763.
- [6] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, C. G. Tin, and Y. Li, 'Pulse width modulation of Z-source inverters,' IEEE Trans. Power Electron., vol. 20, no. 6, pp. 1346–1355, Nov. 2005.
- [7] J. Anderson and F. Z. Peng, 'Four quasi-Z-Source inverters,' in Proc. IEEE Power Electron. Spec. Conf. (PESC), 2008, pp. 2743–2749.
- [8] J. Anderson, F. Z. Peng.: 'A Class of Quasi-Z-Source Inverters', in Proc. of 43rd IAS Annual Meeting, 2008, pp. 1-7.
- [9] Ch. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow 'Extended-Boost Z-Source Inverters', IEEE Transactions on Power Electronics, VOL. 25, NO. 10, October 2010.
- [10] P. W. Hammond, 'A New Approach to Enhance Power Quality for Medium Voltage AC Drives', IEEE Transactions on Industry Applications, Vol. 33, No. 1, pp. 202–208, 1997.

- [11] W. A. Hill and C. D. Harbourt, 'Performance of Medium Voltage Multilevel Inverters', IEEE Industry Applications Society (IAS) Conference, Vol. 2, pp. 1186–1192, 1999.
- [12] R. H. Osman, 'A Medium Voltage Drive Utilizing Series-Cell Multilevel Topology for Outstanding Power Quality', IEEE Industry Applications Society (IAS) Conference, pp.2662–2669, 1999.
- [13] Park, S.J., Kang, F.S., Cho, S.E., Moon, C.J., Nam, H. K.: 'A novel switching strategy for improving modularity and manufacturability of cascaded transformer based multilevel inverters', Elsevier Electr. Power Syst. Res., 2005, 74, (3), pp. 409–416.
- [14] Rotella, M., Penailillo, G., Pereda, J., Dixon, J. : 'PWM method to eliminate power sources in a non-redundant 27-level inverter for machine drive applications', IEEE Trans. Ind. Electron., 2009, 1, (56), pp. 194–201.
- [15] Lopez, O., Alvarez, J., Doval-Gandoy, J., Freijedo, F.D.: 'Multilevel multiphase space vector PWM algorithm', IEEE Trans. Ind. Electron., 2008, 5, (55), pp. 1933–1942.
- [16] Gupta, A.K., Khambadkone, A. M.: 'A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters', IEEE Trans. Power Electron., 2007, 5, (22), pp. 1672–1681.
- [17] Agelidis, V.G., Balouktsis, A.I., Dahidah, M.S.A.: 'A five-level symmetrically defined selective harmonic elimination PWM strategy: Analysis and experimental validation', IEEE Trans. Power Electron., 2008, 1, (23), pp. 19–26.
- [18] Khaled, E.L.N., Abdelhamid, T.H.: 'Selective harmonic elimination of new family of multilevel inverters using genetic algorithms', Energy Convers. Manage, 2008, 1, (49), pp. 89–95.
- [19] Du, Z., Tolbert, L.M., Chiasson, J.N.: 'Active harmonic elimination for multilevel converters', IEEE Trans. Power Electron., 2006, 2, (21), pp. 459–69.
- [20] M. G. Hosseini Aghdam, S. H. Fathi, G. B. Gharehpetian, "Analysis of Multi-Carrier PWM Methods for Asymmetric Multi-Level Inverter", IEEE, pp. 2057-2062, 2008.
- [21] Banaei, M.R., Dehghanzadeh, A.R., Fazel, A., Baghbany Oskouei, A.: ' Switching algorithm for singleZ-source boost multilevel inverter with ability of voltage control', IET Power Electron., 2013, Vol. 6, Iss. 7, pp. 1350–1359.